Power Integrated Circuits

1997

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Power Integrated Circuits

Power ICs from TEMIC Semiconductors include products for power conversion, power management, motor control, and power interface. Devices in the "power IC" category are found in applications which control, regulate, or switch power. While belonging to the larger category of analog ICs, power ICs integrate simple digital interface functions and offer such features as power drivers, and/or switches, along with higher operating voltages.

The semiconductor technology used to manufacture these products is widely known as BiCDMOS. This process integrates bipolar, CMOS, and power DMOS transistors. This mix of technologies allows TEMIC to provide high-performance, cost-effective solutions that directly respond to the needs of the application.

Power Conversion

Power Conversion devices make up our largest family of power IC products. These include PWM controllers and regulator ICs used in dc-to-dc converter applications, including the following:

- off-line or ac-to-dc converters found in low power systems such as cable TV boxes or remote metering equipment for power companies that operate directly off the main ac power source
- distributed power dc-to-dc converters for telecommunications equipment, such as ISDN terminators, line cards in switching exchanges, base stations and PABXs that operate directly off a –48-V distributed bus
- high-performance microprocessor point-of-use dc-to-dc converters that convert the main supply (usually –5 V) to the lower voltage needed by the processor's core voltage
- power converters in portable computing and communication products. In both cases, TEMIC power ICs take the battery power source and convert it to a regulated voltage. A step-down or "buck" converter is usually used in notebook computers, and a step-up or "boost" converter is used in cellular telephones.

Power Management

TEMIC power management products are aimed at a focused group of applications which are either managing batteries or power supplies.

For battery management, we offer two types of products:

- a lithium ion battery protection IC family that provides all the protection features required in the battery pack
- a battery disconnect switch family that is used to manage battery switching in dual-battery systems such as high-performance notebook computers.

For power supply management we offer two types of products as well.

- a current limiter IC that limits the in-rush current from 5- and 12-V supplies when cards are "hot-swapped" in such systems as network hubs, communication exchanges, computer mainframes, and test equipment.
- PC CARD or PCMCIA power switches that switch the 3-, 5-, and 12-V supplies to PC CARD slot. These applications are found primarily in portable computing devices; however, they can be seen in other applications such as phones, cable TV set top boxes, and test equipment.

Motor Control

TEMIC's motor control IC family consists of MOSFET motor drivers with interface and control features that can be used in a variety of motors. These products are designed to drive high-side, half-bridge, full-bridge, and three-phase motor circuits. Typical end products include copiers, printers, scanners, and rotating memory devices (i.e. hard disk drives and optical disk drives). Due to operating voltage ratings, most TEMIC motor control ICs are used in 5-, 12-, and 24-V dc motor systems. One very universal such device, which features adaptive control techniques, can be used as a floating driver in bridge designs for both dc and ac supply voltages. Typical applications for this product include motors for power steering, industrial ac motors, and low-frequency bridges used in un-interruptible power supplies (UPS).

Power Interface

TEMIC's family of power interface ICs consists of bus transceiver ICs used for multiplexing and serial interface automotive applications. Products in this family support both the ISO-9141 CARB standard and Intel's CAN (Car Area Network), which is also being used by the factory automation industry as a communication protocol.

More About This Data Book

This data book includes data sheets, applications notes, and information about available demo boards. In some cases, we have also included the gerber files for application and demo board layouts, should you care to duplicate these designs in your system. We have also included selector guides to help you choose the right products for your application.

About TEMIC Semiconductors

TEMIC Semiconductors is a division of TEMIC, a Daimler-Benz microelectronics company. Members of TEMIC Semiconductors include Siliconix, Telefunken Semiconductors, Matra MHS, and Dialog Semiconductor. With a rich technology portfolio including bipolar, CMOS, DMOS, silicon germanium, and RF bipolar processes, TEMIC Semiconductors provides solutions that save space, prolong battery life, and reduce component count in pace-setting microelectronic designs.

TEMIC
Semiconductors

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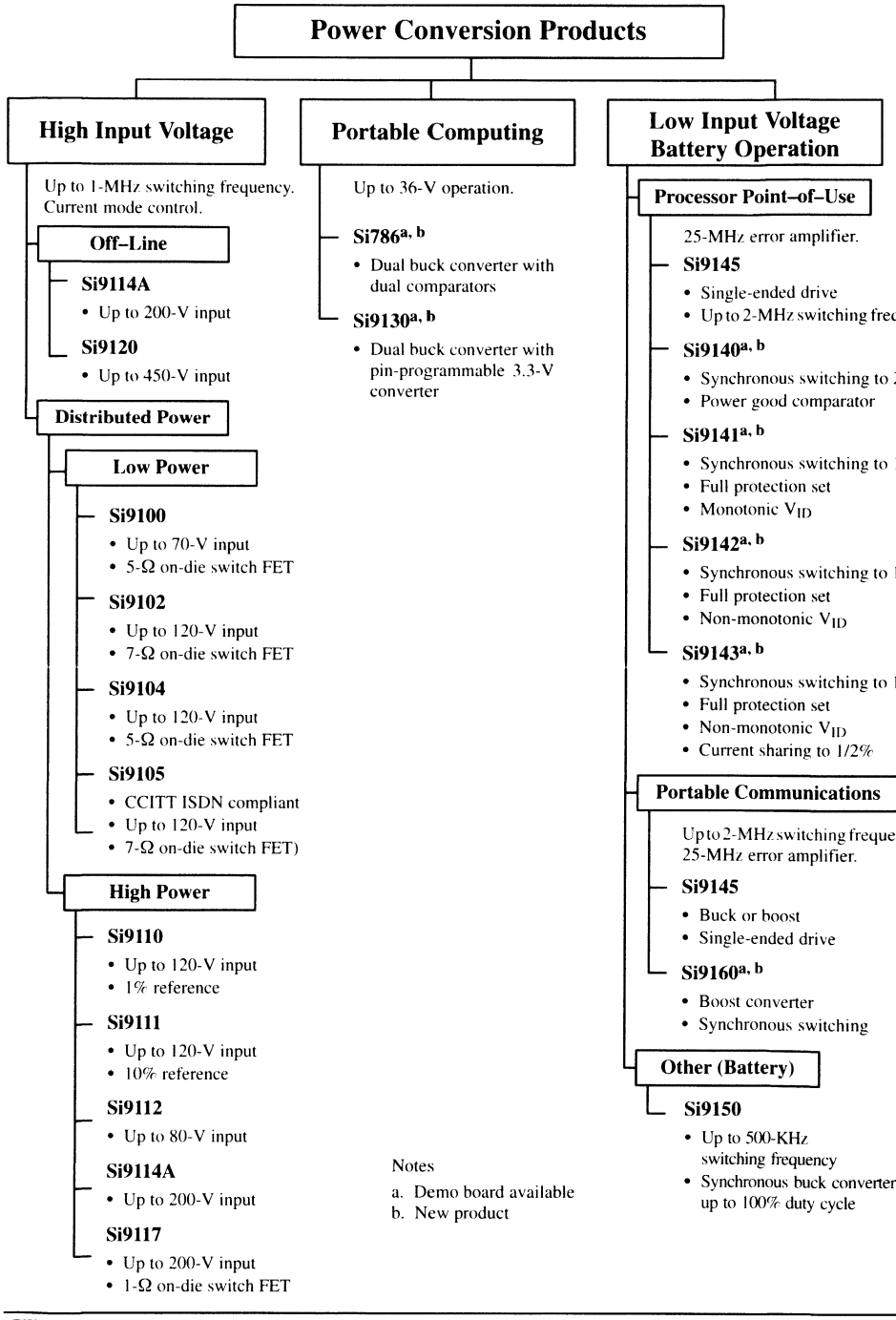
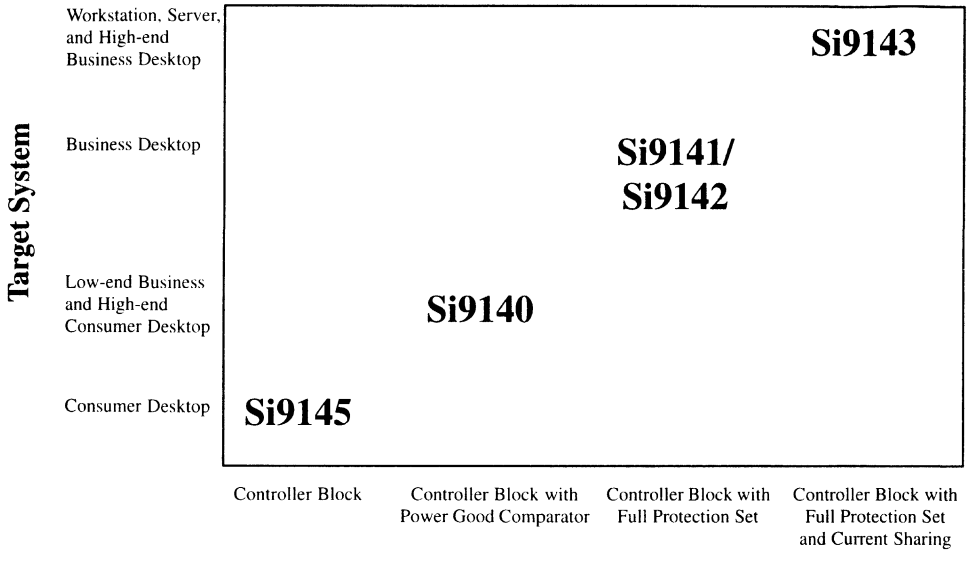
Power Conversion Selector Guide

Part Number	Package	Application	Input Voltage (V)	Mode	Maximum Oscillator Frequency	Reference Voltage (V)	Maximum Supply Current (mA)	Page Number
Distributed Power								
Si9100	DIP-14 PLCC-20	Buck, Flyback, Foward	10 – 70	Current Mode	1 MHz	4	1	1-29
Si9102	DIP-14 PLCC-20	Buck, Flyback, Foward	10 – 120	Current Mode	1 MHz	4	1	1-55
Si9104	SO-16WB	Buck, Flyback, Foward	10 – 120	Current Mode	1 MHz	4	1	1-62
Si9105	SO-16WB DIP-14 PLCC-20	Buck, Flyback, Foward	10 – 120	Current Mode	1 MHz	4	0.5	1-70
Si9110/9111	SO-14 DIP-14	Buck, Flyback, Foward	10 – 120	Current Mode	1 MHz	4	1	1-85
Si9112	SO-14 DIP-14	Buck, Flyback, Foward	9 – 80	Current Mode	1 MHz	4	1	1-111
Si9114A	SO-14 DIP-14	Buck, Flyback, Foward	15 – 200	Current Mode	1 MHz	4	3	1-117
Si9117	SO-16	Buck, Flyback, Foward	15 – 200	Current Mode	1 MHz	4	4.5	1-143
Offline								
Si9120	SO-16 DIP-16	Buck, Flyback, Foward	15 – 450	Current Mode	1 MHz	4	1.5	1-3
Computer Point-of-Use								
Si9140	SO-16	Buck	2.7 – 8	Voltage Mode	2 MHz	1.5	1	1-160
Si9145	SO-16 TSSOP-16	Buck, Boost, Flyback, Foward	2.7 – 8	Voltage Mode	2 MHz	1.5	1.4	1-179
Portable Computer								
Si786	SSOP-28	Dual Buck	5.5 – 30	Current Mode	300 kHz	3.3	1.6	1-212
Si9130	SSOP-28	Dual Buck	5.5 – 30	Current Mode	300 kHz	3.3	1.6	1-226
Portable Communications								
Si9160	TSSOP-16	Boost	2.7 – 7	Voltage Mode	2 MHz	2.5	1	1-258
Other Battery								
Si9150	SO-14	Buck	6 – 18	Voltage Mode	300 kHz	2.5	3	1-240

Product Family Tree



Processor Point-of-Use Converter Family



Si9120

Universal Input Switchmode Controller

Features

- 10- to 450-V Input Range
- Current-Mode Control
- 125-mA Output Drive
- Internal Start-Up Circuit
- Internal Oscillator (1 MHz)
- SHUTDOWN and RESET

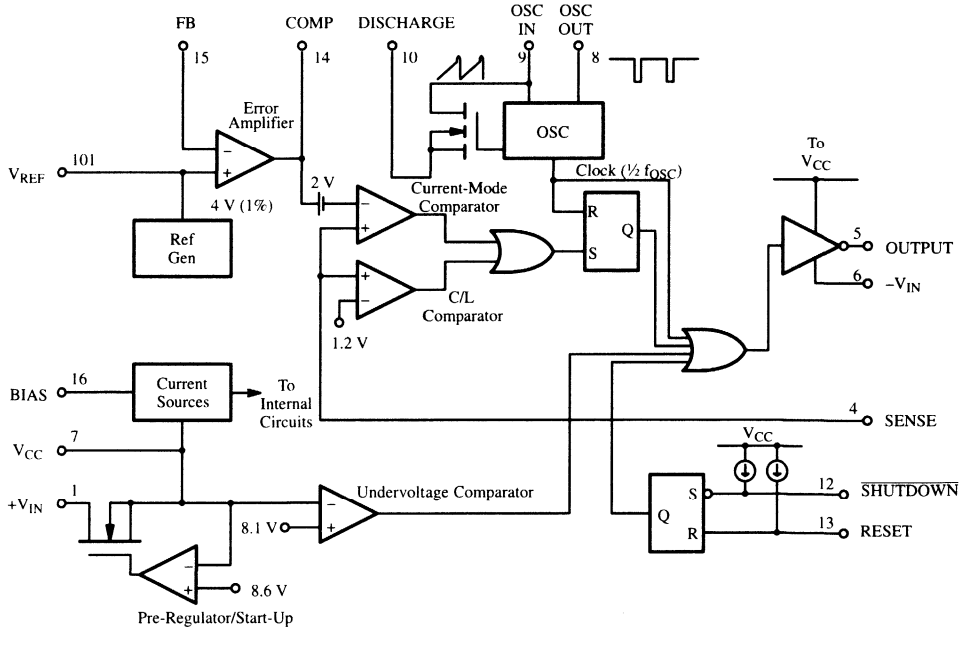
Description

The Si9120 is a BiC/DMOS integrated circuit designed for use in low-power, high-efficiency off-line power supplies. High-voltage DMOS inputs allow the controller to work over a wide range of input voltages (10- to 450-VDC). Current-mode PWM control circuitry is implemented in CMOS to reduce quiescent current to less than 1.5 mA.

A CMOS output driver provides high-speed switching for MOSFET devices with gate charge, Q_g, up to 25 nC, enough to supply 30 W of output power at 100 kHz. These devices, when combined with an output MOSFET and transformer, can be used to implement single-ended power converter topologies (i.e., flyback and forward).

The Si9120 is available in a 16-pin plastic DIP and SOIC packages, and is specified over the industrial, D suffix (–40 to 85°C) temperature range.

Functional Block Diagram



Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70006. Applications information may also be obtained via FaxBack, request documents #70580 and #70578.

Absolute Maximum Ratings

Voltages Referenced to $-V_{IN}$ (Note: $V_{CC} < +V_{IN} + 0.3$ V)
V_{CC} ..... 15 V
$+V_{IN}$ ..... 450 V
Logic Inputs (RESET
$\overline{\text{SHUTDOWN}}$, OSC IN, OSC OUT) ..... –0.3 V to V_{CC} + 0.3 V
Linear Input
(FEEDBACK, SENSE, BIAS, V_{REF}) ..... –0.3 V to 7 V
HV Pre-Regulator Input Current (continuous) ..... 5 mA[a]
Continuous Output Current (Source or Sink) ..... 125 mA
Storage Temperature ..... –65 to 150°C
Operating Temperature ..... –40 to 85°C
Junction Temperature (T_J) ..... 150°C

Power Dissipation (Package)[b]
16-Pin Plastic DIP (J Suffix)[c] ..... 750 mW
16-Pin SOIC (Y Suffix)[d] ..... 900 mW
Thermal Impedance (Θ_{JA})
16-Pin Plastic DIP ..... 167°C/W
16-Pin SOIC ..... 140°C/W

Notes
a. Continuous current may be limited by the applications maximum input voltage and the package power dissipation.
b. Device mounted with all leads soldered or welded to PC board.
c. Derate 6 mW/°C above 25°C.
d. Derate 7.2 mW/°C above 25°C.

Recommended Operating Range

Voltages Referenced to $-V_{IN}$
V_{CC} ..... 9.5 V to 13.5 V
$+V_{IN}$ ..... 10 V to 450 V
f_{OSC} ..... 40 kHz to 1 MHz
R_{OSC} ..... 25 kΩ to 1 MΩ
Linear Inputs ..... 0 to V_{CC} – 3 V
Digital Inputs ..... 0 to V_{CC}

Specifications[a]

Parameter	Symbol	Test Conditions Unless Specified DISCHARGE = $-V_{IN}$ = 0 V, V_{CC} = 10 V $+V_{IN}$ = 300 V R_{BIAS} = 390 kΩ, R_{OSC} = 330 kΩ	Temp[b]	Limits D Suffix –40 to 85°C Min[c]	Typ[d]	Max[c]	Unit
Reference							
Output Voltage	V_R	OSC IN = – V_{IN} (OSC Disabled) R_L = 10 MΩ	Room Full	3.88 3.82	4.0	4.12 4.14	V
Output Impedance[e]	Z_{OUT}		Room	15	30	45	kΩ
Short Circuit Current	I_{SREF}	V_{REF} = $-V_{IN}$	Room	70	100	130	µA
Temperature Stability[e]	T_{REF}		Full		0.5	1.0	mV/°C
Oscillator							
Maximum Frequency[e]	f_{MAX}	R_{OSC} = 0	Room	1	3		MHz
Initial Accuracy	f_{OSC}	C_{STRAY} Pin 9 ≤ 5 pF R_{OSC} = 330 kΩ	Room	80	100	120	kHz
		C_{STRAY} Pin 9 ≤ 5 pF R_{OSC} = 150 kΩ	Room	160	200	240	
Voltage Stability	$\Delta f/f$	$\Delta f/f$ = f(13.5 V) – f(9.5 V) / f(9.5 V)	Room		10	15	%
Temperature Coefficient[e]	T_{OSC}		Full		200	500	ppm/°C
Error Amplifier							
Feedback Input Voltage	V_{FB}	FB Tied to COMP OSC IN = – V_{IN} (OSC Disabled)	Room	3.92		4.08	V
Input BIAS Current	I_{FB}	OSC IN = – V_{IN}, V_{FB} = 4 V	Room		25	500	nA
Input OFFSET Voltage	V_{OS}	OSC IN = – V_{IN}	Room		± 15	± 40	mV
Open Loop Voltage Gain[e]	A_{VOL}	OSC IN = – V_{IN}	Room	60	80		dB
Unity Gain Bandwidth[e]	BW	OSC IN = – V_{IN}	Room	1.0	1.5		MHz

Specifications[a]

Parameter	Symbol	Test Conditions Unless Specified DISCHARGE = $-V_{IN}$ = 0 V, V_{CC} = 10 V $+V_{IN}$ = 300 V R_{BIAS} = 390 kΩ, R_{OSC} = 330 kΩ	Temp[b]	Limits D Suffix –40 to 85°C Min[c]	Typ[d]	Max[c]	Unit
Error Amplifier (Cont'd)							
Dynamic Output Impedance[e]	Z_{OUT}	Error Amp configured for 60 dB gain	Room		1000	2000	Ω
Output Current	I_{OUT}	Source V_{FB} = 3.4 V	Room		–2.0	–1.4	mA
		Sink V_{FB} = 4.5 V	Room	0.12	0.15		
Power Supply Rejection	PSRR	9.5 V ≤ V_{CC} ≤ 13.5 V	Room	50	70		dB
Current Limit							
Threshold Voltage	V_{SOURCE}	V_{FB} = 0 V	Room	1.0	1.2	1.4	V
Delay to Output[e]	t_d	V_{SENSE} = 1.5 V, See Figure 1	Room		100	150	ns
Pre-Regulator/Start-Up							
Input Voltage	$+V_{IN}$	I_{IN} = 10 µA	Room	450			V
Input Leakage Current	$+I_{IN}$	V_{CC} ≥ 9.4 V	Room			10	µA
V_{CC} Pre-Regulator Turn-Off Threshold Voltage	V_{REG}	$I_{PRE-REGULATOR}$ = 10 µA	Room	7.8	8.6	9.4	V
Undervoltage Lockout	V_{UVLO}		Room	7.0	8.1	8.9	
$V_{REG} - V_{UVLO}$	V_{DELTA}		Room	0.3	0.6		
Supply							
Supply Current	I_{CC}	C_L = 500 pF at Pin 5	Room		0.85	1.5	mA
Bias Current	I_{BIAS}		Room	10	15	20	µA
Logic							
$\overline{\text{SHUTDOWN}}$ Delay[e]	t_{SD}	C_L = 500 pF, $V_{SENSE} = -V_{IN}$ See Figure 2	Room		50	100	ns
$\overline{\text{SHUTDOWN}}$ Pulse Width[e]	t_{SW}	See Figure 3	Room	50			
RESET Pulse Width[e]	t_{RW}		Room	50			
Latching Pulse Width $\overline{\text{SHUTDOWN}}$ and RESET Low[e]	t_{LW}		Room	25			
Input Low Voltage	V_{IL}		Room			2.0	V
Input High Voltage	V_{IH}		Room	8.0			
Input Current Input Voltage High	I_{IH}	V_{IN} = 10 V	Room		1	5	µA
Input Current Input Voltage Low	I_{IL}	V_{IN} = 0 V	Room	–35	–25		
Output							
Output High Voltage	V_{OH}	I_{OUT} = –10 mA	Room Full	9.7 9.5			V
Output Low Voltage	V_{OL}	I_{OUT} = 10 mA	Room Full			0.3 0.5	
Output Resistance	R_{OUT}	I_{OUT} = 10 mA, Source or Sink	Room Full		20 25	30 35	Ω
Rise Time[e]	t_r	C_L = 500 pF	Room		40	75	ns
Fall Time[e]	t_f		Room		40	75	

Notes
a. Refer to PROCESS OPTION FLOWCHART for additional information.
b. Room = 25°C, Cold and Hot = as determined by the operating temperature suffix.
c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
e. Guaranteed by design, not subject to production test.

Timing Waveforms

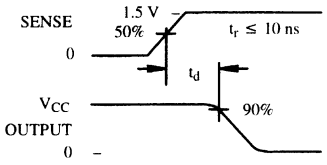


Figure 1.

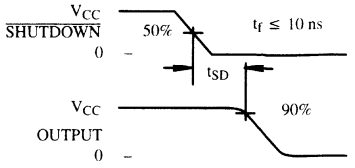


Figure 2.

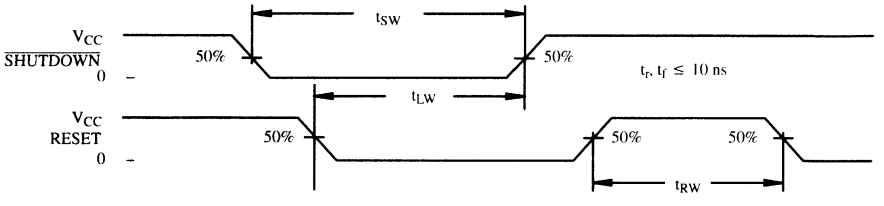
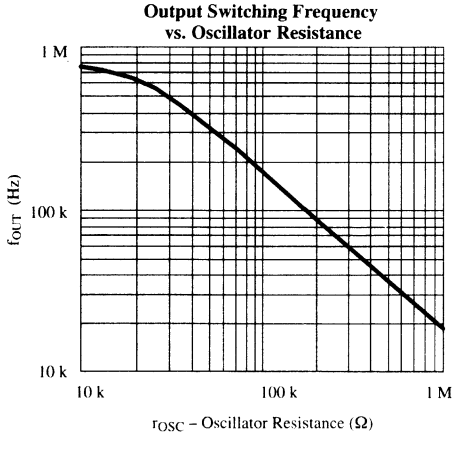


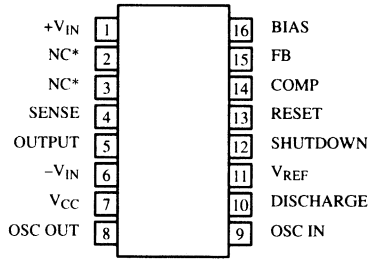
Figure 3.

Typical Characteristics



Pin Configurations

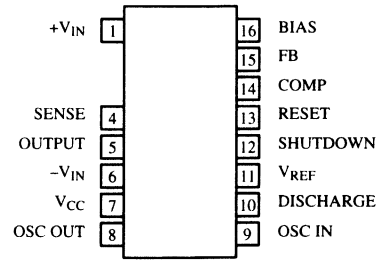
Dual-In-Line



Top View

Order Number: Si9120DJ

SOIC



Top View

Order Number: Si9120DY
Note: Pins 2 and 3 are removed

Detailed Description

Pre-Regulator/Start-Up Section

Due to the low quiescent current requirement of the Si9120 control circuitry, bias power can be supplied from the unregulated input power source, from an external regulated low-voltage supply, or from an auxiliary "bootstrap" winding on the output inductor or transformer.

When power is first applied during start-up, $+V_{IN}$ (pin 1) will draw a constant current. The magnitude of this current is determined by a high-voltage depletion MOSFET which is connected between $+V_{IN}$ and V_{CC} (pin 7). This start-up circuitry provides initial power to the IC by charging an external bypass capacitance connected to the V_{CC} pin. The constant current is disabled when V_{CC} exceeds 8.6 V. If V_{CC} is not forced to exceed the 8.6-V threshold, then V_{CC} will be regulated to a nominal value of 8.6 V by the pre-regulator circuit.

As the supply voltage rises toward the normal operating conditions, an internal undervoltage (UV) lockout circuit keeps the output driver disabled until V_{CC} exceeds the undervoltage lockout threshold (typically 8.1 V). This guarantees that the control logic will be functioning properly and that sufficient gate drive voltage is available before the MOSFET turns on. The design of the IC is such that the undervoltage lockout threshold will be at least 300 mV less than the pre-regulator turn-off voltage. Power dissipation can be minimized by providing an external power source to V_{CC} such that the constant current source is always disabled.

Note: When driving large MOSFETs at high frequency without a bootstrap V_{CC} supply, power dissipation in the pre-regulator may exceed the power rating of the IC package.

BIAS

To properly set the bias for the Si9120, a 390-kΩ resistor should be tied from BIAS (pin 16) to $-V_{IN}$ (pin 6). This determines the magnitude of bias current in all of the analog sections and the pull-up current for the $\overline{\text{SHUTDOWN}}$ and RESET pins. The current flowing in the bias resistor is nominally 15 µA.

Reference Section

The reference section of the Si9120 consists of a temperature compensated buried zener and trimmable divider network. The output of the reference section is connected internally to the non-inverting input of the error amplifier. Nominal reference output voltage is 4 V. The trimming procedure that is used on the Si9120 brings the output of the error amplifier (which is configured for unity gain during trimming) to within ±2% of 4 V. This compensates for input offset voltage in the error amplifier.

The output impedance of the reference section has been purposely made high so that a low impedance external voltage source can be used to override the internal voltage source, if desired, without otherwise altering the performance of the device.

Detailed Description (Cont'd)

Error Amplifier

Closed-loop regulation is provided by the error amplifier, which is intended for use with "around-the-amplifier" compensation. A MOS differential input stage provides for high input impedance. The noninverting input to the error amplifier (V_{REF}) is internally connected to the output of the reference supply and should be bypassed with a small capacitor to ground.

Oscillator Section

The oscillator consists of a ring of CMOS inverters, capacitors, and a capacitor discharge switch. Frequency is set by an external resistor between the OSC IN and OSC OUT pins. (See Typical Characteristics for details of resistor value vs. frequency.) The DISCHARGE pin should be tied to $-V_{IN}$ for normal internal oscillator operation. A frequency divider in the logic section limits switch duty cycle to $\leq$ 50% by locking the switching frequency to one half of the oscillator frequency.

$\overline{\text{SHUTDOWN}}$ and RESET

$\overline{\text{SHUTDOWN}}$ (pin 12) and RESET (pin 13) are intended for overriding the output MOSFET switch via external control logic. The two inputs are fed through a latch preceding the output switch. Depending on the logic state of RESET. $\overline{\text{SHUTDOWN}}$ can be either a latched or unlatched input. The output is off whenever $\overline{\text{SHUTDOWN}}$ is low. By simultaneously having $\overline{\text{SHUTDOWN}}$ and RESET low, the latch is set and $\overline{\text{SHUTDOWN}}$ has no effect until RESET goes high. See Table 1.

Both pins have internal current source pull-ups and should be left disconnected when not in use. An added feature of the current sources is the ability to connect a capacitor and an open-collector driver to the $\overline{\text{SHUTDOWN}}$ or RESET pins to provide variable shutdown time.

Table 1: Truth Table for the $\overline{\text{SHUTDOWN}}$ and RESET Pins

$\overline{\text{SHUTDOWN}}$	RESET	OUTPUT
H	H	Normal Operation
H	⌐‾	Normal Operation (No Change)
L	H	Off (Not Latched)
L	L	Off (Latched)
_⌐	L	Off (Latched—No Change)

Output Driver

The push-pull driver output has a typical on-resistance of 20 Ω. maximum switching times are specified at 75 ns for a 500-pF load. This is sufficient to directly drive MOSFETs such as the IRF820, BUZ78 or BUZ80. Larger devices can be driven, but switching times will be longer, resulting in higher switching losses.

For applications information refer to AN707 (FaxBack #8707) and AN708 (FaxBack #8708).

Designing Low-Power Off-Line Flyback Converters Using the Si9120 Switchmode Controller IC

by Craig Varga

Getting high efficiency from low-power off-line power supplies has always posed difficulties for the design engineer. Power hungry control circuits require either line frequency transformers for bias or bleeder circuits for start-up. The problem with the bleeder approach is that, to date, no provisions have been made in PWM ICs to turn off the bleeder; so several watts of power get consumed during normal operation — serving no purpose but to heat the bleed resistor. While solutions are available, they all require additional parts, which increase costs and use precious circuit board real estate.

The Si9120 from Siliconix was designed to address these problems. This current-mode control, pulse-width modulator IC is implemented with combined BiC/DMOS technology. All logic functions are implemented in CMOS to reduce the typical quiescent power requirements to 0.85 mA while driving a 500-pF load at 50 kHz. Included on chip is a 450-V DMOS, depletion-mode transistor configured as a linear voltage regulator to supply operating power to the chip directly from the rectified 115-V mains. The chip contains MOS capacitors for the clock circuit, so the only external timing component required is a resistor to set the operating frequency. Other features include a temperature-compensated buried Zener reference for less than 0.2 mV/°C drift; a latchable shutdown feature; and a dual current-limit comparator, which minimizes false tripping due to leading-edge current spikes. A major advantage of CMOS processing is speed—current-limit delays are typically under 100 ns while supply current is kept at less than 1 mA. This allows reliable operation up to 500 kHz.

Functional Description

Pre-regulator

A BiC/DMOS power integrated circuit process is used to integrate a high-voltage (450-V rated) lateral DMOS transistor with the CMOS PWM controller. By using an ion implant to shift the gate threshold to a negative value, as shown in Figure 1, the transistor is made to operate as a depletion-mode device. This eliminates the need for a pull-up voltage above V_{CC} to turn the device on, and an amplifier and voltage reference can be used to implement a linear regulator, as shown in Figure 2. The CMOS circuitry is thus protected from transients which appear on the input power bus.

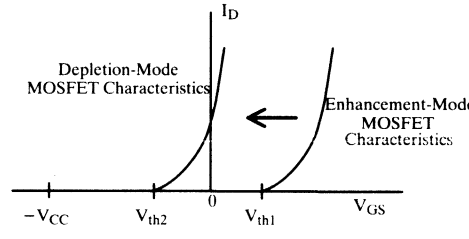


Figure 1. Depletion-mode MOSFET Characteristics

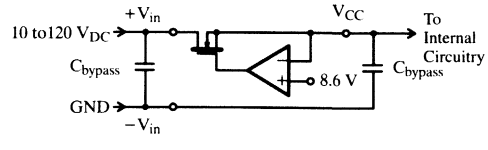


Figure 2. Pre-regulator/Start-up Circuit

For some applications it is useful to turn off the pre-regulator after start-up. This is easily accomplished by using an auxiliary winding on the transformer to develop a bootstrap supply voltage. After the converter starts, its own output feeds 10 to 12 V to pin 7 (V_{CC}), and the amplifier pulls the gate of the MOSFET to the $-V_{in}$ rail. Thus, $V_{GS} = -V_{CC}$, and the device is turned off.

Updates to this app note may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70580.

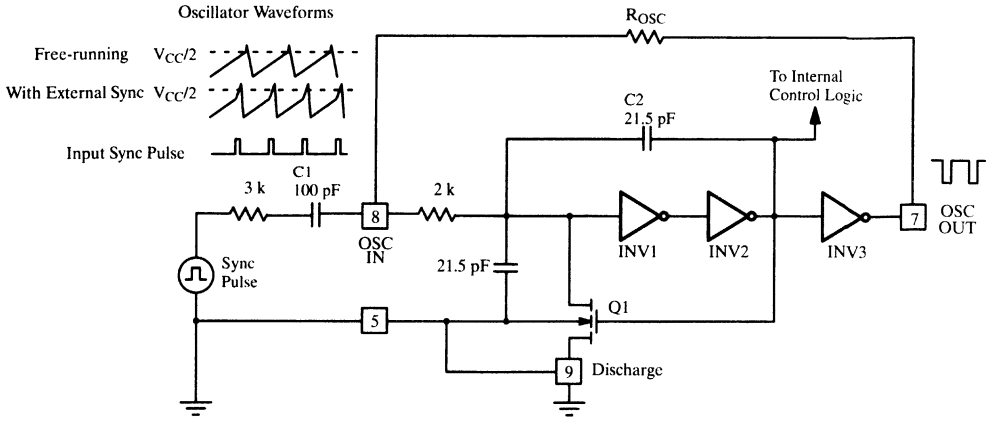


Figure 3. Si9120 Oscillator Circuit Operation

Oscillator

A ring of inverters and internal MOS capacitors form the oscillator circuit, as shown in Figure 3. This circuit requires only a resistor (no external capacitor) to program the frequency. The internal capacitance is charged towards V_{CC} through R_{OSC}. When the capacitor voltage reaches $V_{CC}/2$ (the CMOS logic threshold), inverter INV1 changes state (from high to low), and the INV2 output goes from a low to a high output. The capacitor, C2, provides positive feedback to ensure stable operation without frequency jitter.

It also causes the "bump" at the end of the ramp until INV2 can turn on the discharge switch, Q1, to terminate the cycle.

Oscillator synchronization is achieved by prematurely terminating each clock cycle using a positive going pulse capacitively coupled onto the oscillator ramp voltage. The pulse forces INV1 to change states, Q1 discharges C = C1 + C2, and the cycle repeats. An internal flip-flop blanks out the output during every other clock cycle, so the switch duty ratio is limited to a maximum of 50%. Therefore, the oscillator frequency and SYNC pulse repetition rate must be set at two times the switching frequency, f_s.

Error Amplifier

The bias resistor, connected from pin 16 (bias) to pin 6 ($-V_{in}$), programs the current sources in the analog portion of the current-mode controller — including the error amplifier, the current-mode and current-limit comparators, and the voltage reference. The Si9120 data sheet guarantees the performance of these functions at one value of bias current—15 µA. It is possible to change the performance characteristics of these functions by changing the bias current. (See Siliconix Application Note AN703 for an explanation of how this is accomplished.)

The error amplifier circuit employs PMOS transistors in a differential input stage to achieve a high input impedance of 40 MΩ typically (2-MΩ minimum). This input impedance, combined with a 1-kΩ small-signal output impedance, enables the amplifier to be used with feedback compensation, unlike transconductance error amplifiers. The amplifier can source 2 mA and sink 0.140 mA, as can be seen from the output stage equivalent circuit in Figure 4. Yes, an NPN transistor is used here. Most of the PWM controller is CMOS, but the process allows the flexibility of using bipolar devices where they are advantageous.

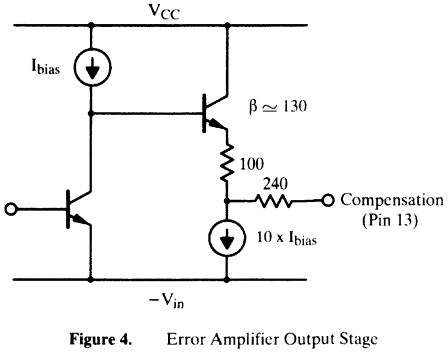


Figure 4. Error Amplifier Output Stage

The error amplifier is unity gain stable with a typical bandwidth of 1.4 MHz and 70° phase margin. Bias current values from 5 µA to 50 µA have been tested, and the error amplifier does remain stable over this range. Actually, the bandwidth and phase margin increase somewhat as I_{bias} is increased above 15 µA. Higher bias currents may, therefore, be useful when compensating higher frequency converters (above 250 kHz).

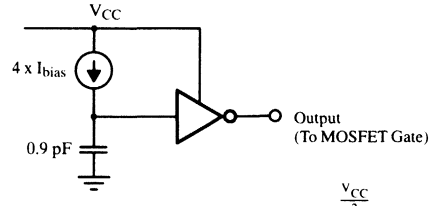
Voltage Reference

A buried Zener with merged temperature compensating diode (Patent no. 4766469) is used to achieve stability of 0.2 mV/°C.

The Si9120 voltage reference is trimmed to 4 V plus or minus 2% with a bias current of 15 µA. Note that trimming is done with the error amplifier connected for unity gain, so the effect of the offset voltage is removed. The reference voltage varies by about 1% as I_{bias} is varied from 5 to 50 µA. If 2% reference accuracy must be guaranteed, I_{bias} should be set at 15 µA.

Comparators

The delay time of the current-limit and current-mode comparators can be modeled as a current source charging an internal nodal capacitance, as shown in Figure 5. The current-mode comparator is intentionally made to be four times slower than the current-limit comparator. In many circuits, this permits the elimination of the RC filter in the current-sense circuit, which is used to prevent false trips by the leading edge current spike. After one of the comparator outputs goes high, there is an additional 20 ns of gate propagation delay before the output driver can begin switching. The total current-limit delay to output versus I_{bias} is shown in Figure 6 for V_{CC} equal to 8.5 V. The delay time is 180 ns for I_{bias} = 5 µA, but decreases to 50 ns for I_{bias} = 30 µA. As operating frequency is increased, I_{bias} may be increased to speed up the current limiting and reduce the minimum MOSFET pulse width. As I_{bias} is increased, however, the current-limit trip voltage also increases. Figure 7 shows how the trip voltage is established and how it varies with I_{bias}. The current sense resistor and I_{bias} determine the peak value of switch current. Since this current limiting is very fast, the trip level of current is usually set to be well above the maximum normal operating current (by a factor of 1.5 to 2). This prevents false trips but still protects the MOSFET switch from exceeding its pulse current ratings.



$$t_D \simeq 20\ ns + C_{node} \frac{\frac{V_{CC}}{2}}{(4xI_{bias})}$$

$$= 20\ ns + 0.9\ pF\ \frac{4.25\ V}{(4xI_{bias})}$$

Figure 5. Current-limit Comparator Delay (Equivalent Circuit Model)

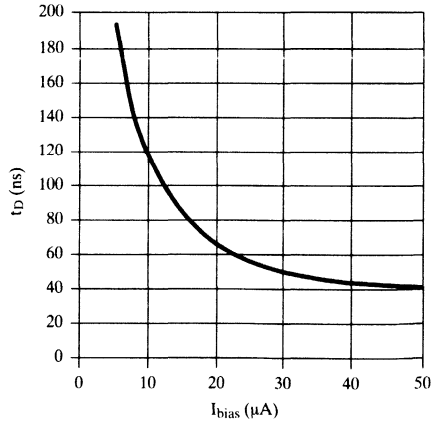
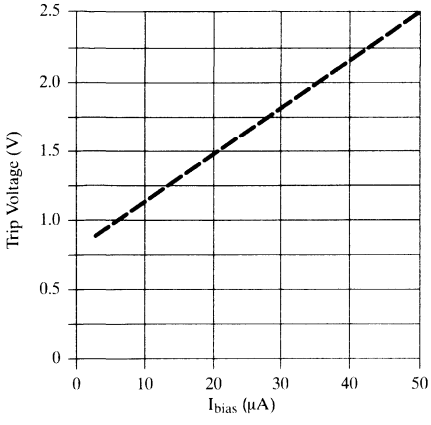


Figure 6. Current-limit Comparator Delay vs. Bias Current



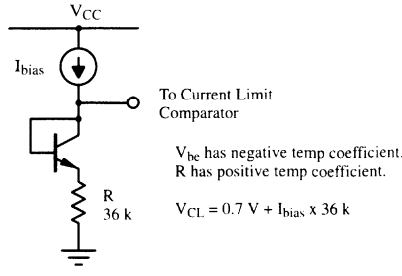


Figure 7. Current-Limit Trip Voltage vs. Programmed Bias Current

MOSFET Driver

The driver circuit is a CMOS inverter whose typical characteristics are shown in Figure 8. The n-channel (turn-off) peak drive current is about 20% higher than that of the p-channel (turn-on) device. Although the on-resistance ($r_{DS(on)}$) of the output drive is specified, usually the saturation current (where $\Delta I_D/\Delta V_{DS}$ is very small) determines the switching speed. This is due to the vertical load line of capacitive loads. In other words, the MOSFET gate capacitance appears as a short circuit across the driver's output.

The CMOS driver is fast enough to effectively eliminate cross-conduction current during switching transitions, at least when $V_{CC} \leq 10$ V. Above this level, a small amount of cross conduction occurs. Therefore, the greatest gate drive efficiency (approaching 100%) is achieved by keeping $V_{CC} \leq 10$ V, and the gate drive power is given by

$$P_{gate} = Q_g \times f_s \times V_{CC}$$

where

Q_g = MOSFET gate charge
f_s = switching frequency
V_{CC} = supply voltage

Shutdown Logic

The shutdown logic employs an RS flip-flop to disable the output drive. Both the SHUTDOWN and RESET inputs have internal current-source pull-ups (equal to I_{bias}), so they can be left open when unused. As long as the SHUTDOWN input is held low, the output is OFF. If the RESET input is hard wired to $-V_{in}$ (through a normally closed reset button if desired), any LOW input to SHUTDOWN will latch the output in the "off" state. It will remain off until power is recycled (or the reset button is pushed).

Undervoltage Lockout

During start-up, the depletion transistor charges the capacitance connected to the V_{CC} pin with a typical charging current of 15 to 20 mA. The output is disabled until V_{CC} reaches the undervoltage (UV) lockout voltage (typically 8.1 V). The IC requires less than 0.5 mA of current during this time, since the largest component of supply current is usually for the gate drive. When V_{CC} reaches 8.1 V, the output is enabled and the MOSFET begins switching. The supply current increases by $Q_g \times f_s$, and V_{CC} charges more slowly until it reaches the pre-regulator voltage (8.6 V).

If too much current is drawn from V_{CC} (for instance, to supply other circuitry), it is possible that the converter will be prevented from starting. Or it may oscillate on and off as it starts up, loads down the V_{CC} pin, shuts off, and then repeats this cycle. Consult the factory if a minimum pre-regulator current specification above 5 mA must be guaranteed.

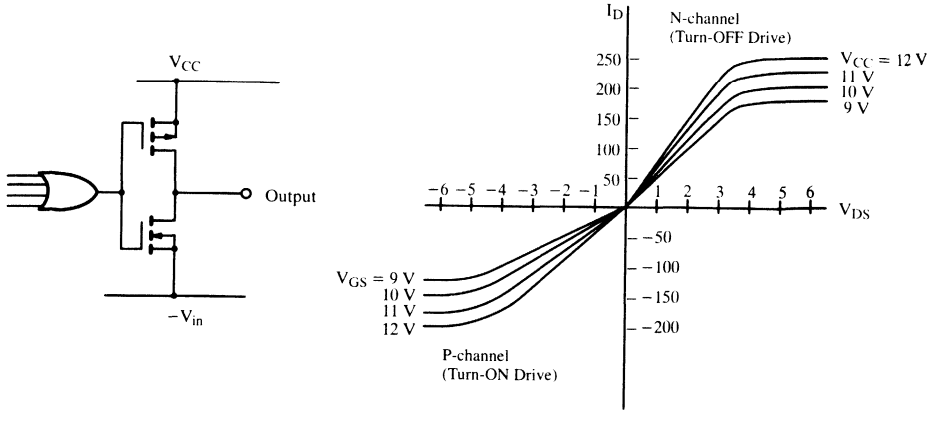


Figure 8. Output Drive Characteristics

Flyback Converter Example

To illustrate the design procedure for a low-power off-line SMPS, a typical example should be presented. But what is a "typical" 5- to 10-W supply requirement? Should the output be a single +5 V or +12 V, or should a dual output, ± 5 V or ± 12 V, be used? How about +5 V and ± 12 V? There is no typical requirement, so a multiple-output design was chosen since cross regulation requirements make this the more difficult problem. The specifications for a 5-W supply with four outputs is given below.

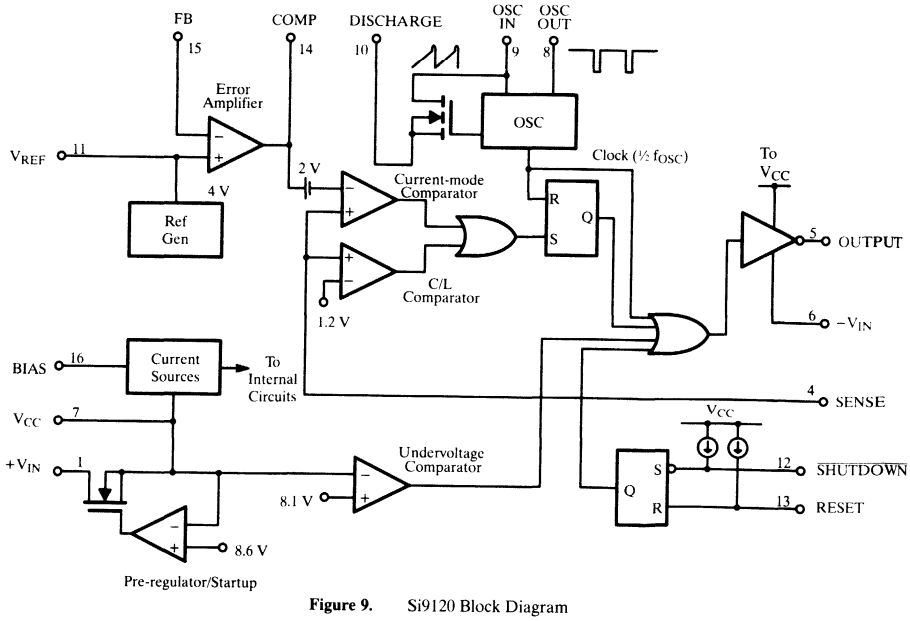


Figure 9. Si9120 Block Diagram

Specifications

Input Voltage 90 to 130 V ac, 50 to 60 Hz

Output Voltage (V)	Min. Load (mA)	Max. Load (mA)	Regulation (%)	Ripple (mV p-p)
+30	1	4	±5	200
+12	80	340	±5	200
$+5_{(Main)}$	25	110	±5	50
$+5_{(Aux)}$	20	80	±5	15

Efficiency >80% Minimum
Switching Frequency 32 kHz

Circuit Description

The flyback converter circuit, shown in Figure 10, was designed for minimum cost and parts count. Since the regulation requirements are fairly loose, it is advantageous to eliminate feedback from primary to secondary. Output voltage is controlled indirectly by regulating a bootstrap auxiliary winding on the primary side. (Strictly speaking, the auxiliary winding is not required, as the chip will run directly from line power; but another feedback scheme would obviously be necessary.) All outputs are isolated from one another. Also, the primary-to-secondary isolation is designed to meet VDE safety requirements.

The power switching transistor (Q1) is an IRF820 rated at 500 V and 2.5 A. On-resistance is specified at 3 Ω. While this device may appear to be overkill for a 5 W output, it is the smallest 500 V die available, and it allows operation without a heatsink.

The flyback inductor (T1) is designed to operate in the discontinuous conduction mode. This makes loop compensation simple since there is no right half plane zero in DCM flyback converters. Also, since the power level is so low, the higher peak currents associated with this mode of operation pose no significant problems. The Si9120 provides all necessary control functions with only a handful of passive components.

Flyback Fundamentals

The flyback circuit works by storing energy in the flyback inductor during the switch's on-time and releasing this energy to the secondary circuits during the switch's off-period. The power transformer, in the case of a flyback converter, is not a transformer at all. Transformers work by coupling energy from primary to secondary, storing as little energy as possible. The flyback, however, stores all the energy for one cycle of operation in what is properly an inductor.

It is widely believed that current in an inductor cannot be changed instantaneously. This is not quite true. Ampere-turns are what cannot change instantaneously. If you could somehow change the turns, you could change the current on demand. This is what happens in the flyback inductor. During the switch-on time, some number of ampere-turns are developed in the primary winding. The power switch is then turned off in essentially zero time, forcing the ampere-turns to appear at the secondary windings. Thus, turns have changed, and amperes scale accordingly. Autotransformer action between the various windings forces the output voltages to track in proportion to the turn ratios of the windings. This forces the output capacitors to peak charge to the respective winding voltages and, thereby, provides regulation between windings. The better the coupling between windings, the better the cross regulation. Hence, all four outputs are wound closely together with no additional insulation between windings. By controlling the peak current through the primary winding during the on-time, the total energy per cycle, hence the total throughput power, can be controlled. By making this current a function of the output voltage error, voltage regulation is achieved.

On initial application of power to the supply, the high-voltage DMOS transistor in the Si9120 begins to charge the V_{CC} supply capacitor, C7. When approximately 8.1 V appears on the bias supply, the Si9120 undervoltage lockout enables the output driver. All internal bias voltages are stable at this point, and clean operation is assured. When V_{CC} reaches 8.6 V, the DMOS linear regulator reduces the charging current to maintain this voltage. Within a few cycles of operation, the bootstrap winding raises V_{CC} beyond the point at which the linear regulator tries to hold the bias supply. The DMOS transistor is forced to cut off. Now the V_{CC} supply is totally independent of the power line and draws no current from it.

A cycle is initiated by the Si9120 clock toggling the output driver on. The driver turns on power switch Q1, causing current to begin ramping up linearly in T1's primary winding. The current is sensed by R7 and filtered by R6 and C6. When the Si9120's current-sense comparator detects that the primary current has reached the control loop's programmed level, the power switch is shut off and energy stored in T1 begins to discharge into the secondary circuits.

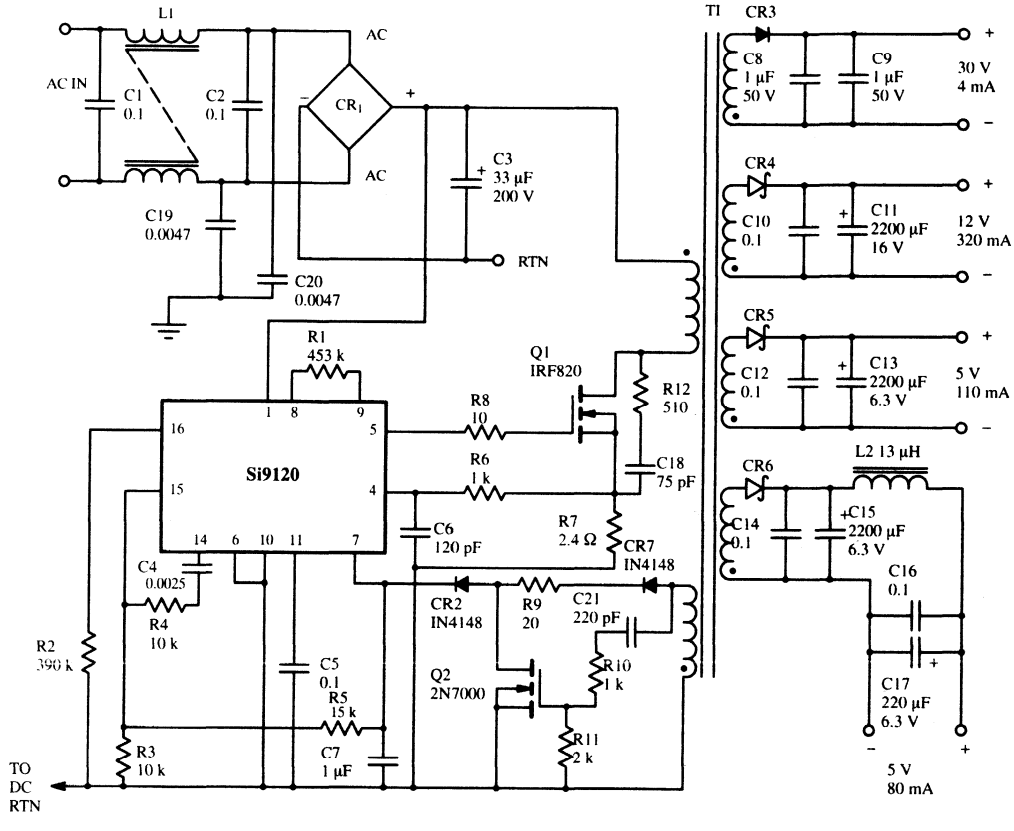


Figure 10. 5-W Offline Flyback Converter

To close the regulator loop, the voltage of the V_{CC} supply winding on the primary side is sensed and compared to a reference. The difference is multiplied by a high-gain amplifier. These functions are all performed by the Si9120. R3 and R5 divide the bias voltage down to the 4 V reference level. R4 and C4 provide for loop compensation, and C7 filters V_{CC}.

A major problem exists in any converter with a large input-to-output isolation voltage -- leakage inductance of the flyback inductor. A portion of the energy stored in this inductance will appear as a voltage spike on the feedback winding. The V_{CC} supply tends to charge to the peak of the spike, forcing the control loop to regulate all of the output voltages substantially below the desired values.

Spike suppression and proper operation of the regulator loop are provided by a blanking circuit (consisting of R9, R10, R11, C21, CR7, and Q2). At the instant Q1 turns off, a positive-going voltage appears at the anode of CR7. C21 forms a differentiator with R10 and R11 that produces a positive voltage on the gate of Q2. This turns on Q2 and clamps the anode of CR2 to ground, back-biasing CR2 and preventing the spike from passing through to the V_{CC} supply. A substantial portion of the energy contained in the voltage spike is shunted to ground through CR7 and R9 (the circuit is behaving, to some degree, like an active snubber). When the spike energy has been dissipated, the voltage drops to the nominal level. R11 then pulls Q2's gate voltage back down, turning off Q2 and allowing the remainder of the pulse to pass through to the V_{CC} supply. Figure 11 shows details of the blanking circuit in operation.

Figures 12-15 show details of the power supply operation. The input voltage for all photos was 115 V RMS and all loads are at maximum. Table 1 gives the line and load regulation of the circuit along with output ripple and efficiency data. At 85% efficiency, absolutely no heatsinks are required.

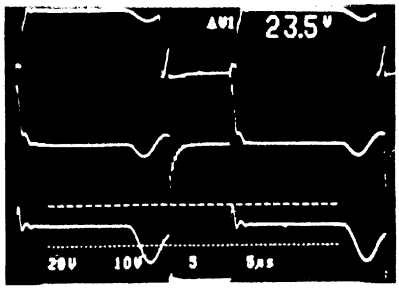


Figure 11. Top Trace – Anode of CR2
Center Trace – Gate of Q2
Bottom Trace – Anode of CR7
Note spike amplitude of 23.5 V.

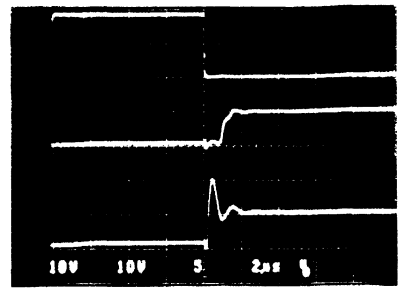


Figure 12. Top Trace – Gate Drive Q1
Center Trace – Anode of CR2
Bottom Trace – Cathode of CR7

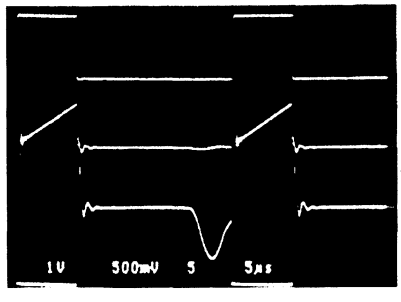


Figure 13. Top Trace – Gate Drive Q1
Center Trace – Voltage Across R7
Bottom Trace – Drain Voltage of Q1 (100 V/div)

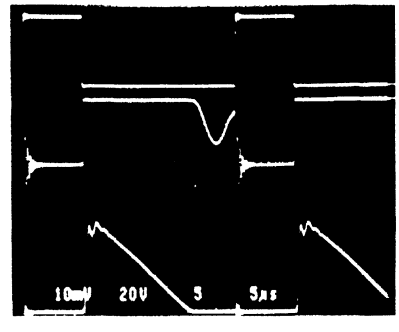


Figure 14. Top Trace – Gate Drive Q1
Center Trace – Anode of CR4
Bottom Trace – CR4 Current (500 mA/div)

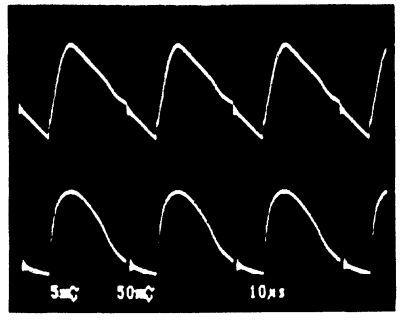


Figure 15. Top Trace – 30-V Output Ripple
Bottom Trace – 5-V, 80-mA Ripple

Table I: 5-W Off-Line Flyback Test Data

AC Input (V RMS)	12 V	30 V	$5_{(Main)}$ V	$5_{(Aux)}$ V
Full Load Outputs (V)				
80	11.00	28.50	5.019	5.058
100	11.05	28.60	5.046	5.080
115	11.08	28.70	5.060	5.095
130	11.11	28.77	5.072	5.111
Half Load Outputs (V)				
80	11.26	29.10	5.170	5.214
100	11.32	29.16	5.180	5.223
115	11.33	29.19	5.186	5.230
130	11.34	29.92	5.190	5.234
Half Load Outputs (V)				
80	11.26	29.10	5.170	5.214
100	11.32	29.16	5.180	5.223
115	11.33	29.19	5.186	5.230
130	11.34	29.92	5.190	5.234
Output Ripple (mV Pk–Pk)				
	90	125	23	12

Actual measured outputs tabulated at various line and load conditions ($5_{(Main)}$ = 5 V, 110 mA, $5_{(Aux)}$ = 5 V, 80 mA)
Full Load Drop Out Voltage = 64-V RMS
Efficiency = (P_{out}/P_{in}) 100% = (4.98/5.86) 100 = 85%

Circuit Design Details

Selecting the Input Capacitor

For a 90-V ac input, the bus voltage is

$$90\sqrt{2} = 127 \text{ V dc}$$

If 20 V of ripple is allowed, the lowest input voltage is 107 V dc. For some margin, use 100 V dc. For a 5-W output with 80% efficiency, $\eta = 0.8$;

$$P_{in} = P_{out}/\eta = 5/0.8 = 6.25 \text{ W}$$
$$I_{in} = P_{in}/V_{in} = 6.25/100 = 62.5 \text{ mA}$$

Input ripple is assumed to be 20 V_{p-p}. The low frequency limit is 50 Hz; thus, the ripple frequency is 100 Hz.

$$C = I \times \Delta T/\Delta V = (0.0625)(0.01)/20$$
$$= 31.25 \text{ µF}$$

33 µF is a standard value.

Finding the Peak Switch Current

At 100 V dc in, the maximum duty factor D = 45%.

$$I_{pk} = 2 \times I_{avg}/D_{max}$$
$$= 2 (0.0625)/0.45$$
$$= 0.28 \text{ A}$$

The RMS switch current is

$$I_{RMS} = I_{pk}\sqrt{\frac{D}{3}} = 0.28 \quad 0.45\sqrt{3} = 0.11 \text{ A}$$

Switch Voltage Rating and Temperature Rise

The transformer primary voltage during the off-time will be independent of input line voltage but must be equal to or greater than the dc input voltage at low line. The maximum switch off-voltage equals the dc input at high line plus the transformer off-voltage. If the transformer off-voltage is assumed to be 125 V (the peak of the rectified sine wave at low line), then

$$V_{off(max)} = V_{in(max)} + 125 \text{ V} = 130\sqrt{2} + 125 = 308 \text{ V}$$

Allowing approximately 100 V for the leakage inductance spike, $V_{DS(max)} \leq 408$ V. A 500-V FET gives a good safety margin. The IRF820 is rated 500 V, 3 Ω. For $T_J = 100°C$, the $r_{DS(on)}$ scale factor = 1.6, so the worst case on-resistance is

$$r_{DS(on)} = 3\ \Omega\ (1.6) = 4.8\ \Omega$$

Conduction loss is

$$(0.11\ A)^2\ (4.8\ \Omega) = 0.058\ W$$

Assuming switching losses are equal to conduction losses, total dissipation in the FET equals 0.116 W. With no heatsink,

$$\Delta T_J = (R_{\Theta JA})\ (P_{DISS}) = (80°C/W)\ (0.155\ W) = 9.3°C$$

Primary Inductance

Operating frequency was selected at approximately 32 kHz to permit synchronization to a television horizontal scan if needed. Period $T_S = 31.25\ \mu s$, so

$$t_{on(max)} = (0.45)\ (31.25) = 14\ \mu s$$

I_{pk} was calculated at 0.28 A and is also invariant with line voltage. At low line,

$$V_{in(min)} = 100\ V \text{ and}$$

$$L_P = \frac{V\Delta t}{\Delta I} = \frac{100(14\mu s)}{0.28} = 5\ mH$$

where

L_P = Primary Inductance
$\Delta t = t_{on(max)}$
$\Delta I = I_{pk}$

Flyback Inductor Design

Using the area product method,

$$A_cA_e = \frac{(25.32\ L_PI_{pk}D^2)\ 10^8}{B_{max}} \qquad \text{(REF-2)}$$

where

D = wire diameter in inches
B_{max} = maximum flux swing in gauss
A_c = core cross sectional area in cm^2
A_e = effective window are in cm^2
A_cA_e = core-window area product in cm^4

Assuming 400 cir/mil/A and 0.11 A RMS, #32 AWG is adequate. Use #31 for cool operation; the diameter of #31 AWG is 0.0108 inches. Allow B_{max} = 2000 gauss.

$$A_cA_e = \frac{(25.32)(5\ mH)(0.28\ A)(0.0108)^2\ (10^8)}{2000}$$

$$= 0.207\ cm^4$$

PQ 42020 size core has $A_cA_e = 0.238\ cm^4$, so it should handle the power.

Find the air gap, l_g, as:

$$l_g = \frac{1.26\ L_PI^2\ pk\ x\ 10^8}{A_cB^2_{max}} = \frac{(1.26)(5.0\ E\text{-}3)(0.28)^2(10)^8}{(0.58)\ (2000)^2}$$

$$= 0.213\ cm$$
$$= 8.4\ mils$$

8 mils is a standard air gap.

Calculate primary turns, N_P. For the chosen core with an 8 mil air gap, the inductance factor, A_L = 363 mH/1000 turns.

$$N_P = 1000\sqrt{\frac{L_P}{A_L}}$$

$$N_P = 1000\sqrt{\frac{5.0}{363}} = 117\ turns$$

Solve for secondary turns, N_S. Based on the feedback winding,

$$N_S = N_P\frac{(V_O + V_f)\ (1 - D_{max})}{V_{in(min)}\ D_{max}} \qquad \text{[See REF. 2]}$$

$$= \frac{(117)\ (10.0 + 0.7)\ (1 - 0.45)}{(100\ V)\ (0.45)} = 15.3\ turns$$

where

V_f = diode forward voltage
V_O = output voltage
D_{max} = maximum duty factor
$V_{in(min)}$ = dc bus voltage at low line

Use 15 turns. This must be less than or equal to the calculated number of turns to ensure current resetting to zero during the off time.

Scaling voltages for other outputs:

$$10.7 \text{ V}/15 \text{ turns} = 0.7133 \text{ V/turn}$$

For all outputs:

$$V_{pk} = V_O + V_f$$

where V_{pk} is transformer secondary voltage.

$$N_S = V_{pk}/0.7133 \text{ V/turn}$$

After calculating all turn numbers and scaling slightly to optimize output voltage balances, the following turns resulted:

+30 V	43 turns
+12 V	17 turns
+5 V	8 turns
10 V bias	15 turns

Choose Wire Sizes. Core window area $A_c = 0.384 \text{ cm}^2$. Allowing about a 50% fill factor results in a winding area of

$$0.5\ (0.384) = 0.192 \text{ cm}^2$$

#31 AWG was assumed for primary. The wire chart lists 1072 turns/cm^2 for #31 AWG.

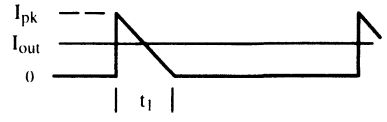
$117/1072 = 0.1091 \text{ cm}^2$
$0.192 - 0.1091 = 0.083 \text{ cm}^2$ left for secondaries

Scaling for the percentage of power output and allotting window area accordingly, the following wire gauges result:

30 V, #40 AWG. (This is about the smallest wire gauge one would use for reliable design and ease of manufacture.)
12 V, #25 AWG
5 V, #31 AWG both outputs
Feedback, #40 AWG for same reasons as +30 V output

Calculating Output Currents

To determine the peak and RMS output currents, the following equations apply:



Output Current Waveform

$$t_1 = \left(\frac{2\ (I_{out})\ A_L}{f(V_{OUT} + V_f)(10^9)}\right)^{\frac{1}{2}}$$

$$I_{pk} = \frac{2(I_{out})}{t_1 f}$$

$$I_{RMS} = \sqrt{\frac{t_1 f}{3}}$$

Where:

t_1 = current decay time
I_{out} = average load current
A_L = core inductance constant in mH/1000 turns
I_{pk} = peak secondary current
f = operating frequency

Results are as follows:

	I_{pk} (A)	t_1 (µs)	I_{RMS} (A)
12 V	1.60	12.85	0.59
30 V	0.11	2.34	0.017
$5_{(Aux)}$ V	1.08	4.60	0.24
$5_{(Main)}$ V	1.28	5.39	0.31
10 V bias	0.16	1.2	1.8

Selecting Output Diodes and Capacitors

Armed with the above data, selection of diode current ratings is possible using the RMS currents calculated. Also, the output capacitors can be sized based on the peak currents. The peak-to-peak ripple will be approximately equal to $(I_{pk})(ESR)$. On the 5 V, 80 mA output, due to a very low ripple specification, a two stage filter to minimize capacitor size was easiest to use. The inductor is a small ferrite core with a few turns of wire. The 30-V output needs only a couple of microfarads of capacitance if ESR = 0. A 2-µF ceramic capacitor fills the bill.

The timing resistor was initially selected at 500 kΩ (from the graph on the Si9120 data sheet) and was optimized empirically at 453 kΩ. Be sure to measure operating frequency on pin 5, as the scope probe capacitance on pin 9 will substantially alter the operating frequency.

Calculating the Primary Current Sense Resistor Value

The minimum current limit threshold is specified at 1 V. The calculated peak primary current is 0.28 A. Allowing approximately 25% over current,

$$I_{pk} = (0.28)(1.25) = 0.35\ A$$
$$R_{cs} = E_s/I_{pk} = 1.0/0.35 = 2.86\ \Omega$$

2.7 Ω is the nearest standard value. R6 and C6 set a 120 ns time constant on the current sense to filter noise spikes.

The blanking circuit differentiator time constant was selected at approximately 0.5 µs. R10 and R11 reduce the gate voltage amplitude to an acceptable level. R3 and R5 divide the feedback voltage down to 4.00 V. R5 was made adjustable for test purposes, and should be approximately 15 kΩ.

Loop Compensation

A frequently asked question is "How can I close the loop without a $40K analyzer?" Well, a number of techniques exist — some tedious, others not quite as bad. The most reliable approach is to apply a pulsed load to the output and empirically adjust the RC compensation for a well-damped exponential output-voltage recovery. With a little practice, this can be done expeditiously. It also has the advantage of showing any problems which may arise when one or more circuit elements are driven non-linear, as can occur during a large transient. This information is missing in a small-signal response plot. Be aware, however, that a load-pulse test lacks the quantitative information of a good Bode plot and fails to permit an accurate assessment of design margins. But with a little hands-on experience, it will be easy to get a good feel for when it's right.

Proceed as follows: Set C4 to approximately 0.1 µF. This sets the error amplifier to unity gain at approximately 100 Hz (Xc = R5 @ 100 Hz). Set R4 to zero. Set up the circuit shown in Figure 16. This allows a load step to be applied to the highest power output. If a bootstrap winding is not used for feedback, apply the step load to the regulated output. The amplitude of the step should be 25% to 50% of the full load current. The repetition rate should be low, around 100 Hz. Monitor the voltage on the V_{CC} pin of the Si9120, as this is controlled by the feedback loop, and watch the recovery characteristics. Gradually increase R4 and decrease C4 to obtain a good response.

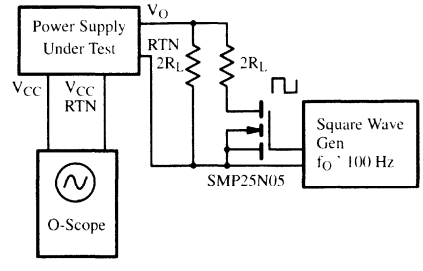


Figure 16. Pulse Load Test Setup

Figure 17 shows the step response to several combinations of RC compensation. A small capacitor across R5 will also speed up the response, but may not be required. In addition, it may be desirable to add a small (100 to 1000 pF) capacitor directly across pins 14 and 15 of the Si9120 to roll off the error amplifier's high frequency gain. Be sure to repeat the above procedure for low and high input line voltages. When the response looks like line D in Figure 17, you're done.

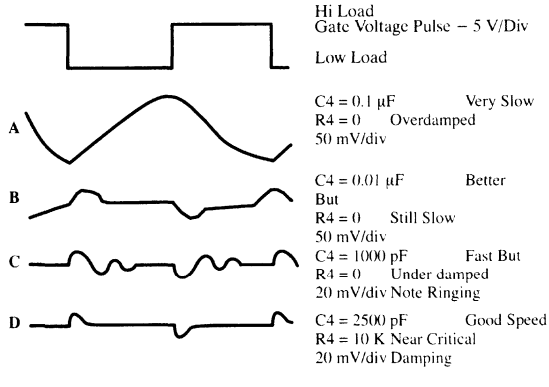


Figure 17. Step Response to Combinations of RC Compensation

Conclusion

Using the Si9120, the design of low-power, high-efficiency, switching power supplies for off-line applications becomes straightforward. By running a DCM flyback topology under current-mode control, a reliable, easily compensated design is achieved. The leakage inductance spike-blanking circuit presented here makes for a well-regulated supply while allowing VDE voltage-isolation requirements to be met.

Flyback Converter Parts List

C1, C2	0.01 µF, 250 V ac, class X2
C3	33 µF, 200 V United Chemicon SL200VB33RU16X31LL
C4	2500 pF, 50 V ceramic
C5, C10, C12, C14, C16	0.1 µF, 50 V ceramic
C6	120 pF, 50 V ceramic
C7, C8, C9	1 µF, 50 V ceramic
C11	2200 µF, 16 V United Chemicon SXC16VB222M18X35LL
C13, C15	2200 µF, 6.3 V United Chemicon SXC6.3VB222M16X25LL
C17	220 µF 6.3 V United Chemicon SXC6.3VB221M10X12LL
C18	75 pF, 500 V (mica or ceramic)
C19, C20	0.0047 µF, 250 V ac, class Y
C21	220 pF, 50 V (ceramic)
CR1	Bridge rectifier 600 V, 1 A
CR3	MUR110
CR4	1N5822
CR5, CR6	1N5819
IC1	Si9120DJ
L1	Common-mode choke 8 mH
L2	13 µH: core: Magnetics Inc J40401TC with 6 turns # 26 AWG
Q1	IRF820
Q2	2N7000
R1	453 kΩ .... 1% ... 1/4 W
R2	390 kΩ .... 5% ... 1/4 W
R3	10 kΩ ..... 1% ... 1/4 W
R4	10 kΩ ..... 5% ... 1/4 W
R5	15 kΩ ..... 1% ... 1/4 W
R6, R10	1 kΩ ..... 5% ... 1/4 W
R7	2.7 Ω ..... 5% ... 1/4 W
R8	10 Ω ..... 5% ... 1/4 W
R9	20 Ω ..... 5% ... 1/4 W
R11	2 kΩ ..... 5% ... 1/4 W
R12	510 Ω ..... 5% ... 1/4 W
T1	Schott Corp #6712244

References

1) Liu, K.H., *"Effects of Leakage Inductance on the Cross Regulation in a Discontunuous-Mode Flyback Converter,"* Proceedings, 1989 High Frequency Power Conference, Naples, Florida.

2) Chryssis, G., *"High Frequency Switching Power Supplies,"* McGraw Hill 1984.

Low-Power Universal-Input Power Supply Achieves High Efficiency

by Craig Varga

Expanding global markets have created a demand for what have become known as universal-input power supplies — that is, power supplies that allow devices to be plugged into wall outlets anywhere in the world. These power supplies must be able to operate directly from 100-, 110-, and 220-V ac power lines without the use of selector switches or jumpers. A power supply with the ability to operate under such conditions while remaining cost-effective is now becoming a necessity.

In the under 30-W power range, meeting the above requirements while maintaining high efficiency has been a challenge. Add to this the need to meet various international safety standards, and the circuit designer has his hands full.

The demands of low-power universal-input power supplies are met by the Si9120 pulse width modulation (PWM) controller from Siliconix. Using the Si9120, the flyback circuit presented in this application note demonstrates that designing universal-input supplies can be a simple task.

Circuit Topology

For the low power levels that are of interest here (under 30 W), the discontinuous-mode (DCM) flyback converter is the preferred topology. The biggest advantage of this topology is simplicity. The parts count in the power path cannot get any lower.

The peak-to-average primary current ratio in a DCM flyback is high relative to other topologies; however, at low power levels, this is not a serious drawback. On-state losses are minimal. Magnetics are small. Also, the transformer reset voltage is set by the minimum input voltage and remains fairly constant as the line voltage changes. As a result, a 600-V MOSFET proves adequate, even with ac inputs up to 300 V RMS.

The DCM flyback converter, when operated under current-mode control, provides a natural input volt-second limit, which helps keep the drain voltage from getting out of control during line or load transient conditions. Also, today's power MOSFETs are able to withstand avalanche current many times greater than a low power circuit can typically deliver (see appendix A). As such, the MOSFET will serve as a clamp for the occasional spike which may result from a short circuit or extreme load transient.

Cross regulation is fairly good, especially if leakage inductance between windings can be kept low.[1] In a universal-input application, meeting VDE input-to-output isolation requirements is essential. Depending on the end product, this can be as high as 3750 V RMS, primary to secondary — a figure that is totally inconsistent with the desire to achieve low leakage inductance. As a result, cross regulation between primary and secondary- referenced windings will be poor. This complicates the regulation of the primary-side bootstrap winding used to avoid secondary-to-primary feedback across the isolation boundary. The addition of a simple spike-blanking circuit solves the problem (see AN707, "Designing Low-Power Off-Line Flyback Converters Using the Si9120 Switchmode Controller IC").

When using the Si9120 for universal-input applications, it is recommended that a bootstrap winding be employed. While not strictly necessary, the power dissipation and chip temperature are higher if bootstrapping is not utilized. As an example, at V_{IN} = 400 V dc and I_{CC} = 1.5 mA, the power dissipation on the chip without a bootstrap is 600 mW. If a 10 V bootstrap supply is used, the dissipation is only 15 mW. This becomes more of a concern as the gate charge requirements of the power MOSFET increase, since the value of I_{CC} for the controller is largely dependent on gate drive demands.

Another advantage of the DCM flyback converter is its single-pole loop response. This makes compensating the feedback loop comparatively simple. In addition, transient response can be quite good in DCM flyback converters. It is possible (though not practical in a closed-loop system) to slew the power stage from no load to full load in only one switching cycle.

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Design Example

The circuit shown in Figure 1 is an 11.1-W, 3-output off-line supply. The input voltage is specified from 90- to 260-V ac. Outputs are +5 V at 1.5 A, +12 V at 150 mA, and −12 V at 150 mA. The design features full VDE isolation, primary side regulation, and true foldback current limiting. Operating frequency is 100 kHz.

DCM flyback operating principles are generally well understood and will not be presented here. Refer to Siliconix Application Note AN707 for a detailed design example. References 2 and 3 are also recommended.

Sizing the input capacitor and rectifiers for universal input requires more thought than for comparable single-input converters. Keep in mind that while the maximum input voltage occurs at high-input line, the maximum current stresses will occur at low line. This implies that the input capacitor value must be sized at low line while the voltage rating is dictated by the high-line condition. The bridge rectifier should be rated at 600-V dc minimum. The RMS current rating is calculated below.

For the present example:

Output power = 5.0 V x 1.5 A + 12 V x 0.15 A x 2 = 11.1 W

If efficiency is assumed to be 70%,

Input power = 11.1 W/0.7 = 15.86 W

For a little cushion, assume a low-input line voltage of 85 V ac.

Thus,

$$V_{dc} = 85\sqrt{2} = 120\text{V dc.}$$

Assuming a 20-V pk-pk input-capacitor ripple voltage the minimum voltage is

$$V_{min} = 120\text{ V} - 20\text{ V} = 100\text{ V.}$$

$$I_{in} = P_{in}/V_{DC}$$

$$= 15.86\text{ W}/100\text{ V} = 0.1586\text{ A}$$

$$C = I\frac{dt}{dv}$$

$$= \frac{0.1586\text{ A} \times 0.01\text{ s}}{20\text{ V}}$$

$$= 79\ \mu\text{F}$$

68 µF is a standard value. With 68 µF, the ripple voltage is

$$V_{pp} = I\frac{dt}{C}$$

$$= \frac{0.16\text{ A} \times 0.01\text{ s}}{68\text{E}-6\text{F}}$$

$$= 23.5\text{ V, an acceptable value.}$$

The capacitor voltage rating is calculated:

$$V_{max} = 260\text{ V ac} \times \sqrt{2} = 368\text{ V dc.}$$

A 400-V capacitor is acceptable. A rating of 450-V dc is preferable if high reliability is required or significant line transients are expected.

Assuming a power factor of 0.65, the RMS input current is

$$I_{ac} = \frac{P_o}{h_{ac}\,(PF)}$$

$$= \frac{11.1\text{ W}}{(0.7)\ (85\text{ V})\ (0.65)}$$

$$= 0.287\text{ A}$$

A 1-A bridge rectifier is more than adequate.

The primary inductance value is chosen by analyzing the lowest input voltage case. For a given load, the value of the peak transformer primary current will remain constant regardless of the input voltage. Since the primary inductance is fixed, the time to ramp to a given value of current is inversely proportional to input voltage (V = Ldi dt). Therefore, low line is where the most time is needed to ramp to the desired primary current. The duty factor limit dictates an on-time limit. After choosing an operating frequency and calculating the peak primary current, a value for primary inductance, L_P, can be determined as follows:

For 100 kHz, period = 10 µs.

At 50% duty factor, $t_{on(max)}$ = 5 µs.

$$I_{pk} = I_{in} \times 4$$

$$= (0.1586\text{ A})\ (4)$$

$$= 0.634\text{ A pk.}$$

For V_{IN} (dc) = 100 V

$$L = V\frac{dt}{dv}$$

$$= \frac{(100\text{ V})\ (5\text{E}-6\text{ s})}{0.634\text{ A}}$$

$$= 788\ \mu\text{H.}$$

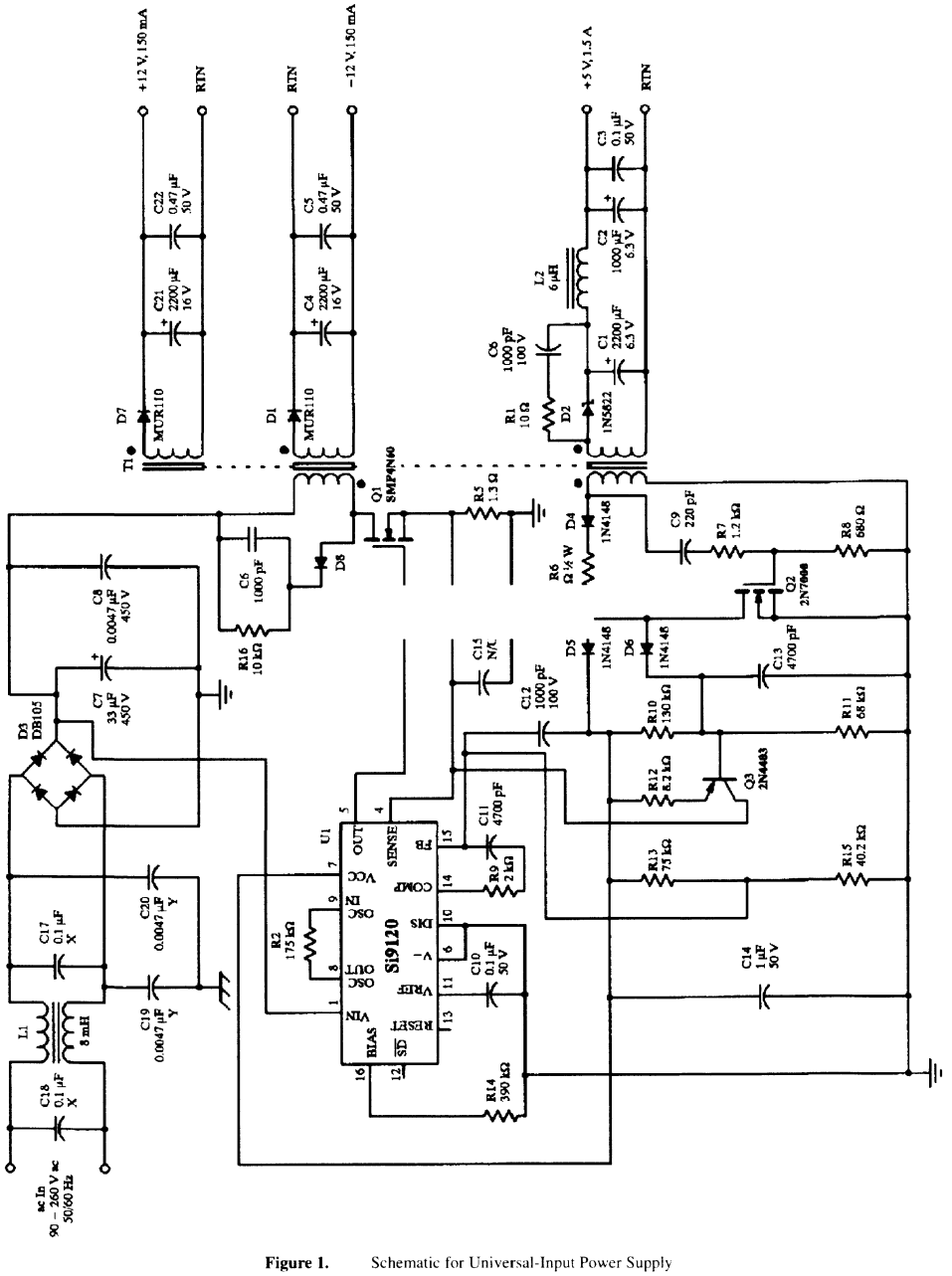


Figure 1. Schematic for Universal-Input Power Supply

The actual inductance used was 735 µH. [For high-volume production applications, the design engineer should consider the worst case tolerances for clock frequency and inductor value.]

See AN707 for transformer design equations and a fully worked example.

The biggest considerations for universal input are related to the additional insulation required to comply with VDE isolation specifications. The physical space occupied by the insulation typically reduces the useable fill factor to 25%. Furthermore, the increase in leakage inductance caused by large physical separation of the windings has the undesirable effects of creating large voltage spikes on the power MOSFET drain, contributing to power losses, and degrading load regulation.

Barrier tape at window ends will take up a lot of useable space, so a core geometry with a long, low window should be selected to minimize wasted area. This has the added benefit of reducing leakage inductance. (See equation 6.4 of reference 4.)

Wind the primary first. Apply the required insulation, and then wind the secondaries. All secondaries should be wound together with no intervening insulation, if voltage levels allow. Optimal cross regulation is achieved in this way.

Further reductions in leakage inductance can be realized by using interleaved windings. First wind one half of the primary, followed by the secondaries and remaining primary turns. The multiple primaries are usually connected in parallel. The spike blanking circuit described in AN707 virtually eliminates the primary-to-secondary leakage inductance problems, at least from the standpoint of the regulation effects.

In selecting a power MOSFET, the main concerns will be the $r_{DS(on)}$ and the drain voltage ratings. The transformer primary voltage during the off time is $V_P = (V_o + V_D)\ N_P/N_S$. Using the 5-V winding,

$V_P = (5.0\ V + 0.4\ V)(45\ T/7\ T) = 81$

Therefore,

$V_{DS(off)} = V_{IN(max)} + V_P = 368\ V + 81\ V = 449\ V.$

A 600 V MOSFET allows for a 150 V spike due to leakage inductance at high line. The RC snubber was sized empirically to keep the peak drain voltage below 600 V.

The SMP4N60 is the smallest 600-V device available. At 25°C the $r_{DS(on)}$ is 2.0 Ω. At 100°C, $r_{DS(on)}$ = 1.75 x 2 Ω = 3.5 Ω. The peak drain current was previously calculated at 0.634 A. The maximum RMS drain current is given by

$$I_{RMS} = I_{pk}\left(\frac{D}{3}\right)^{\frac{1}{2}} = 0.634A\left(\sqrt{\frac{0.5}{3}}\right) = 0.26\ A$$

On-state losses are given by

$P_{on} = I_{RMS}^2 \times r_{DS(on)}$

$= (0.26\ A)^2 \times 3.5\ \Omega$

$= 237\ mW.$

Switching losses are estimated at 350 mW. Since the thermal resistance is specified at 80°C/W, a total temperature rise of 47°C is expected. This permits operation up to approximately 50°C ambient temperature, while holding the maximum junction temperature to 100°C.

Something of more concern for universal-input than for a single-input voltage supply is the range of duty factor to be expected. Since the on time varies inversely with input voltage, the high-line on-time can become quite small in a high-frequency converter. For this kind of application, try to keep the minimum on time to not much less than 1 µs. This will help minimize noise problems with the current sense.

Also, be sure to use a non-inductive resistor for the current sense (carbon composition or film type). Use of a wire-wound resistor will produce large spikes which have to be filtered out. The dual-delay current-limit comparators of the Si9120 will frequently eliminate the need for a current-sense filter altogether. The magnitude of the noise on the current sense voltage will be affected by transformer parasitic capacitances and PCB layout. As such, every design will exhibit slightly different characteristics. Careful attention to detail in the magnetics design and construction as well as the board layout is a must.

For designs using current-sense resistors in the power MOSFET's source leg, note that the gate drive current is "seen" by the sense resistor. In very low-power designs, this can easily exceed the full load sense voltage causing severe noise problems. Adding a fairly large-value gate resistor will help in this case. Also, an RC current-sense filter becomes much more important.

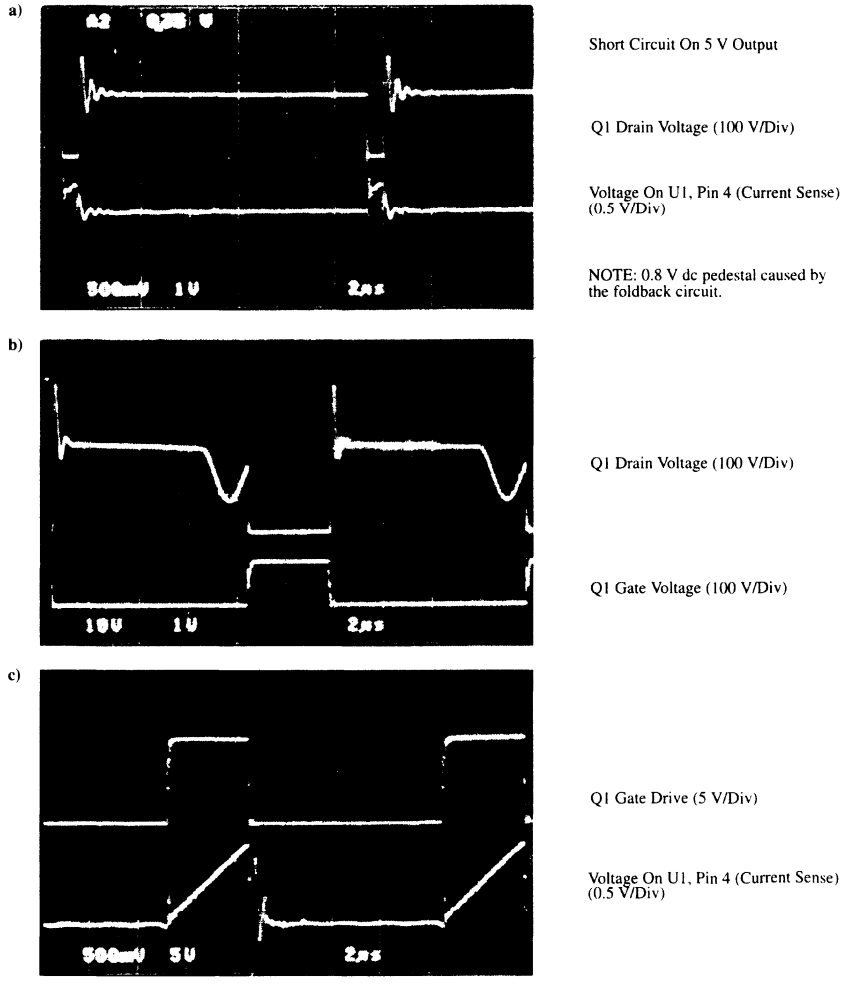
Foldback Circuit

Foldback current limiting is provided by Q3 and its associated components. Under normal operating conditions, diode D6 keeps C13 charged to V_{CC}. Hence, Q3 is biased off. In the event of a short circuit on any output, all winding voltages are clamped low. This causes the voltage on C13 to drop to a level set by divider R10 and R11. V_{CC} is held at 8.6 V by the Si9120's start-up regulator. The current set by the value of R12 flows through Q3 and R3, and causes the voltage on pin 4 to rise. Since a peak threshold of 1.2 V is internally set on pin 4, the voltage required across R5 to terminate a pulse is reduced by an amount equal to the drop on R3.

$I_D = \{1.2 - (I_{Q3})(R3)\}/R5$.

Thus as I_{Q3} increases, I_D decreases.

See Figure 2a for foldback operating waveforms.



Short Circuit On 5 V Output

Q1 Drain Voltage (100 V/Div)

Voltage On U1, Pin 4 (Current Sense) (0.5 V/Div)

NOTE: 0.8 V dc pedestal caused by the foldback circuit.

Q1 Drain Voltage (100 V/Div)

Q1 Gate Voltage (100 V/Div)

Q1 Gate Drive (5 V/Div)

Voltage On U1, Pin 4 (Current Sense) (0.5 V/Div)

Figure 2. Operating Waveforms (all photos full load, V_{IN} = 150 V dc)

The foldback circuit will not perform correctly without the spike blanking circuit. The leakage spike will peak charge C13 even with a shorted load. However, the foldback function is completely optional and all associated components can be eliminated if a lower cost supply is desired.

Test Results

Data compiled on the test circuit appear in Table 1. Combined line and load regulation measures ±2.7%, well within a ±5% specification. Measured efficiency is 73.4% with no effort at optimization. A detailed loss assessment could, no doubt, offer some improvements. Pulse load tests show reasonable transient response, and phase margin is measured at 60 degrees. For details on how to close the feedback loop, refer to Siliconix application notes AN713 and AN707.

Table I. Universal-Input Supply Test Data

All data taken with dc input source to ensure stable readings.

Full Load:

V_{IN} (dc)	I_{in} (mA)	+5 V	+12 V	−12 V
100 V	143.9	4.974	12.64	12.50
200 V	72.3	5.014	12.76	12.61
300 V	48.9	5.027	12.79	12.65
385 V	39.4	5.049	12.81	12.67

Half Load:

100 V	78.0	5.153	12.99	12.83
200 V	40.3	5.205	13.10	12.96
300 V	27.9	5.235	13.12	12.97
385 V	23.0	5.254	13.14	13.01

Pk-Pk Output Ripple Voltages (Spikes Not Included)		
5 V	+12 V	−12 V
60 mV	45 mV	40 mV

NOTE: Worst case over full line-voltage range.

Measured efficiency at V_{IN} = 300 V_{DC} was 73.4%.

During testing, an input capacitor value of as little as 33 µF proved adequate versus the design value of 68 µF. The low-value capacitor produces an input ripple voltage of 30 V pk-pk. Since the primary inductance is slightly lower than the design maximum value, the circuit is still able to maintain regulation with the higher input ripple voltage value. This is a good example of where trade-offs can be made during development programs. By using the larger input capacitance and primary inductance, the peak input current could be reduced slightly, and a slight improvement in efficiency should result. However, a larger input capacitance will decrease the conduction angle of the input rectifiers, and consequently will reduce the input power factor. The priorities of a particular application will determine the optimal approach.

Conclusion

The simple universal-input power supply design that has been presented combines economy and performance which should prove more than adequate for the majority of applications. The overall cost of the supply should rival linear regulators of similar power level if heatsink cost is considered. Good regulation has been achieved while maintaining the 3750-V ac input-to-output isolation mandated by VDE. The Si9120 eliminates the need for any external start-up circuitry. Also, foldback current-limiting is demonstrated which requires no feedback across the isolation boundary.

Appendix A

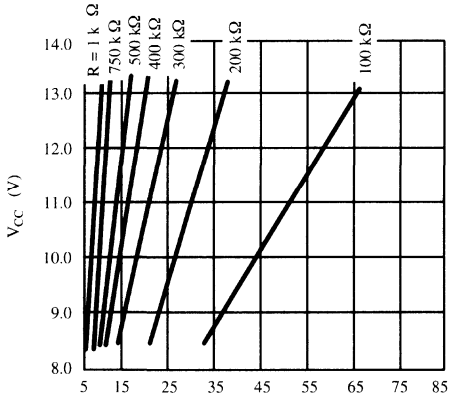
The SMP4N60 was tested for ability to withstand repetitive avalanche currents and for non-repetitive capability. Inductance values of 12 µH and 94 µH were used. Repetitive tests were run at 3 A, with 94 µH at 25°C. Failure current was measured at 25°C and 100°C. Results were as follows:

L = 94 µH		L = 12 µH	
25°C	100°C	25°C	100°C
4.25 A	2.40 A	7.28 A	6.40 A

For the 11.1-W flyback supply presented here, the leakage inductance is specified at 60 µH maximum. The maximum drain current is set to approximately 1.0 A. Therefore, based on the above data, adequate margin is present to prevent avalanche failure.

Appendix B

A number of performance parameters of the Si9120 can be altered by setting I_{bias} to a value other that 15 µA. At lower I_{bias}, higher efficiency can be obtained. At higher I_{bias}, lower propagation delays and a wider error amplifier bandwidth are possible. Also, if a V_{CC} supply other than 10 V is used, R_{bias} should be something other than 390 kΩ. Figure 3 below relates V_{CC} to R_{bias} and typical I_{bias}. The equation given can be used for points not on the graph.



$$R_{bias} = \frac{V_{CC} - 2.3\ V - 484\ \sqrt{I_{bias}}}{I_{bias}}$$

Figure 3. Relationship of V_{CC} to R_{bias} and Typical I_{bias}

References

1) Liu, K.H., "Effects of Leakage Inductance on the Cross Regulation in a Discontinuous-Mode Flyback Converter," Proceedings, 1989 High Frequency Power Conference, Naples, Florida.

2) Chryssis, G., "High Frequency Switching Power Supplies," McGraw Hill 1984.

3) Billings, K., "Switchmode Power Supply Handbook," McGraw Hill 1989.

4) McLyman, Col. W.T., "Transformer and Inductor Design Handbook," McGraw Hill 1988.

Universal Input Power Supply Parts List

C1 ..... 2200 µF, 6.3 V Al. Electrolytic – United Chemicon SXC
C2 ..... 1000 µF, 6.3 V Al. Electrolytic – United Chemicon SXC
C3, C10 .... 0.1 µF, 50 V Ceramic
C4, C21 .... 2200 µF, 16 V Al. Electrolytic – United Chemicon SXC
C5, C22 .... 0.47 µF, 50 V Ceramic
C6, C12 .... 1000 pF, 100 V Ceramic
C7 ..... 33 µF, 450 V Al Electrolytic (400 V ok)
C9 ..... 220 pF, 100 V Ceramic
C11, C13 ... 4700 pF, 100 V Ceramic
C14 ..... 1 µF, 50 V Ceramic
C16 ..... 75 pF, 500 V Ceramic or Mica
C17, C18 ... 0.1 µF, 250 V,ac VDE Class X2 Wima MKS 4-R
C8, C19, C20 0.0047 µF, 250 V,ac VDE Class Y Wima MP3-Y
D1, D7 ..... MUR 110 Motorola 1 A 100 V
D2 ..... 1N5822 3 A, 40 V Schottky
D3 ..... Bridge 1 A, 600 V DB105
D4, D5, D6 .. 1N4148
L1 ..... Common mode choke Renco 1361-2
L2 ..... Inductor 6 µH, 1.5 A
Q1 ..... FET N-channel SMP4N60 Siliconix
Q2 ..... FET N-channel 2N7000 Siliconix
Q3 ..... 2N4403 PNP (or 2N2907)
R1, R4 ..... 10 Ω, 1/8 Carbon Film or Metal Film
R2 ..... 175 kΩ, 1/8 W Carbon Film or Metal Film
R3 ..... 1 kΩ, 1/8 W Carbon Film or Metal Film
R5 ..... 1.3 Ω, 1/4 W Carbon Film or Metal Film
R6 ..... 20 Ω, 1/2 W Carbon Film or Metal Film
R7 ..... 1.2 kΩ, 1/8 W Carbon Film or Metal Film
R8 ..... 680 Ω, 1/8 W Carbon Film or Metal Film
R9 ..... 2 kΩ, 1/8 W Carbon Film or Metal Film
R10 ..... 130 kΩ, 1/8 W Carbon Film or Metal Film
R11 ..... 68 kΩ, 1/8 W Carbon Film or Metal Film
R12 ..... 8.2 kΩ, 1/8 W Carbon Film or Metal Film
R13 ..... 75 kΩ, 1/8 W 1% Carbon Film or Metal Film
R14 ..... 390 kΩ, 1/8 W Carbon Film or Metal Film
R15 ..... 40.2 kΩ, 1/8 W 1% Carbon Film or Metal Film
R16 ..... 330 Ω, 1/2 W 5% Carbon Composition
T1 ..... Schott Corp. #67122700

3-W High-Voltage Switchmode Regulator

Features

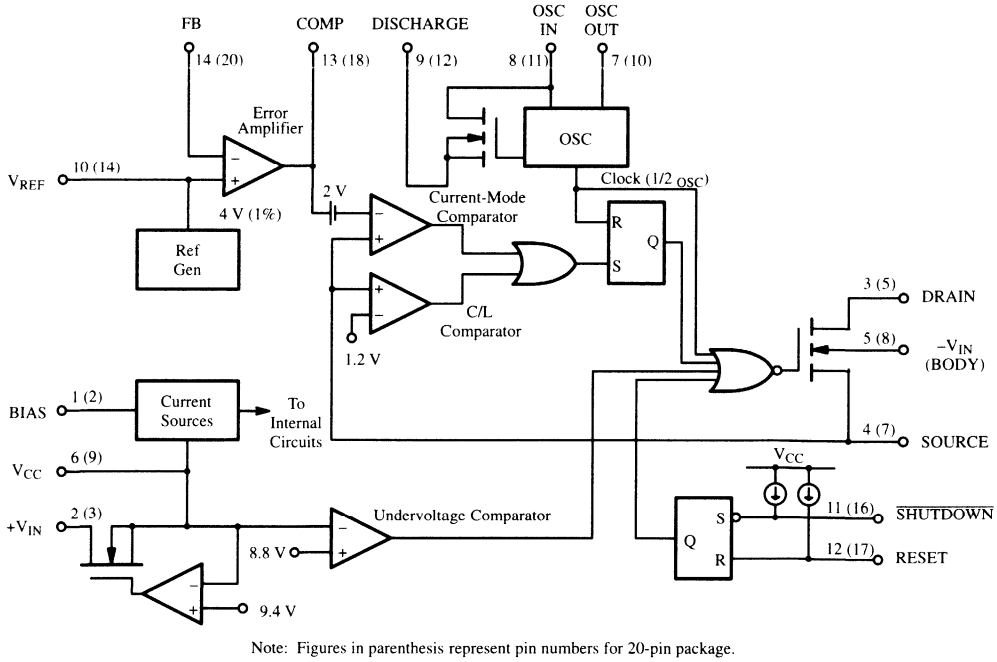
- 10- to 70-V Input Range
- Current-Mode Control
- On-Chip 150-V, 5-Ω MOSFET Switch
- Reference Selection Si9100 – ± 1%
- High Efficiency Operation (> 80%)
- Internal Start-Up Circuit
- Internal Oscillator (1 MHz)
- $\overline{\text{SHUTDOWN}}$ and RESET

Description

The Si9100 high-voltage switchmode regulators are monolithic BiC/DMOS integrated circuits which contain most of the components necessary to implement high-efficiency dc-to-dc converters up to 3 watts. They can either be operated from a low-voltage dc supply, or directly from a 10- to 70-V unregulated dc power source. The Si9100 may be used with an appropriate transformer to implement most single-ended isolated power converter topologies (i.e., flyback and forward), or by using a level shift circuit can generate a +5-V or a –5-V non-isolated output from a –48-V source.

The Si9100 is available in 14-pin plastic DIP and 20-pin PLCC packages. It is specified over the industrial, D suffix (–40 to 85°C) temperature ranges.

Functional Block Diagram



Note: Figures in parenthesis represent pin numbers for 20-pin package.

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70000. Applications information may also be obtained via FaxBack, request documents #70576 and #70584.

Absolute Maximum Ratings

Voltages Referenced to $-V_{IN}$ ($V_{CC} < +V_{IN} + 0.3$ V)

V_{CC} ..... 15 V
$+V_{IN}$ ..... 70 V
V_{DS} ..... 150 V
I_D (Peak) (Note: 300 µs pulse, 2% duty cycle) ..... 2.5 A
I_D (rms) ..... 350 mA
Logic Inputs (RESET, $\overline{\text{SHUTDOWN}}$, OSC IN) ..... –0.3 V to V_{CC} + 0.3 V
Linear Inputs (FEEDBACK, SOURCE) ..... –0.3 V to 7 V
HV Pre-Regulator Input Current (continuous) ..... 3 mA
Storage Temperature ..... –65 to 125°C
Operating Temperature ..... –40 to 85°C
Junction Temperature (T_J) ..... 150°C
Power Dissipation (Package)[a]
14-Pin Plastic DIP (J Suffix)[b] ..... 750 mW
20-Pin PLCC (N Suffix)[c] ..... 1400 mW
Thermal Impedance (Θ_{JA})
14-Pin Plastic DIP ..... 167°C/W
20-Pin PLCC ..... 90°C/W

Notes
a. Device mounted with all leads soldered or welded to PC board.
b. Derate 6 mW/°C above 25°C
c. Derate 11.2 mW/°C above 25°C

Recommended Operating Range

Voltages Referenced to $-V_{IN}$

V_{CC} ..... 9.5 V to 13.5 V
$+V_{IN}$ ..... 10 V to 70 V
f_{OSC} ..... 40 kHz to 1 MHz
R_{OSC} ..... 24 kΩ to 1 MΩ
Linear Inputs ..... 0 to 7 V
Digital Inputs ..... 0 to V_{CC}

Specifications[a]

Parameter	Symbol	Test Conditions Unless Otherwise Specified DISCHARGE = $-V_{IN}$ = 0 V V_{CC} = 10 V, $+V_{IN}$ = 48 V R_{BIAS} = 390 kΩ, R_{OSC} = 330 kΩ	Temp[b]	Limits D Suffix –40 to 85°C Min[c]	Typ[d]	Max[c]	Unit
Reference							
Output Voltage	V_R	OSC IN = – V_{IN} (OSC Disabled) R_L = 10 MΩ	Room	3.92	4.0	4.08	V
Output Impedance[e]	Z_{OUT}		Room	15	30	45	kΩ
Short Circuit Current	I_{SREF}	$V_{REF} = -V_{IN}$	Room	70	100	130	µA
Temperature Stability[e]	T_{REF}		Full		0.5	1.0	mV/°C
Oscillator							
Maximum Frequency[e]	f_{MAX}	R_{OSC} = 0	Room	1	3		MHz
Initial Accuracy	f_{OSC}	R_{OSC} = 330 kΩ, See Note f	Room	80	100	120	kHz
		R_{OSC} = 150 kΩ, See Note f	Room	160	200	240	
Voltage Stability	$\Delta f/f$	$\Delta f/f$ = f(13.5 V) – f, (9.5 V)/f(9.5 V)	Room		10	15	%
Temperature Coefficient[e]	T_{OSC}		Full		200	500	ppm/°C
Error Amplifier							
Feedback Input Voltage	V_{FB}	FB Tied to COMP OSC In = $-V_{IN}$ (OSC Disabled)	Room	3.96	4.00	4.04	V
Input BIAS Current	I_{FB}	OSC IN = $-V_{IN}$, V_{FB} = 4 V	Room		25	500	nA

Specifications[a]

Parameter	Symbol	Test Conditions UnlessOtherwise Specified DISCHARGE = $-V_{IN}$ = 0 V V_{CC} = 10 V, $+V_{IN}$ = 48 V R_{BIAS} = 390 kΩ, R_{OSC} = 330 kΩ	Temp[b]	D Suffix D Suffix –40 to 85°C Min[c]	Typ[d]	Max[c]	Unit
Error Amplifier (Cont'd)							
Input OFFSET Voltage	V_{OS}	OSC IN = – V_{IN}, (OSC Disabled)	Room		± 15	± 40	mV
Open Loop Voltage Gain[e]	A_{VOL}		Room	60	80		dB
Unity Gain Bandwidth[e]	BW		Room		1		MHz
Dynamic Output Impedance[e]	Z_{OUT}		Room		1000	2000	Ω
Output Current	I_{OUT}	SOURCE (V_{FB} = 3.4 V)	Room		–2.0	–1.4	mA
		SINK (V_{FB} = 4.5 V)	Room	0.12	0.15		
Power Supply Rejection	PSRR	OSC IN = – V_{IN}, (OSC Disabled)	Room	50	70		dB
Current Limit							
Threshold Voltage	V_{SOURCE}	R_L = 100 Ω from DRAIN to V_{CC} V_{FB} = 0 V	Room	1.0	1.2	1.4	V
Delay to Output[e]	t_d	R_L = 100 Ω from DRAIN to V_{CC} V_{SOURCE} = 1.5 V, See Figure 1	Room		100	200	ns
Pre-Regulator/Start-Up							
Input Voltage	$+V_{IN}$	I_{IN} = 100 µA	Room			70	V
Input Leakage Current	$+I_{IN}$	$V_{CC} \geq$ 10 V	Room			10	µA
Pre-Regulator Start-Up Current	I_{START}	Pulse Width ≤ 300 µs V_{CC} = V_{UVLO}	Room	8	15		mA
V_{CC} Pre-Regulator Turn-Off Threshold Voltage	V_{REG}	$I_{PRE-REGULATOR}$ = 10 µA	Room	7.8	9.4	9.7	V
Undervoltage Lockout	V_{UVLO}	R_L = 100 Ω from DRAIN to V_{CC} See Detailed Description	Room	7.0	8.8	9.2	
V_{REG} – V_{UVLO}	V_{DELTA}		Room	0.3	0.6		
Supply							
Supply Current	I_{CC}		Room	0.45	0.6	1.0	mA
Bias Current	I_{BIAS}		Room	10	15	20	µA
Logic							
$\overline{\text{SHUTDOWN}}$ Delay[e]	t_{SD}	V_{SOURCE} = $-V_{IN}$, See Figure 2	Room		50	100	ns
$\overline{\text{SHUTDOWN}}$ Pulse Width[e]	t_{SW}	See Figure 3	Room	50			
RESET Pulse Width[e]	t_{RW}		Room	50			
Latching Pulse Width[e] $\overline{\text{SHUTDOWN}}$ and RESET Low	t_{LW}		Room	25			
Input Low Voltage	V_{IL}		Room			2.0	V
Input High Voltage	V_{IH}		Room	8.0			
Input Current Input Voltage High	I_{IH}	V_{IN} = 10 V	Room		1	5	µA
Input Current Input Voltage Low	I_{IL}	V_{IN} = 0 V	Room	–35	–25		

Specifications[a]

Parameter	Symbol	Test Conditions UnlessOtherwise Specified DISCHARGE = $-V_{IN}$ = 0 V, V_{CC} = 10 V, $+V_{IN}$ = 48 V, R_{BIAS} = 390 kΩ, R_{OSC} = 330 kΩ	Temp[b]	D Suffix D Suffix –40 to 85°C Min[c]	Typ[d]	Max[c]	Unit
MOSFET Switch							
Breakdown Voltage	$V_{(BR)DSS}$	V_{SOURCE} = $V_{\overline{SHUTDOWN}}$ = 0 V I_{DRAIN} = 100 µA	Full	150	180		V
Drain-Source On Resistance[g]	$r_{DS(on)}$	V_{SOURCE} = 0 V, I_{DRAIN} = 100 mA	Room		3	5	Ω
Drain Off Leakage Current	I_{DSS}	V_{SOURCE} = $V_{\overline{SHUTDOWN}}$ = 0 V V_{DRAIN} = 100 V	Room			10	µA
Drain Capacitance	C_{DS}	V_{SOURCE} = $V_{\overline{SHUTDOWN}}$ = 0 V	Room		35		pF

Notes
a. Refer to PROCESS OPTION FLOWCHART for additional information.
b. Room = 25°C, Full = as determined by the operating temperature suffix.
c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum.
d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
e. Guaranteed by design, not subject to production test.
f. C_{STRAY} Pin 8 = ≤ 5 pF
g. Temperature coefficient of $r_{DS(on)}$ is 0.75% per °C, typical.

Timing Waveforms

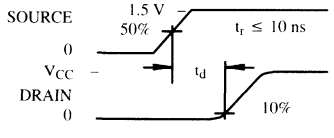


Figure 1.

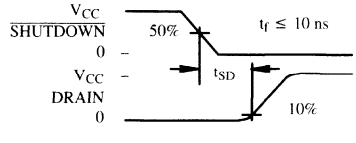


Figure 2.

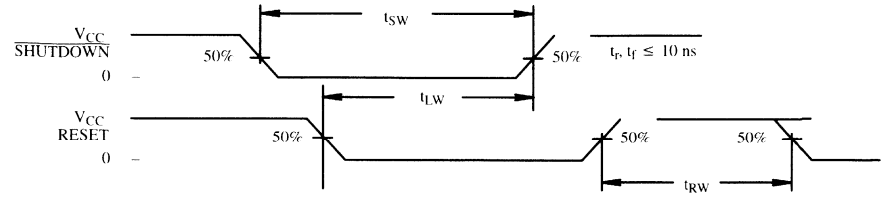
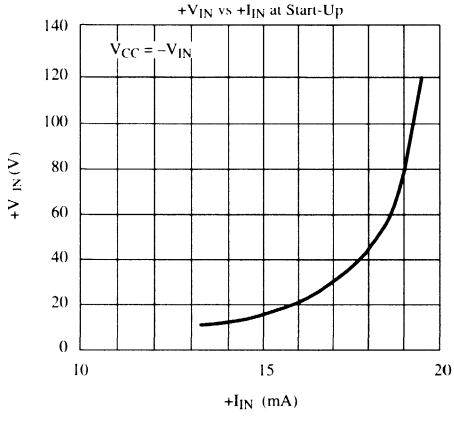
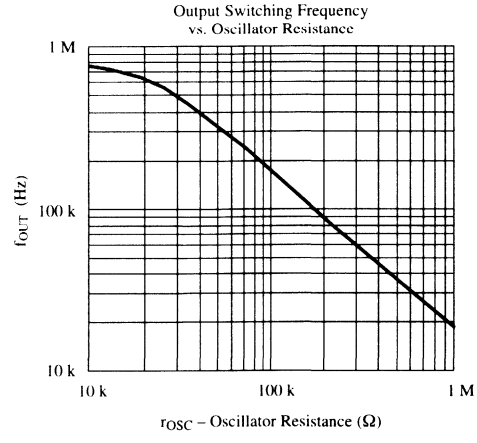


Figure 3.

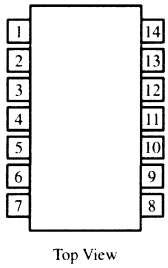
Typical Characteristics





Pin Configurations

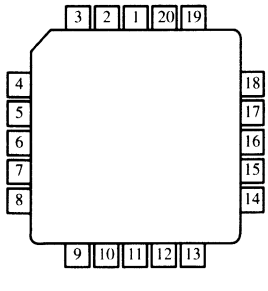
PDIP-14



Top View

Order Number
Plastic DIP: Si9100DJ02

PLCC-20



Top View

Order Number
Plastic PLCC: Si9100DN02

Function	Pin	
	14-Pin DIP	20-Pin PLCC*
BIAS	1	2
$+V_{IN}$	2	3
DRAIN	3	5
SOURCE	4	7
$-V_{IN}$	5	8
V_{CC}	6	9
OSC OUT	7	10
OSC IN	8	11
DISCHARGE	9	12
V_{REF}	10	14
SHUTDOWN	11	16
RESET	12	17
COMP	13	18
FB	14	20
*Pins 1, 4, 6, 13, 15, and 19 = N/C		

Detailed Description

Pre-Regulator/Start-Up Section

Due to the low quiescent current requirement of the Si9100 control circuitry, bias power can be supplied from the unregulated input power source, from an external regulated low-voltage supply, or from an auxiliary "bootstrap" winding on the output inductor or transformer.

When power is first applied during start-up, $+V_{IN}$ will draw a constant current. The magnitude of this current is determined by a high-voltage depletion MOSFET device which is connected between $+V_{IN}$ and V_{CC}. This start-up circuitry provides initial power to the IC by charging an external bypass capacitance connected to the V_{CC} pin. The constant current is disabled when V_{CC} exceeds 9.4 V. If V_{CC} is not forced to exceed the 9.4-V threshold, then V_{CC} will be regulated to a nominal value of 9.4 V by the pre-regulator circuit.

As the supply voltage rises toward the normal operating conditions, an internal undervoltage (UV) lockout circuit keeps the output MOSFET disabled until V_{CC} exceeds the undervoltage lockout threshold (typically 8.8 V). This guarantees that the control logic will be functioning properly and that sufficient gate drive voltage is available before the MOSFET turns on. The design of the IC is such that the undervoltage lockout threshold will not exceed the pre-regulator turn-off voltage. Power dissipation can be minimized by providing an external power source to V_{CC} such that the constant current source is always disabled.

Note: During start-up or when V_{CC} drops below 9.4 V the start-up circuit is capable of sourcing up to 20 mA. This may lead to a high level of power dissipation in the IC (for a 48-V input, approximately 1 W). Excessive start-up time caused by external loading of the V_{CC} supply can result in device damage. Figure 4 gives the typical pre-regulator current at start-up as a function of input voltage.

BIAS

To properly set the bias for the Si9100, a 390-kΩ resistor should be tied from BIAS to $-V_{IN}$. This determines the magnitude of bias current in all of the analog sections and the pull-up current for the $\overline{\text{SHUTDOWN}}$ and RESET pins. The current flowing in the bias resistor is nominally 15 μA.

Reference Section

The reference section of the Si9100 consists of a temperature compensated buried zener and trimmable divider network. The output of the reference section is connected internally to the non-inverting input of the error amplifier. Nominal reference output voltage is 4 V. During the reference trimming procedure the error amplifier is connected for unity gain in order to compensate for the input offset voltage in the error amplifier.

The output impedance of the reference section has been purposely made high so that a low impedance external voltage source can be used to override the internal voltage source, if desired, without otherwise altering the performance of the device.

Error Amplifier

Closed-loop regulation is provided by the error amplifier, which is intended for use with "around-the-amplifier" compensation. A MOS differential input stage provides for low input leakage current. The noninverting input to the error amplifier (V_{REF}) is internally connected to the output of the reference supply and should be bypassed with a small capacitor to ground.

Oscillator Section

The oscillator consists of a ring of CMOS inverters, capacitors, and a capacitor discharge switch. Frequency is set by an external resistor between the OSC IN and OSC OUT pins. (See Figure 5 for details of resistor value vs. frequency.) The DISCHARGE pin should be tied to $-V_{IN}$ for normal internal oscillator operation. A frequency divider in the logic section limits switch duty cycle to $\leq$ 50% by locking the switching frequency to one half of the oscillator frequency.

Remote synchronization is accomplished by capacitive coupling of a positive SYNC pulse into the OSC IN terminal. For a 5-V pulse amplitude and 0.5-μs pulse width, typical values would be 100 pF in series with 3 kΩ to OSC IN.

Detailed Description (Cont'd)

$\overline{\text{SHUTDOWN}}$ and RESET

$\overline{\text{SHUTDOWN}}$ and RESET are intended for overriding the output MOSFET switch via external control logic. The two inputs are fed through a latch preceding the output switch. Depending on the logic state of RESET, $\overline{\text{SHUTDOWN}}$ can be either a latched or unlatched input. The output is off whenever $\overline{\text{SHUTDOWN}}$ is low. By simultaneously having $\overline{\text{SHUTDOWN}}$ and RESET low, the latch is set and $\overline{\text{SHUTDOWN}}$ has no effect until RESET goes high. The truth table for these inputs is given in Table 1.

Both pins have internal current source pull-ups and should be left disconnected when not in use. An added feature of the current sources is the ability to connect a capacitor and an open-collector driver to the $\overline{\text{SHUTDOWN}}$ or RESET pins to provide variable shutdown time.

Table 1. Truth Table for the $\overline{\text{SHUTDOWN}}$ and RESET Pins

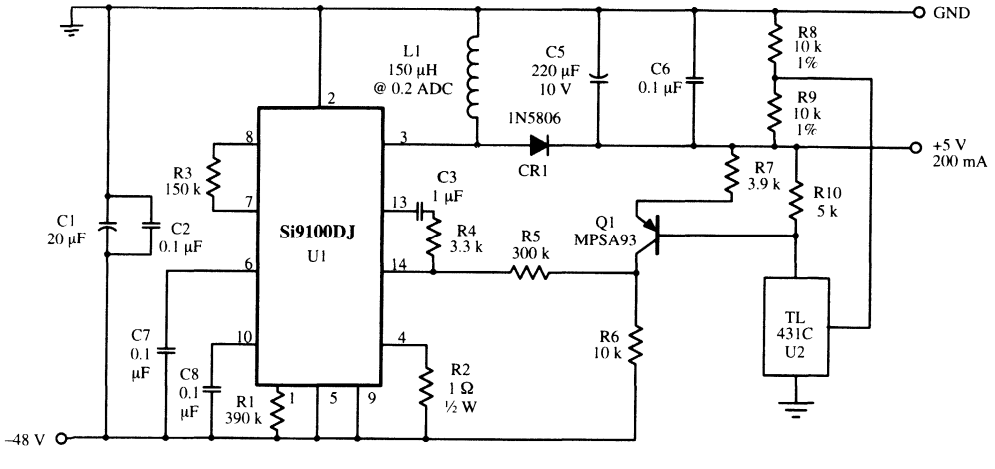
$\overline{\text{SHUTDOWN}}$	RESET	Output
H	H	Normal Operation
H	↿	Normal Operation (No Change)
L	H	Off (Not Latched)
L	L	Off (Latched)
∫	L	Off (Latched, No Change)

Output Switch

The output switch is a 5-Ω, 150-V lateral DMOS device. Like discrete MOSFETs, the switch contains an intrinsic body-drain diode. However, the body contact in the Si9100 is connected internally to $-V_{IN}$ and is independent of the SOURCE.

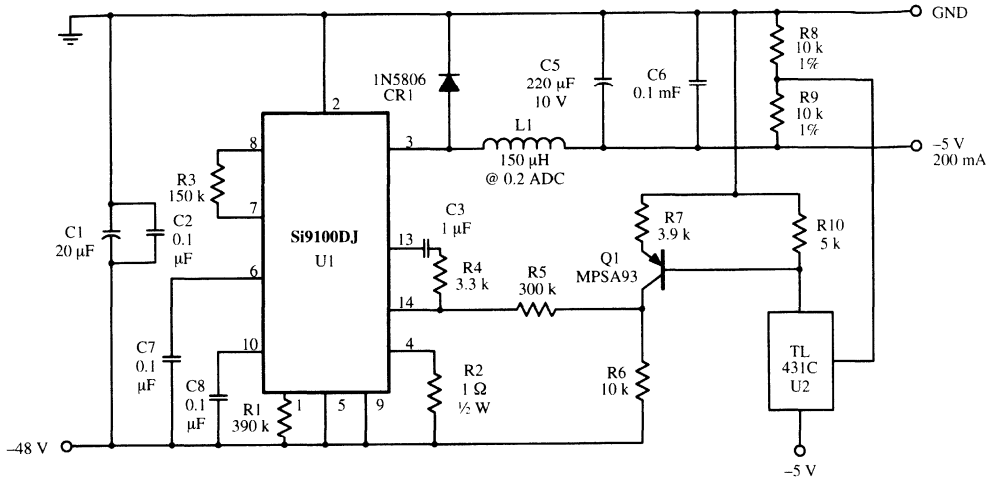
Applications

Buck–Boost
Non-Isolated 1-W Supply

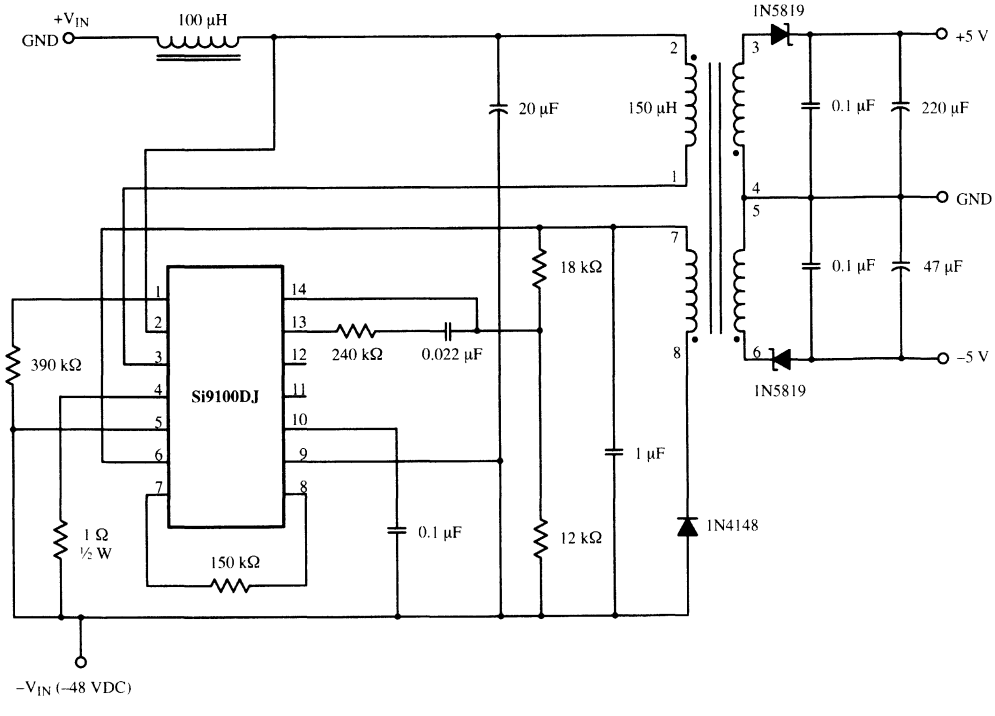


Applications (Cont'd)

Non-Isolated 1-W Supply (Buck)



One-Watt Flyback Converter for Telecommunications Power Supplies*



* For additional information on using the Si9100 in telecommunications and ISDN power supplies, see AN713 and AN702.

Efficient ISDN Power Converters Using the Si9100

James Blanc

One of the latest technology revolutions, an integrated worldwide telecommunications network, will be accompanied by another advance in power conversion technology. The integrated services digital network (ISDN) will allow different forms of information (voice, computer data, video, facsimile, etc.) to be transmitted over the telephone network. The International Consultative Committee for Telephone and Telegraph (CCITT) has proposed standards for the interfaces required to implement ISDN. Although the standards have yet to be formally adopted, telecommunications companies are moving ahead with pilot test programs, and semiconductor makers are developing chip sets to build ISDN hardware. Every network terminator (NT), signal regenerator (RG), and terminal equipment (TE) unit used for the implementation of ISDN will require a power converter.[1]

A major requirement of these telecom applications (due to the need for emergency-mode operation from a high-impedance source) is high-efficiency energy conversion at fractional-watt power levels. Minimization of parts count, another key factor for the design of these power converters, is sought to simultaneously achieve low cost and high reliability.

BiC/DMOS integrated circuit technology is ideally suited for the power requirements of ISDN. The analog and digital logic functions needed for pulse-width modulation can be implemented in CMOS to minimize quiescent current to the controller. DMOS transistors provide high-voltage power switching with both very low dynamic and gate drive losses. Integration of the CMOS controller on the DMOS power device yields the best overall performance at the lowest cost and component count.

Design Objectives

While some differences exist between designs, there are several requirements in addition to efficiency which are common to ISDN power converter applications. These include:

- reliable start-up and operation from the high source impedance of telephone subscriber lines (U-interface only)
- current limiting to prevent failure of other network terminals when one power converter output is shorted (S-interface only)
- a free-running internal oscillator for start-up as well as independent operation, which can be synchronized to an external clock signal
- electromagnetic interference (EMI) filtering to limit conducted emissions during both start-up and normal operation, as well as during equipment connections and disconnections.

The Si9100 power IC facilitates compliance with these design requirements with a minimum number of external parts. To illustrate this capability, a discontinuous conduction mode (DCM) flyback converter was built and tested. Measured efficiency was greater than 80% for a wide range of loads, and 60% efficiency was achieved with only a 15-mW load. Before describing the circuit concepts in detail, it is instructive to note the main features of the ISDN power-feeding concept which has been endorsed by the CCITT.

ISDN Power Feeding

Figure 1 is a block diagram of the ISDN basic access configuration. The two-wire transmission line defined at the U-interface provides a 192 k-bits-per-second (bps) digital data path which connects subscriber equipment to the local telephone exchange. Although ISDN permits many new services to be offered, the basic service of voice transmission remains a vital function. Therefore, the network power feeding from batteries in the local telephone exchange remains an essential part of modern telephone system planning. The network terminal (NT) connects the local loop, called the S-bus, to the U-interface at the customer's premises. ISDN-compatible terminals (TE1) communicate at a standard 64 k-bps rate over the four-wire S-bus. Non-ISDN-compatible terminal equipment (TE2), such as analog phones, must connect to the S-bus via a terminal adapter (TA).

Updates to this app note may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70576.

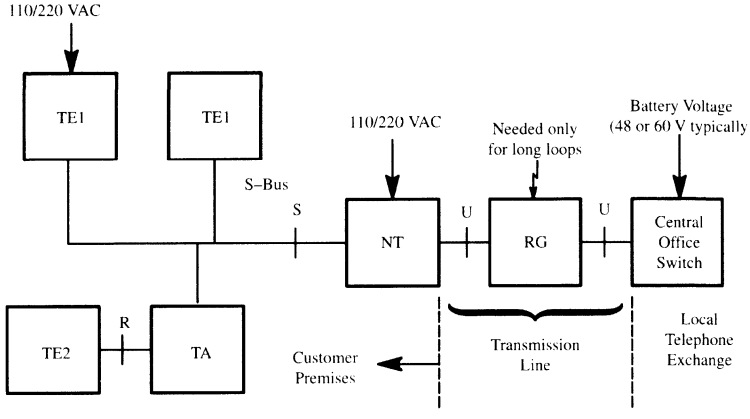


Figure 1. ISDN Basic Access Configuration

To minimize noise-coupling problems, the S-bus must be galvanically isolated from the two-wire U-interface. The CCITT recommendations call for an off-line power converter in the NT to supply 4 W at 40 V nominal to the S-bus during normal operation (for up to four telephones with full features). Other terminal equipment (e.g., fax terminals) would be fed solely from local ac power lines. In the event of a power outage, one telephone at the customer premises must be fed from the central office battery. This procedure is accomplished by reversing the voltage polarity on the S-bus. Non-priority terminals have a diode input which isolates them during emergency-mode operation. A single telephone terminal is fed via a full diode bridge, allowing it to operate during the emergency.

A signal regenerator may be required for long loops (U-interface). The Deutsche Bundespost (DBP) proposes to increase the feeding voltage from 60 V to 93 V to compensate for voltage drops on long lines requiring signal regeneration. The standard telephone line voltage used in many other parts of the world is 48 V. Whatever the voltage, the problem for power converters connected to telephone subscriber lines remains the same--they are fed from a high-impedance source.

Source Impedance Effects

The impedance of telephone subscriber lines limits the amount of power that can be supplied to the load. Referring to Figure 2, for a battery voltage, V_S, and line resistance, R_S, the maximum power to the converter is given by Equation 1, since the power limit occurs when source and load impedances are equal.

$$P_{MAX} = \frac{V_1^2}{R_e} = \frac{\left(\frac{V_S}{2}\right)^2}{R_e} = \frac{V_S^2}{4R_e} \quad (1)$$

R_e is defined as the effective low-frequency input impedance of the power converter.

For a flyback converter, with waveforms as shown in Figure 3, the calculation of the low-frequency input impedance is straightforward. The coupled inductor is designed to ensure operation in the discontinuous conduction mode (DCM). This operation requires that the core flux be reset to zero during each cycle. The current is zero at turn-on and ramps up at a rate given by di/dt = V_1/L_p. The maximum value of the peak primary current, I_{pk}, is

$$I_{pk} = \frac{di}{dt}(t_{ON(MAX)}) = \frac{V_1}{L_p}\frac{T_S}{2} \quad (2)$$

The 50% maximum duty ratio imposed by the Si9100 controller limits the "on" time of Q1 to one-half of the switching period. The average value of the current waveform in Figure 3 is the dc current in the inductor, L1. The current ripple in L1 is small, and the average inductor current, I_{DC}, during start-up is one-fourth the peak current value, as given by

$$I_{DC} = \left(\frac{I_{pk}}{2}\right)(D_{(MAX)}) = \frac{I_{pk}}{4} \quad (3)$$

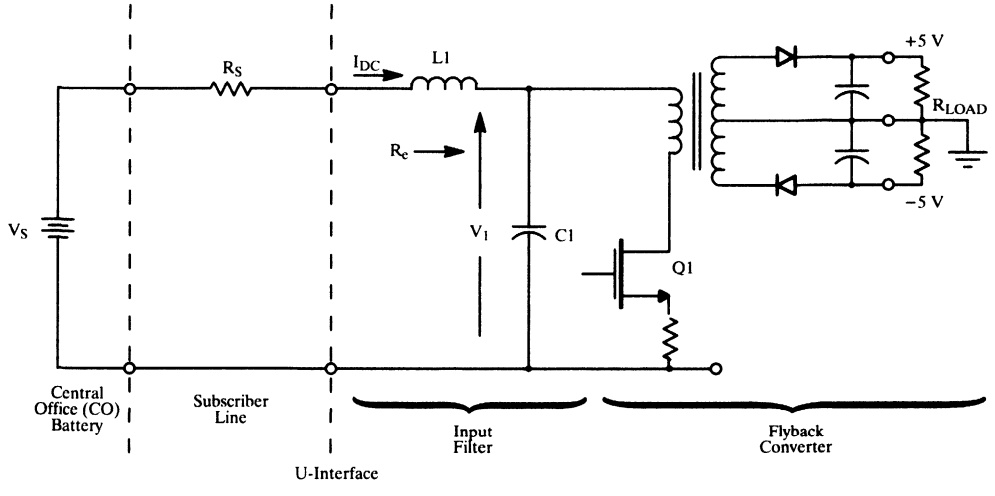


Figure 2. Power Converter with High Source Impedance

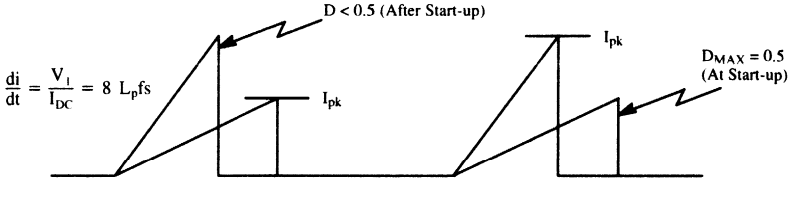


Figure 3. Primary Side Current Waveforms

Substituting this result into Equation 2 gives R_e in terms of the primary inductance, L_S, and switching frequency, f_S ($f_S = 1/T_S$).

$$R_e = \frac{V_I}{I_{DC}} = 8L_pf_S \quad (4)$$

L_p effectively acts as a current limiter during start-up, thus eliminating the need for active current limiting circuitry. The value of L_p must be chosen between a minimum value, which sufficiently limits start-up current, and a maximum value, which permits the rated throughput power to the load. Assume, for example, the maximum load condition given in Table 1.[2] The input power to the converter is the output power divided by the efficiency.

$$P_{IN} = \frac{P_O}{\eta} = \frac{0.650}{0.80} = 0.813 \text{ W} \quad (5)$$

Worst-case efficiency at maximum load is assumed to be equal to 80%. The input power to the converter is given by

$$P_{IN} = \frac{1}{2}L_pI_{pk}^2f_S \quad (6)$$

As seen from Figure 3, if L_p is doubled, I_{pk} is reduced by half. Therefore, P_{IN} varies in inverse proportion to L_p.

Referring again to Figure 1, the dc analysis of the input characteristics gives

$$V_I = V_S - I_{DC} R_S \quad (7)$$

Table 1. ISDN Power Requirements

Operating Mode	Load			Measured Efficiency
	+5 V Current	−5 V Current	Output Power	
Normal -- Active	100 mA	30 mA	650 mW	87%
Normal -- Power Down	11 mA	3 mA	70 mW	79%
Emergency -- Active	55 mA	9 mA	320 mW	88%
Emergency -- Power Down	3 mA	0 mA	15 mW	60%

Equations 2, 6, and 7 can be combined to give a quadratic equation which yields the maximum and minimum values for L_p. A graphical approach, however, gives the same answer and, at the same time, provides more insight into system behavior. After start-up has occurred, the power converter no longer presents a constant impedance at the input terminals. Instead, a constant power characteristic pertains, given by

$$P_{IN} = (V_I)(I_{DC}) = \text{constant} \quad (8)$$

The demonstration flyback converter was designed to operate from a battery voltage of 48 V and a maximum line resistance of 600 Ω. The constant power curve for $(V_I)(I_{DC}) = 0.813$, with the load line defined by V_S = 48 V and R_S = 600 Ω, are plotted in Figure 4. The intersection of the load line with the constant power curve determines two operating points, A and B, which occur at (V_I, I_{DC}) = (14.6 V, 55.7 mA) and (33.4 V, 24.3 mA). If V_S is slowly increased from zero, V_s and I_{DC} increase along the line, whose slope is R_e, from the origin to the constant power curve. This analysis is an oversimplification since a step increase in voltage is more likely to occur at power-up. However, worst-case start-up conditions occur at maximum R_S, which guarantees that the input filter is heavily overdamped. Therefore, the increase in V_I is monotonic, and the results of the simplified analysis are valid.

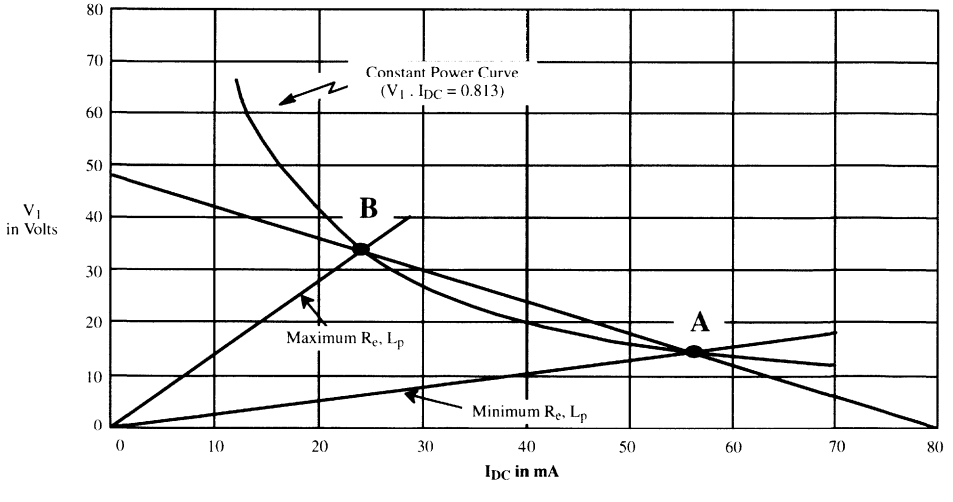


Figure 4. Flyback Converter Operating States

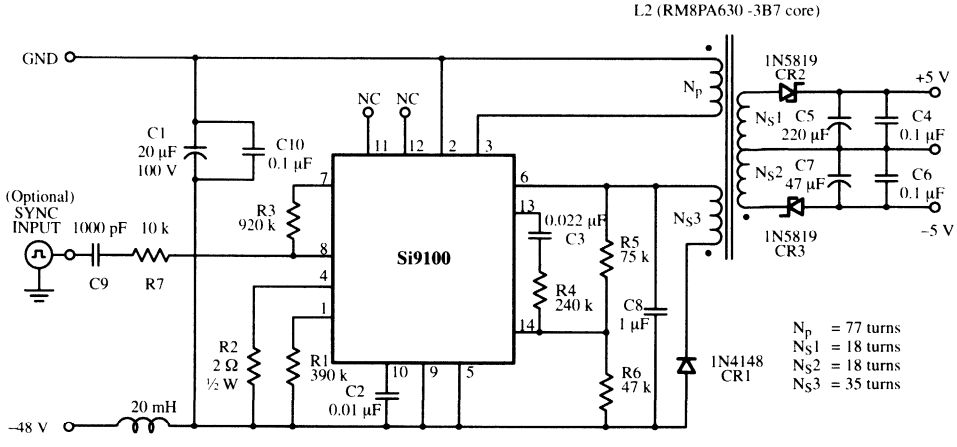


Figure 5. ISDN Flyback Converter

The lines from the origin to points A and B define the minimum and maximum values for R_e, and with Equation 4, also determine the limits for L_p.

$$R_{e(min)} = 14.6/0.0557 = 263\ \Omega$$
$$R_{e(max)} = 33.4/0.0243 = 1.37\ k\Omega$$

For a switching frequency design value equal to 20 kHz, Equation 4 gives

$$L_{p(min)} = 1.64\ mH$$
$$L_{p(max)} = 8.65\ mH$$

L_p may be chosen near the upper end of the permissible range for maximum start-up current limiting, or it may be chosen for maximum power transfer on a high-resistance line. Setting $R_e = R_S = 600\ \Omega$ for maximum power transfer gives

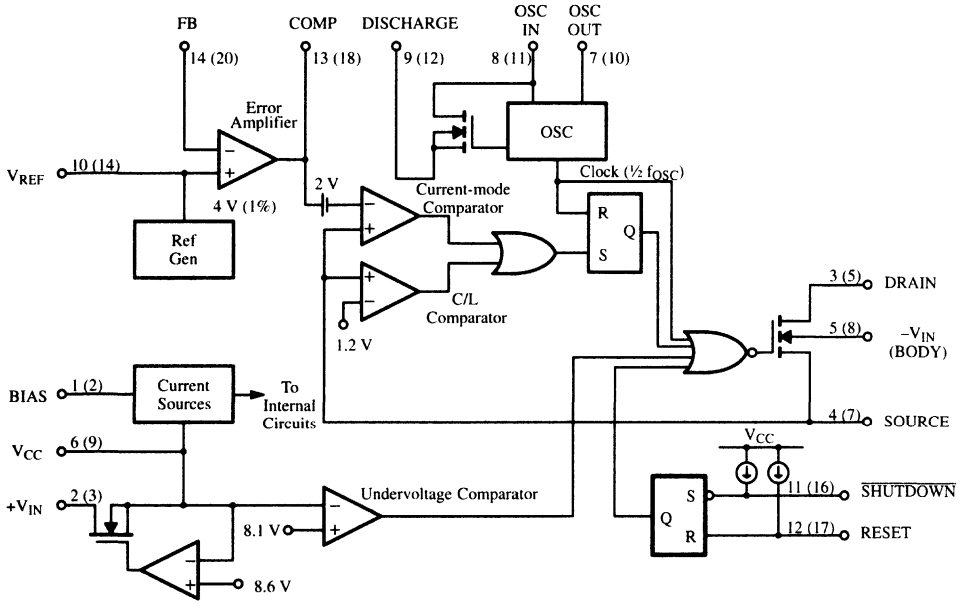
$$L_p = \frac{R_e}{8\ f_s} = \frac{600}{(8)(20,000)} = 3.75\ mH$$

The latter approach was chosen for the demonstration converter (see schematic in Figure 5). The Si9100 functional diagram is given in Figure 6 for reference.

Converter Performance

Measured efficiency data for the flyback converter is given in the last column of Table 1. Most notable is the 60% efficiency at a load of only 15 mW, which is allowed by the low quiescent current requirement of the CMOS control circuitry in the Si9100. Although power converters can operate at much higher frequencies, the dynamic losses incurred reduce the efficiency during the power-down state. The switching speed (30 ns typical) of the DMOS output transistor in the Si9100 permits operation above audible frequencies with very low dynamic and drive losses. Such performance cannot be achieved with bipolar transistors. A single resistor, R3, sets the oscillator frequency at approximately 34 kHz. A positive sync pulse (5 V amplitude and 0.5 µs pulse width) at 40 kHz was fed through R7 and C9 to pin 8 to demonstrate the principle of synchronization with an external clock. Typically, the free-running frequency should be set at 10 to 20% below the external clock frequency (note that the switching frequency is ½ of the oscillator frequency).

Start-up characteristics were verified by connecting a 600-Ω resistance from a dc power supply to the converter input terminals. Reliable start-up was demonstrated at maximum load for supply voltages as low as 44 V. With zero source resistance inserted in the line, the converter maintained regulation down to an input voltage of 23 V. In both cases, the maximum operating voltage is 70 V for the Si9100 . The inductor, L1, was wound with 540 turns of #32 magnet wire on a #55206 molypermalloy powder core.



NOTE: Figures in parenthesis represent pin numbers for 20-pin package.

Figure 6. Si9100 Functional Diagram

The relatively high series resistance of this inductor (6 Ω) provides series damping of the input filter. This damping reduces peaking of the filter output impedance, preventing degradation of the control loop response at the filter resonant frequency when the supply is operated from a low-resistance source.

Measured ripple on both outputs was less than 50 mV peak to peak, and regulation was better than 5% over line and load. The –5-V output increases from –5.05 V to –5.75 V when totally unloaded.

The current-mode controller of the Si9100 provides fast current-limiting response in the event of a shorted output. With either output shorted to ground, the measured value of short-circuit current drawn at the converter input was 30 mA. Any output terminal can be shorted for an indefinite period with no resulting high stress condition on the Si9100. Normal operation resumes when the short circuit is removed.

The input filtering provided by L1 and C1 provides a calculated attenuation of 68 dB at the fundamental of the switching frequency. This allows compliance with FCC Class B and VDE-0871/B requirements; however, conformance testing to these specifications was not performed. Common-mode noise coupling is minimized by the Si9100 since the MOSFET drain is electrically isolated from the package case (a 14-pin DIP). Therefore, very little parasitic capacitance exists from drain to ground. Since the Si9100 places both the driver and MOSFET on the same chip, gate driver lead lengths are reduced from a few centimeters for discrete designs to a few hundred microns.

The 5-mA/μs dynamic current limit required during connection of equipment to the S-bus[3] is met by selecting a suitably high value, 20 mH, for L1. Since several ohms of series resistance is desired, a small wire gauge is used and the inductor is not prohibitively large. A smaller value may be chosen for L1 where the EMI requirements are less critical.

Summary

BiC/DMOS power IC technology is ideally suited for the requirements of low-power dc/dc converters, such as those required for the implementation of ISDN. A circuit design for an 85%-efficient power converter using the Si9100 SMARTPOWER IC has been presented here. Measured performance data is given, along with a graphical analysis method for ensuring reliable start-up when power is fed from a high-impedance source.

References

1. Rosenbaum, D. and K.H. Stolp. "The Feeding Conception of the ISDN Basic Access," IEEE INTELEC Conference Proceedings, Munich, FRG, Oct.14-17, 1985, 505-512.
2. Sigloch, R. "Requirements for Small High Efficiency dc/dc Converters in Complex Communication Networks," IEEE INTELEC Conference Proceedings, Toronto, Canada, Oct 19-22, 1986, 197-202.
3. Krautkramer, W. and B. Schickling. "Remote Power Feeding of ISDN-Terminals at the Basic Access," IEEE INTELEC Conference Proceedings, Munich, FRG, Oct. 14-17, 1985, 513-519.

A 1-Watt Flyback Converter Using the Si9100

James Blanc

The Si9100 is a monolithic BiC/DMOS SMARTPOWER IC which combines high-efficiency CMOS logic, a high-voltage switching transistor and high-voltage pre-regulator on a single die. It is the first low-cost, high efficiency regulator designed to operate directly from unregulated high-voltage dc power sources in areas such as telecommunications and avionics. The primary application will be in feature phones and ISDN terminals to power the logic components without exceeding the load limits set by the telecommunications industry. Power integrated circuit technology allows low-power CMOS control circuits to be combined with DMOS power transistors in the Si9100. The resulting reduced parts count decreases system cost, improves reliability, and simplifies circuit design.

The flyback converter presented here uses the Si9100 to provide an isolated ±5 V supply rated at 1 W. Specifications for this supply are as follows:

Input Voltage . . 15 to 70 V_{DC}

Maximum load +5 V @ 167 mA,
–5 V @ 33 mA
Minimum load . +5 V @ 32 mA,
–5 V @ 8 mA
Regulation .... ±5%
Maximum Ripple ..... 100 mV p-p
Switching Frequency ..... 100 kHz
Efficiency .... 80% min for 1 W load
75% min for 0.2 W load

A schematic for the flyback converter is found in Figure 1, with a parts list provided in Appendix B. However, before discussing the details of the power supply design, it is instructive to review the functions of the Si9100 integrated circuit.

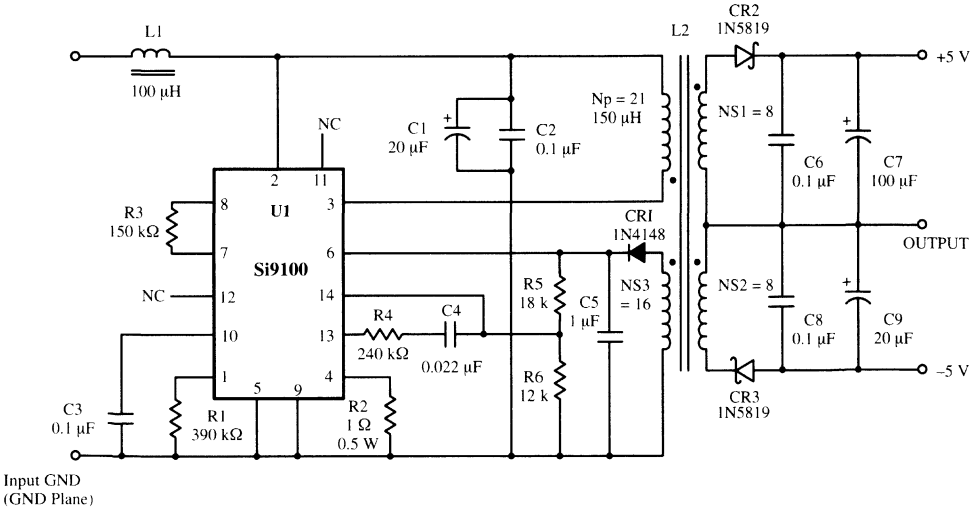


Figure 1. Schematic Diagram of the Si9100 Discontinuous Flyback Converter Circuit

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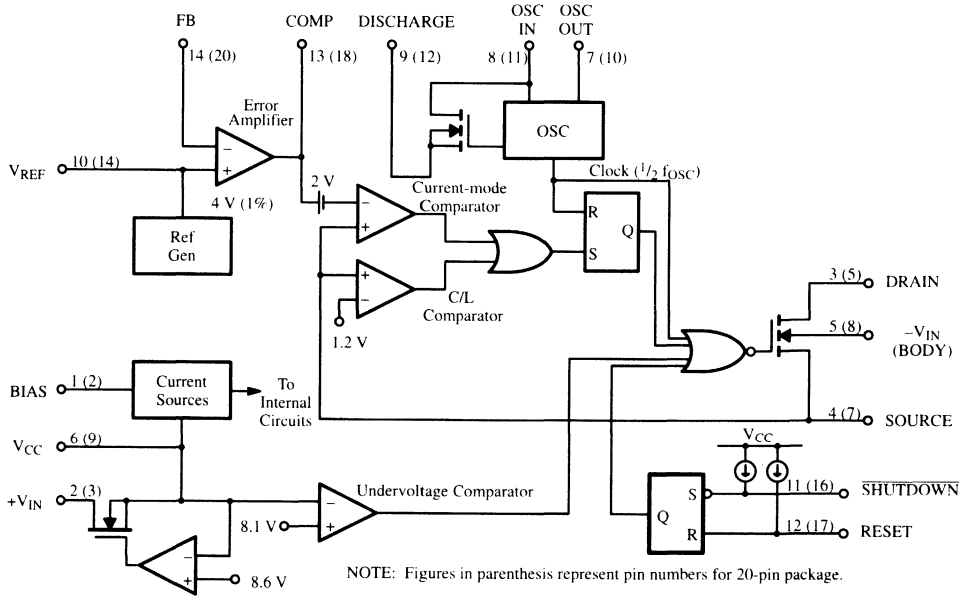


Figure 2. Si9100 Simplified Block Diagram

Si9100 Description

As shown in the block diagram of Figure 2, the Si9100 combines an oscillator, pre-regulator/start-up circuit, precision voltage reference, error amplifier, current-mode controller, and a MOSFET switching transistor into one 14-pin dual-in-line package. Overcurrent protection, undervoltage lockout, and logic inputs for both latched and unlatched shutdown modes are also included.

Start-up/Preregulator Circuit

A unique start-up/preregulator circuit, which is shown in Figure 3, permits the Si9100 to operate over a wide input voltage range (10 to 70 V). The input voltage for the device is connected between the $+V_{IN}$ (pin 2) and $-V_{IN}$ (pin 5) terminals. The high-voltage depletion-mode (normally ON) MOSFET acts as a current source during start-up, charging the capacitance at the V_{CC} terminal (pin 6) directly from the input source. When V_{CC} exceeds the 8.1 V undervoltage threshold, the output switch is enabled to provide well-defined start-up characteristics. V_{CC} is then regulated to 8.6 V by the pre-regulator circuit. If an external voltage source greater than 8.6 V is fed to the V_{CC} terminal, the depletion-mode MOSFET is shut off to reduce power drain from the input power source.

Oscillator

The oscillator requires a single resistor to set its frequency. The requirements of flux reset in single-ended converters generally dictates a maximum duty cycle of 50%. With the oscillator frequency set at two times the desired switching frequency, a flip-flop divides the clock signal by two, and the logic disables the output during every other clock cycle.

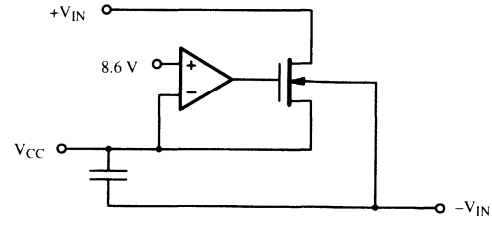


Figure 3. Schematic Diagram of the Start-up Section of the Si9100

MOSFET Switch

The MOSFET switching transistor has typical $r_{DS(ON)}$ and $V_{(BR)DSS}$ characteristics of 4 Ω and 180 V, respectively. Worst case specifications are 5 Ω and 150 V. The device is a lateral DMOS structure which has external connections for the DRAIN (pin 3) and SOURCE (pin 4). The body of the MOSFET is internally tied to the $-V_{IN}$ terminal, which must be connected to the most negative input potential in the circuit.

Error Amplifier

The error amplifier permits compensation of control loops for stable regulator operation. The amplifier uses PMOS input transistors to provide high input impedance (2 MΩ minimum), and is internally compensated for unity gain stability, with 1 MHz (typical) bandwidth and 60° phase margin.

Protection

In addition to the undervoltage lockout function already described, the Si9100 provides overcurrent protection and inputs for external logic control. With a sense resistor (typically 1 to 2 Ω) connected from the MOSFET source to the $-V_{IN}$ terminal, the voltage at pin 4 is proportional to the output current. When this voltage exceeds a 1.2 V reference the overcurrent comparator disables the output MOSFET. The shutdown delay is typically 100 ns (200 ns maximum).

Logic inputs $\overline{\text{SHUTDOWN}}$ (pin 11) and RESET (pin 12) permit the use of latched or unlatched shutdown modes. Internal current source pull-ups normally hold both logic pins high. If the $\overline{\text{SHUTDOWN}}$ pin is pulled low while the RESET is high, then the output switch will be disabled until the $\overline{\text{SHUTDOWN}}$ pin is again allowed to go high. This is the unlatched shutdown mode. If, however, the RESET pin is pulled low while the $\overline{\text{SHUTDOWN}}$ pin is also pulled low, then the converter will be latched off until RESET goes high again.

Flyback Converter Operation

Start-up

Applying input voltage to the circuit initiates charging of capacitor, C_1, through the filter inductor, L_1. The depletion-mode MOSFET, as described above, supplies current to capacitor C_5 through the V_{CC} terminal of the IC. When V_{CC} reaches the undervoltage threshold (8.1 V), then transistor switching begins. The 4 V reference and the voltage divider ratio formed by R_5 and R_6 cause the feedback winding, N_{S3}, to be regulated to +10 V. After start-up is complete the feedback voltage trips the comparator to turn off the pre-regulator circuit, and the Si9100 derives its bias power from the feedback winding. The power saved by this bootstrap technique is equal to the product of the IC supply current times the difference between V_{IN} and V_{FB}:

Power Saved = (600 µA) (48 V – 10 V) = 23 mW

While this is not a great deal of power, it does represent 2.3% of the output for a 1 W supply. Integrated Services Digital Network (ISDN) applications require such techniques for bias power minimization in order to meet emergency-mode limits for the power-down state.

Flyback Operation

Flyback converter operation is illustrated by the basic waveforms shown in Figure 4. When the MOSFET switch is turned on, current will ramp up in the primary at a rate given by:

$$\frac{di}{dt} = \frac{V}{L} = \frac{I_{pk}}{t_{ON}}$$

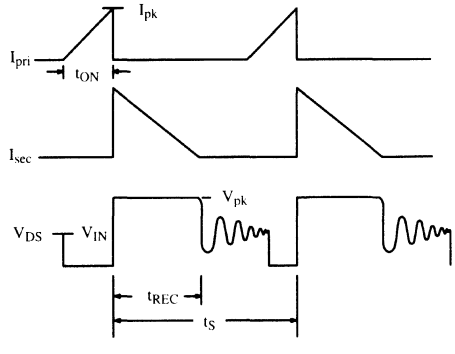


Figure 4. Flyback converter waveforms

Stored energy, given by $^1/_2 L_P I_{pk}^2$, is present in L_2 at the time the MOSFET is switched off. This energy is released to the secondary windings, N_{S1} through N_{S3}, during the off time, as shown by the total secondary current, I_{sec}, in Figure 4.

This is the flyback principle in its simplest terms. A transformer is designed to transfer energy directly from the primary to the secondary, with as little stored energy as possible.

A flyback inductor receives energy during one interval of the switching cycle, then releases this stored energy at a later interval of the switching cycle.

During the time that the secondaries are conducting, shown as t_{REC}, the magnetic flux recovers, or "resets" to zero, and the MOSFET must block the sum of the reflected voltage from the secondary and the input voltage. This requires a worst case blocking voltage of:

$$V_{pk} = V_{IN} + \frac{N_P}{N_{S1}}(V_O + V_D)$$

$$= 70 + \frac{21}{8}(5.0 + 0.5) = 85 \text{ V}$$

A leakage inductance spike appears at the leading edge of the V_{DS} waveform. The spike is less than the 150 V minimum $V_{(BR)DSS}$, and no snubber network is required. Since the flux is reset to zero before the end of each switching cycle, current flow through the secondary is discontinuous. Consequently, this circuit is called a discontinuous-conduction-mode (DCM) flyback converter.

Regulator Control Loop

The function of the regulator control loop is to maintain the output voltages constant as either the input line voltage or load current vary. These are termed "line regulation" and "load regulation", respectively.

A sense winding has been chosen to close the regulator loop and provide output isolation. Since the secondary windings are coupled on a common core, the volts/turn ratio is the same for N_{S1}, N_{S2} and N_{S3}. The resulting secondary voltages will track each other quite closely. There is, however, some degradation in load regulation due to leakage (uncoupled) inductance between the $^1/_2$ 5-V output windings and the sense winding. This effect becomes progressively worse as the switching frequency is increased. The coupled inductor used here has been designed for good coupling between output and sense windings in order to maintain better than 5% regulation over the 0.2 W to 1 W load range. Design details for the coupled inductor are included in Appendix A.

To analyze the system closed loop response, begin by reflecting the filter capacitance and load resistance from each output winding to the feedback winding.

$$C_{eff} = C_5 + \left(\frac{N_{S1}}{N_{S3}}\right) \text{ x } (C_7 + C_9)$$

$$= 1\ \mu\text{F} + \left(\frac{8}{16}\right)^2 (100\mu\text{F} + 20\mu\text{F}) = 31\mu\text{F}$$

The effective load resistance, R_{eff}, can be found by assuming that the entire 1-W load is connected across the sense winding output:

$$R_{eff} = \frac{V_S^2}{P_O} = \frac{(10\text{V})^2}{1\text{W}} = 100\ \Omega$$

The effective load impedance is determined at low frequency by the 100 Ω resistance and at high frequency by the capacitive reactance given by $X_C = 1/\omega C_{eff}$. The control-to-output transfer function thus has a pole at:

$$f_p = \frac{1}{2\pi R_{eff} C_{eff}} = \frac{1}{2\pi(100)(31 \text{ x } 10^{-6})} = 51 \text{ Hz}$$

To calculate the low frequency gain of the power stage, assume a 1 mV change in the error voltage, V_e, at the output of the error amplifier, and calculate the voltage change, ΔV_S, which results at the feedback winding. Then combine the power stage gain with the error amplifier gain (including the voltage divider) to yield the total loop response. Assume for these calculations that the converter efficiency remains constant at 83.33%.

$$P_{IN} = \frac{P_O}{\eta} = \frac{1\text{ W}}{0.8333} = 1.2 \text{ W}$$

The power input to the converter is the product of the stored inductive energy times the switching frequency.

$$P_{IN} = ½ L_p (I_{pk})^2 \bullet f_s$$

Rearranging to solve for I_{pk} gives:

$$I_{pk} = \sqrt{\frac{2\ P_{IN}}{L_P \text{ x } f_s}} = \sqrt{\frac{2(1.2)\text{ W}}{(150\ \mu\text{H})\ 10^5\ \text{Hz}}} = 0.4 \text{ A}$$

Since the current sense resistor, R_2, equals 1 Ω, a 1 mV change in the error voltage (at pin 13) will result in a 1 mA change in the peak inductor current, i.e., $\Delta I_{pk} = \Delta V_e$. A 1 mA increase in I_{pk} causes P_{IN} to increase to:

$$P_{IN} = ½ L_p (I_{pk} + DI_{pk})^2 \bullet f_s =$$

$$½ \bullet 150 \bullet 10^{-6} (0.400 + 0.001)^2 \bullet 10^5 = 1.206 \text{ W}$$

Assuming efficiency remains constant,

$$P_O = (0.833) \bullet P_{IN} = 1.005 \text{ W}$$

This translates to an increase in the sense voltage to:

$$V_S = \sqrt{P_O \text{ x } R_{eff}} = \sqrt{(100 \text{ x } 1.005)} = 10.025 \text{ V}$$

The gain is given by:

$$\frac{\Delta V_S}{\Delta V_c} = \frac{10.025\ V - 10\ V}{1\ mV} = 25$$

At full load the low frequency gain of the power stage is 25 (28 dB), with a single pole in the transfer function at 51 Hz. Performing a similar calculation at the 20% load condition yields a gain of 56 (35 dB) with a pole at 10 Hz. There will also be a zero in the transfer function at approximately 30 kHz due to capacitor ESR.

The solid line in Figure 5 represents the transfer function of the converter power stage at full load. The corresponding curve at a 20% load is shown in Figure 6. To complete the analysis of the control loop requires accounting for the resistive voltage divider and the error amplifier. The resistor R_6 sets the dc bias condition, but does not enter into the small signal analysis.

At high frequencies the gain is R_4/R_5, with a zero occurring in the transfer function at

$$f_Z = \frac{1}{2\pi\ (240\ k\Omega)\ (0.022\ \mu F)} = 30\ Hz$$

The error amplifier response is shown in Figures 5 and 6 as dashed lines. The error amplifier response times the power stage gain gives the total loop gain, which is shown as the gray line for full load in Figure 5 and light load in Figure 6. Actual measurements of loop gain and phase yielded a loop bandwidth of 14 kHz with 68 degrees phase margin. Figure 7 shows the response of the +5-V output as the load is stepped between 20% and 100% of full load. Response time is under 200 µs with no overshoot.

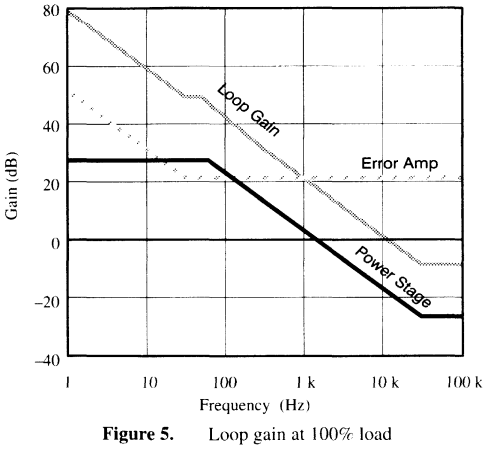


Figure 5. Loop gain at 100% load

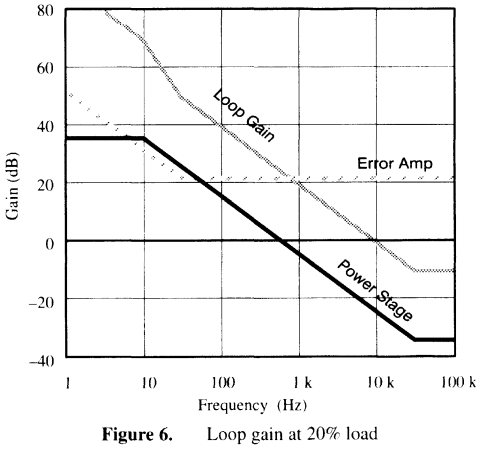


Figure 6. Loop gain at 20% load

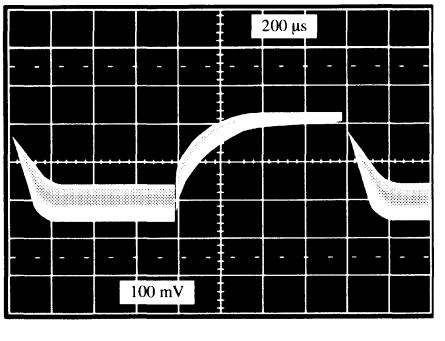


Figure 7. Step Load Response

ISDN APPLICATIONS

Integrated Services Digital Network (ISDN) poses some unique problems to telecom systems design engineers. Standards proposed by the International Telephone and Telegraph Consultative Committee (CCITT) recommend that input power to ISDN terminal equipment (TE) meet the limits outlined in Table I[1].

Table I. ISDN Power Requirements

Operating Mode	Maximum Input Power to TE	Efficiency Target
Normal-active	900 mW	70%
Normal-power down	100 mW	60%
Emergency-active	400 mW	70%
Emergency-power down	25 mW	40%

The 25-mW limit during emergency power-down mode operation may be especially troublesome[2]. In order to supply 10 mW to the TE for such functions as memory back-up, total converter losses must be less than 15 mW. Under such light load conditions the major power loss is in the PWM controller. Only controllers implemented in CMOS can presently be expected to meet this requirement.

Although the converter circuit of Figure 1 was not designed specifically for use in ISDN terminals, with some modifications it can be used in these applications. Since CMOS logic circuits consume power only during switching transitions, the first modification which is recommended is to decrease the switching frequency. The coupled inductor, L_2, can be operated at 40 to 50 kHz (change R_3 from 150 kΩ to 390 kΩ) without a redesign. Decreasing the frequency further requires a larger core size.

A second circuit modification which is recommended is to increase the resistances used in the voltage divider network (R_5 and R_6). The values used in the 1 W converter will dissipate $(10)^2/(18\ k\Omega + 12\ k\Omega) = 3.33$ mW. This loss is negligible for the 1 W converter, but it is nearly one fourth of the budgeted power loss for the ISDN supply during the emergency power-down state. Setting R_5 = 51.1 kΩ and R_6 = 34.0 kΩ reduces the voltage divider dissipation to 1.2 mW. With these two minor changes the flyback converter meets the efficiency specifications of Table I. Figure 8 illustrates the efficiency improvement at light load levels which results from the circuit changes outlined above.

Other Si9100 Applications Circuits

The Si9100 has been called a "One Watt High-Voltage Switchmode Regulator" in order to describe its most appropriate type of application--low power converters. The device is not, however, limited to 1 W designs. Figure 9 shows the maximum achievable output power as a function of minimum input voltage for several types of converters, two of which are discussed below.

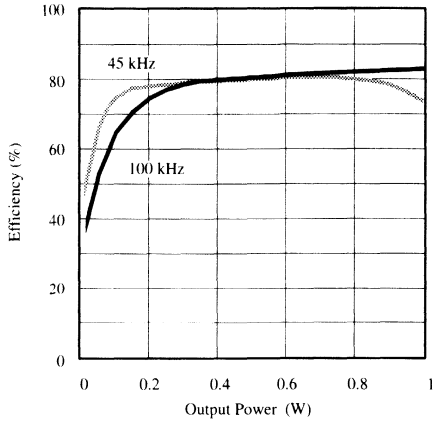


Figure 8. Efficiency vs. load curves for the flyback converter

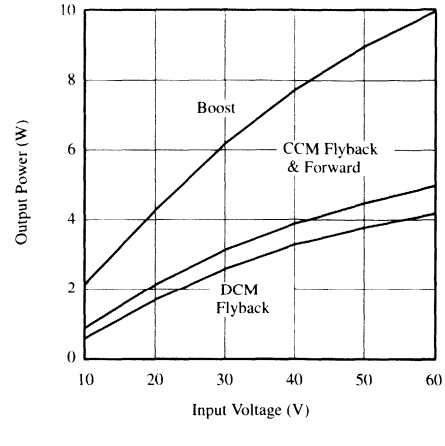


Figure 9. Maximum output power vs. minimum input voltage

Other Si9100 Applications Circuits

The Si9100 has been called a "One Watt High-Voltage Switchmode Regulator" in order to describe its most appropriate type of application--low power converters. The device is not, however, limited to 1 W designs. Figure 9 shows the maximum achievable output power as a function of minimum input voltage for several types of converters, two of which are discussed below.

CCM Flyback Converter

By redesigning the magnetics for continuous conduction, the flyback circuit of Figure 1 can be made to provide 3 W of output power. Operation in the continuous conduction mode (CCM) introduces a right-half-plane (RHP) zero into the control-to-output transfer function of the power stage. The RHP zero incurs a phase lag without the corresponding gain rolloff caused by left-half-plane poles, and lead compensation cannot be used. Instead, the gain must be rolled off to unity (0 dB) below the RHP zero frequency. The continuous-mode flyback will, therefore, have a slower dynamic response than the DCM flyback. Also, to maintain the same output ripple for the 3 W converter, it is necessary to increase the size of the output filter capacitors.

Forward Converter

Forward converters are not normally used for power supplies rated under 50 W, due to the additional cost of the output filter chokes. However, for 2 to 4 W converter applications requiring ultra-low ripple, the cost of the additional inductor may be warranted. One such application is low power instrumentation for avionics.

The forward converter of Figure 10 was designed to operate from 28-V aircraft power (MIL-STD-704D) to provide 2.5 W at 80% efficiency. A single core with multiple windings has been used to decrease cost and board space required for the output filter inductors. The input voltage range is 18 to 32 V_{DC}; regulation is 5%; and the switching frequency is 100 kHz. Measured peak-to-peak voltage ripple was 8 mV for the +15-V output, 4 mV for the −15-V output, and 13 mV for the +5-V output, at maximum load.

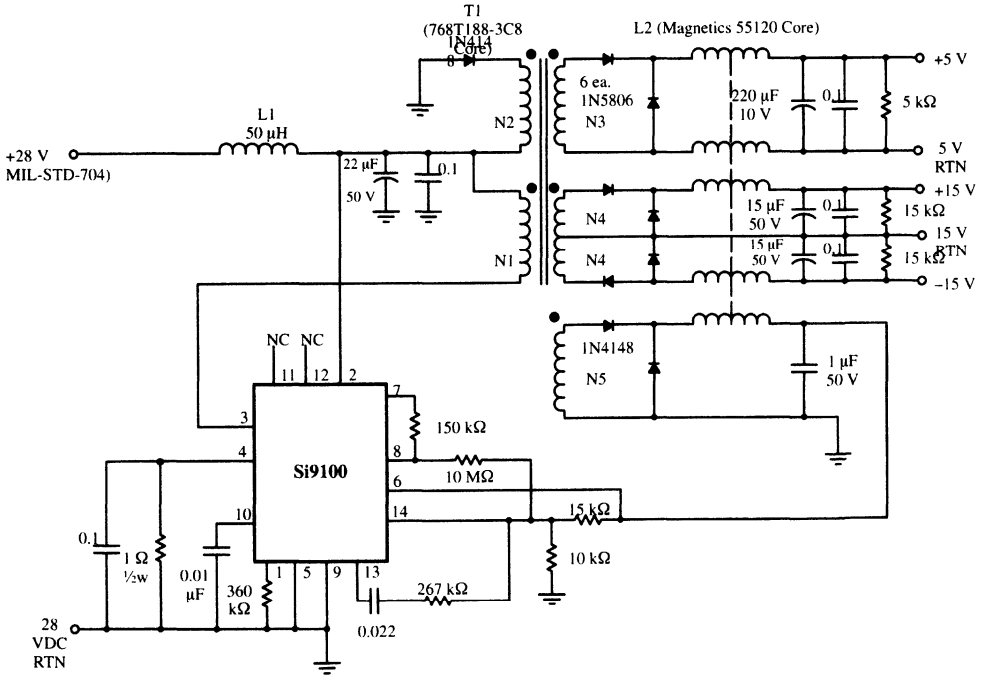


Figure 10. 2.5 W Forward Converter Using the Si9100

Toroidal cores were used for both the transformer and the coupled output inductor to achieve very low leakage inductance. The transformer winding data is as follows:

Core - Ferroxcube #768T188-3C8

Windings - N1 = 31 turns (AWG26)
N2 = 31 turns (AWG34)
N3 = 22 turns (AWG32)
N4 = 64 turns (AWG32)
N5 = 43 turns (AWG34)

The primary and clamp windings are placed on the core first, wound bifilar to minimize leakage inductance. The +5-V output is wound next, followed by the ± 15-V outputs wound bifilar. The 10-V winding was placed on the outside. Each winding is spread over the entire circumference of the toroidal core for optimum magnetic coupling.

Coupled inductors must have the same turns ratios as the transformer secondaries or high circulating currents result in very high output ripple. The coupled inductor, L_2, is a molypermalloy powder (MPP) toroid (Magnetics #55120) with three times the number of turns as each of the T1 secondaries. The inductor winding data is as follows:

+5 V – 66 turns (AWG30)
±15 V – 192 turns (AWG30)
–15 V – 192 turns (AWG34)
+10 V – 129 turns (AWG34)

It should be mentioned here that MIL-STD-461 EMI testing was not performed for this supply. To meet CE03 and CS01 limits, some input filter redesign is required. Although current-mode control exhibits excellent audio-susceptibility performance, it is still necessary to damp the input filter to reduce peaking of its output impedance at the resonant frequency (Reference 3 provides useful design information regarding these requirements).

References

1) Rosenbaum, D. and Stolp, K. H., "The Feeding Conception of the ISDN Basic Access," IEEE Intelec Conference, Munich, FRG, Oct 14-17, 1985, pp. 505-512.

2) Krautkramer, W. and Schickling, B., "Remote Power Feeding of ISDN Terminals at the Basic Access," IEEE Intelec Conference, Munich, FRG, Oct 14-17,1985, pp. 513-519.

3) Middlebrook, R. D., "Input Filter Considerations in Design and Application of Switching Regulators," IEEE Industry Applications Society Annual Meeting, Oct. 11-14, 1976.

Appendix A: Flyback Inductor Design

Inductance Calculation

The first step is to calculate the maximum primary inductance for discontinuous conduction at maximum load. Input power to the coupled inductor is approximately:

$$P_{IN} = \frac{1W}{0.8} = 1.25\ W \qquad (1)$$

Input power is also equal to the product of the stored energy in the magnetic field times the switching frequency:

$$P_{IN} = \tfrac{1}{2} L_P (I_{pk})^2 \bullet f_S \qquad (2)$$

The minimum primary current slope occurs at the minimum input voltage condition.

$$\left.\frac{di}{dt}\right|_{MIN} = \frac{V_{IN(MIN)}}{L_{P(MAX)}}$$

If a maximum duty ratio of 0.45 is assumed, then the minimum current peak is given by:

$$I_{pk} \le \left.\frac{di}{dt}\right|_{MIN} \times 0.45\ T_S$$

or

$$I_{pk} \le \frac{V_{IN(MIN)}}{L_{P(MAX)}} \times 0.45\ T_S \qquad (3)$$

Combining equations 2 and 3 gives:

$$P_{IN(MAX)} = \frac{1}{2} L_{P(MAX)}\ I_{pk(MIN)}{}^2 \times f_S$$

$$= \frac{1}{2} L_{P(MAX)} \left(\frac{V_{IN(MIN)}}{L_{P(MAX)}}\right)^2 (0.45\ T_S)^2 f_S$$

$$= \frac{1}{2} \frac{V_{IN(MIN)}{}^2}{L_{P(MAX)}} \times (0.45\ T_S)^2\ f_S$$

$$\therefore L_{P(MAX)} = \frac{1}{2} \frac{V_{IN(MIN)}{}^S}{P_{IN(MAX)}} \times (0.45\ T_S)^2 f_S$$

$$= \frac{1}{2} \frac{(15)^2}{1.25} \times (0.45\ T_S)^2\ 10^5 = 182\ \mu H$$

To allow for component tolerances choose a nominal primary inductance of 150 µH. Equation 2 then gives $I_{pk} \approx 0.4$ A.

Core Selection

The area product method was used to determine the inductor core size. Refer to "Magnetic Core Selection for Transformers and Inductors" by McLyman, for more information on magnetics design methods (Marcel Dekker, Inc., 1982).

$$A_P = \left(\frac{2\ E \times 10^4}{B_m \times K_u \times K_j}\right)^{1.14}$$

where:

E = Core energy storage requirement
B_m = Maximum flux density
K_u = Window utilization factor
K_j = Current density coefficient

$$E = \tfrac{1}{2} L_P I_{pk}{}^2$$

Let $B_m = 1500$, gauss = 0.15 tesla, and $K_u = 0.10$

$$A_P = \frac{2 \times \frac{1}{2} \times 150 \times 10^{-6}(0.4)^2\ 10^4}{0.15\ (0.10)\ (433)}$$

$$= 0.0233\ cm^4$$

Since the empirical equation given above applies for the area product of simple one-winding inductors, multiply by 2 for a coupled inductor. All of the secondaries combined will handle the same energy as the primary, and can therefore be allotted equal portions of the window area. The area product requirement is thus:

$$A_P = 2 \bullet 0.0233\ cm^4 = 0.0466\ cm^4$$

The EP-13 core has an area product of 0.049 cm^4, which meets this requirement. Also, this EP core can be tube-loaded for automatic insertion in high volume manufacturing applications, and is available from multiple sources (Siemens, TDK, and Amperex Ferroxcube).

Core A_L Value Determination

The number of primary turns is found from:

$$L = \frac{N_P \Phi}{I_{pk}} = \frac{N_P B_M A_C}{I_{pk}}$$

Limiting the peak flux density to 0.15 Tesla gives:

$$N_P = \frac{L_P I_{pk}}{B_M A_C} = \frac{(150 \times 10^{-6})(0.4) \times 10^4}{(0.15)(0.195\ cm^2)}$$

$$= 20.5\ turns \simeq 21\ turns$$

This gives the following value for A_L:

$$A_L = \left(\frac{1000}{21}\right)^2 (150 \times 10^{-6}) = 340 \text{ mH per 1000 turns}$$

Secondary Turns Calculation

The core flux is reset to zero during the off time for each switching cycle. To guarantee discontinuous conduction mode at the maximum load condition, it is necessary to limit the inductance of the secondary windings to some maximum value. Worst case conditions occur at the maximum switching frequency (110 kHz) and maximum A_L value (374 mH/1000 turns for 10 % tolerance). The voltage across N_{S1} during the diode conduction interval is $V_O + V_D$= 5.0 + 0.5 = 5.5 V, and the negative current slope is

$$\frac{di}{dt} = \frac{I_{S1}}{d_{REC}} = \frac{V_O + V_D}{L_{S1}}$$

where I_{S1} is the peak current in the N_{S1} winding, t_{REC} is the conduction time of CR2, and L_{S1} is the inductance of N_{S1}. The rectifier conduction duty ratio is defined as:

$$d_r = \frac{t_{REC}}{T_S}$$

The load current is related to the peak secondary current and duty ratio by the equation:

$$I_{S1} = \frac{2 \times I_O}{d_r}$$

Combining these equations solves for the rectifier conduction duty ratio in terms of load current, inductance, and output voltage.

$$d_r = \sqrt{\frac{2 \times I_O \times L_{S1}}{(V_O + V_D) \times T_S}}$$

Setting the duty ratio < 0.45 gives:

$$d_r = \frac{2(0.167) \times L_{S1}}{5.5\ (9.09)\ 10^{-6}} \leq 0.45$$

Therefore, L_{S1} < 30.3 µH. Since $AL_{(MAX)}$ = 374 mH/1000 turns,

$$L_{S1} = \frac{N_{S1}}{5.5 \text{ V}} \qquad 2$$

Use $N_{S1} = N_{S2}$ = 8 turns:

$$N_{S3} = (10 \text{ V} + 0.7 \text{ V}) \frac{N_{S1}}{5.5 \text{ V}}$$

$$= 15.6 \text{ turns} \simeq 16 \text{ turns}$$

Winding Order

The primary winding (1-2) is placed first over the bobbin using one strand of AWG31 magnet wire (21 turns). The highest current secondary (3-4) is wound over the primary using two strands of AWG31 (8 turns). The 10-V sense winding (7-8) is put down next, using one strand of AWG36 (16 turns). The –5-V output (5-6) is wound last using one strand of AWG31 wire (8 turns).

Appendix B: Si9100 Flyback Converter Parts List

U1	Si9100
L1	Inductor, 100 µH @ 75 mA dc
L2	Coupled Inductor, GFS Mfg. # 85-787-4*
C1	20 µF, 100 V, Aluminum Electrolytic, Sprague # 30D+TE1409
C2, C3, C6, C8	0.1 µF ceramic
C4	0.022 µF ceramic
C7	100 µF, 10 V, tantalum, Sprague # 196D107X9010P
C9	20 µF, 10 V, tantalum, Sprague # 196D226X9010J
C5	1 µF, 50 V, WIMA MKS2
CR1	1N4148
CR2, CR3	1N5819, Schottky rectifier
R1	390 kΩ, $^1/_4$ W Carbon
R2	1 Ω, $^1/_2$ W Carbon
R3	150 kΩ, $^1/_4$ W Carbon
R4	240 kΩ, $^1/_4$ W Carbon
R5	18 kΩ, $^1/_4$ W Carbon
R6	12 kΩ, $^1/_4$ W Carbon

* GFS Manufacturing Company, 21 Crosby Road, Dver, NH, USA 03820-1409

3-W High-Voltage Switchmode Regulator

Features

- 10- to 120-V Input Range
- Current-Mode Control
- On-chip 200-V, 7-Ω MOSFET Switch
- $\overline{\text{SHUTDOWN}}$ and RESET
- High Efficiency Operation (> 80%)
- Internal Start-Up Circuit
- Internal Oscillator (1 MHz)

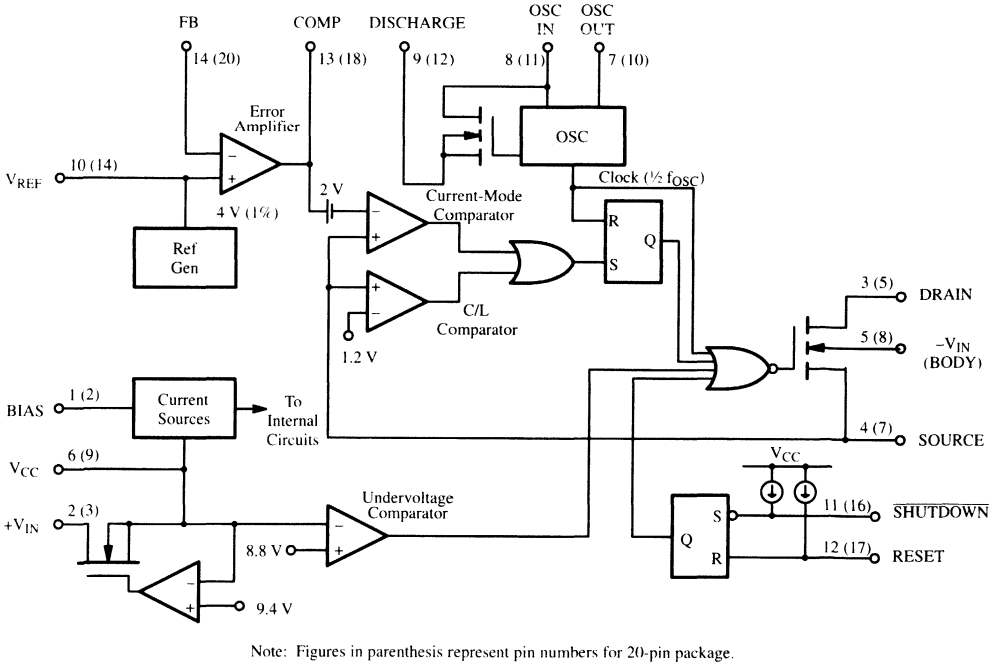
Description

The Si9102 high-voltage switchmode regulator is a monolithic BiC/DMOS integrated circuit which contains most of the components necessary to implement a high-efficiency dc-to-dc converter up to 3 watts. It can either be operated from a low-voltage dc supply, or directly from a 10- to 120-V unregulated dc power source.

This device may be used with an appropriate transformer to implement most single-ended isolated power converter topologies (i.e., flyback and forward).

The Si9102 is available in 14-pin plastic DIP and 20-pin PLCC packages, and is specified over the D suffix (–40 to 85°C) temperature range.

Functional Block Diagram



Note: Figures in parenthesis represent pin numbers for 20-pin package.

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70001.

Absolute Maximum Ratings

Voltages Referenced to $-V_{IN}$ ($V_{CC} < +V_{IN} + 0.3$ V)
V_{CC} ..... 15 V
$+V_{IN}$ ..... 120 V
V_{DS} ..... 200 V
I_D (Peak) (Note: 300 µs pulse, 2% duty cycle) ..... 2 A
I_D (rms) ..... 250 mA
Logic Inputs (RESET, $\overline{\text{SHUTDOWN}}$, OSC IN) ..... –0.3 V to V_{CC} + 0.3 V
Linear Inputs
(FEEDBACK, SOURCE) ..... –0.3 V to 7 V
HV Pre-Regulator Input Current (continuous) ..... 3 mA
Storage Temperature ..... –65 to 125°C
Operating Temperature ..... –40 to 85°C
Junction Temperature (T_J) ..... 150°C
Power Dissipation (Package)a
14-Pin Plastic DIP (J Suffix)[b] ..... 750 mW
20-Pin PLCC (N Suffix)[c] ..... 1400 mW
Thermal Impedance (Θ_{JA})
14-Pin Plastic DIP ..... 167°C/W
20-Pin PLCC ..... 90°C/W

Notes
a. Device mounted with all leads soldered or welded to PC board.
b. Derate 6 mW/°C above 25°C
c. Derate 11.2 mW/°C above 25°C

Recommended Operating Range

Voltages Referenced to $-V_{IN}$
V_{CC} ..... 9.5 V to 13.5 V
R_{OSC} ..... 25 kΩ to 1 MΩ
Linear Inputs ..... 0 to 7 V
$+V_{IN}$ ..... 10 V to 120 V
f_{OSC} ..... 40 kHz to 1 MHz
Digital Inputs ..... 0 to V_{CC}

Specifications[a]

Parameter	Symbol	Test Conditions Unless Otherwise Specified DISCHARGE = $-V_{IN}$ = 0 V V_{CC} = 10 V, $+V_{IN}$ = 48 V R_{BIAS} = 390 kΩ, R_{OSC} = 330 kΩ	Temp[b]	Limits D Suffix –40 to 85°C Min[d]	Typ[c]	Max[d]	Unit
Reference							
Output Voltage	V_R	OSC IN = – V_{IN} (OSC Disabled) R_L = 10 MΩ	Room Full	3.92 3.86	4.0	4.08 4.14	V
Output Impedance[e]	Z_{OUT}		Room	15	30	45	kΩ
Short Circuit Current	I_{SREF}	$V_{REF} = -V_{IN}$	Room	70	100	130	µA
Temperature Stability[e]	T_{REF}		Full		0.5	1.0	mV/°C
Oscillator							
Maximum Frequency[e]	f_{MAX}	R_{OSC} = 0	Room	1	3		MHz
Initial Accuracy	f_{OSC}	R_{OSC} = 330 kΩ[g]	Room	80	100	120	kHz
		R_{OSC} = 150 kΩ[g]	Room	160	200	240	
Voltage Stability	Δf/f	Δf/f = f(13.5 V) – f(9.5 V)/f(9.5 V)	Room		10	15	%
Temperature Coefficient[e]	T_{OSC}		Full		200	500	ppm/°C
Error Amplifier							
Feedback Input Voltage	V_{FB}	FB Tied to COMP OSC IN = – V_{IN} (OSC Disabled)	Room	3.96	4.00	4.04	V
Input BIAS Current	I_{FB}	OSC IN = – V_{IN}, V_{FB} = 4 V, OSC IN = – V_{IN} (OSC Disabled)	Room		25	500	nA
Open Loop Voltage Gain[e]	A_{VOL}		Room	60	80		dB
Unity Gain Bandwidth[e]	BW		Room	0.7	1		MHz
Dynamic Output Impedance[e]	Z_{OUT}		Room		1000	2000	Ω

Specifications[a]

Parameter	Symbol	Test Conditions Unless Otherwise Specified DISCHARGE = $-V_{IN}$ = 0 V V_{CC} = 10 V, $+V_{IN}$ = 48 V R_{BIAS} = 390 kΩ, R_{OSC} = 330 kΩ	Temp[b]	Limits D Suffix −40 to 85°C Min[d]	Typ[c]	Max[d]	Unit
Error Amplifier (Cont'd)							
Output Current	I_{OUT}	Source (V_{FB} = 3.4 V)	Room		−2.0	−1.4	mA
Input OFFSET Voltage	V_{OS}	OSC IN = − V_{IN} (OSC Disabled)	Room		± 15	± 40	mV
Output Current	I_{OUT}	Sink (V_{FB} = 4.5 V)	Room	0.12	0.15		mA
Power Supply Rejection	PSRR	9.5 V ≤ V_{CC} ≤ 13.5 V	Room	50	70		dB
Current Limit							
Threshold Voltage	V_{SOURCE}	R_L = 100 Ω from DRAIN to V_{CC} V_{FB} = 0 V	Room	1.0	1.2	1.4	V
Delay to Output[e]	t_d	R_L = 100 Ω from DRAIN to V_{CC} V_{SOURCE} = 1.5 V, See Figure 1	Room		100	200	ns
Pre-Regulator/Start-Up							
Input Voltage	$+V_{IN}$	I_{IN} = 100 µA	Room			120	V
Input Leakage Current	$+I_{IN}$	V_{CC} ≥ 10 V	Room			10	µA
Pre-Regulator Start-Up Current	I_{START}	Pulse Width ≤ 300 µs, V_{CC} = 7 V	Room	8	15		mA
V_{CC} Pre-Regulator Turn-Off Threshold Voltage	V_{REG}	$I_{PRE-REGULATOR}$ = 10 µA	Room	7.8	9.4	9.7	V
Undervoltage Lockout	V_{UVLO}	R_L = 100 Ω from DRAIN to V_{CC} See Detailed Description	Room	7.0	8.8	9.2	
V_{REG}, $-V_{UVLO}$	V_{DELTA}		Room	0.3	0.6		
Supply							
Supply Current	I_{CC}		Room	0.45	0.6	1.0	mA
Bias Current	I_{BIAS}		Room	10	15	20	µA
Logic							
$\overline{\text{SHUTDOWN}}$ Delay[e]	t_{SD}	V_{SOURCE} = $-V_{IN}$, See Figure 2	Room		50	100	ns
$\overline{\text{SHUTDOWN}}$ Pulse Width[e]	t_{SW}	See Figure 3	Room	50			
RESET Pulse Width[e]	t_{RW}		Room	50			
Latching Pulse Widthe $\overline{\text{SHUTDOWN}}$ and RESET Low	t_{LW}		Room	25			
Input Low Voltage	V_{IL}		Room			2.0	V
Input High Voltage	V_{IH}		Room	8.0			
Input Current Input Voltage High	I_{IH}	V_{IN} = 10 V	Room		1	5	µA
Input Current Input Voltage Low	I_{IL}	V_{IN} = 0 V	Room	−35	−25		

Specifications[a]

Parameter	Symbol	Test Conditions Unless Otherwise Specified DISCHARGE = $-V_{IN}$ = 0 V V_{CC} = 10 V, $+V_{IN}$ = 48 V R_{BIAS} = 390 kΩ, R_{OSC} = 330 kΩ	Temp[b]	Limits D Suffix −40 to 85°C Min[d]	Typ[c]	Max[d]	Unit
MOSFET Switch							
Breakdown Voltage	$V_{BR(DSS)}$	I_{DRAIN} = 100 µA	Full	200	220		V
Drain-Source On Resistance[f]	$r_{DS(on)}$	I_{DRAIN} = 100 mA	Room			7	Ω
Drain Off Leakage Current	I_{DSS}	V_{DRAIN} = 100 V	Room		5	10	µA
Drain Capacitance	C_{DS}		Room		35		pF

Notes
a. Refer to PROCESS OPTION FLOWCHART for additional information.
b. Room = 25°C, Full = as determined by the operating temperature suffix.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
e. Guaranteed by design, not subject to production test.
f. Temperature coefficient of $r_{DS(on)}$ is 0.75% per °C, typical.
g. C_{STRAY} Pin 8 = ≤ 5 pF

Timing Waveforms

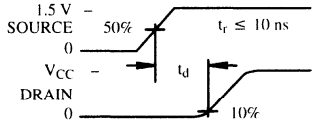


Figure 1.

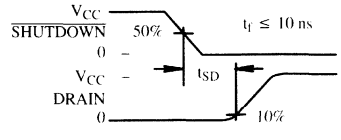


Figure 2.

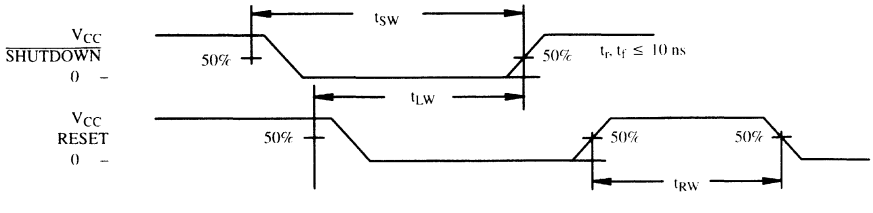
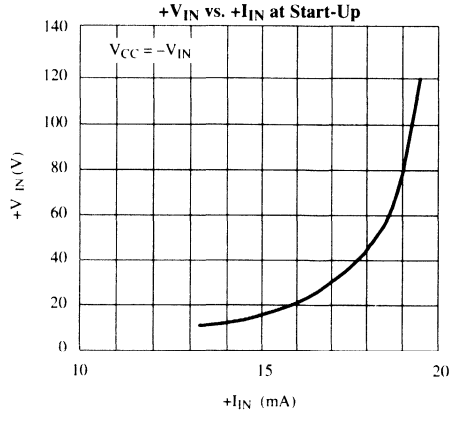
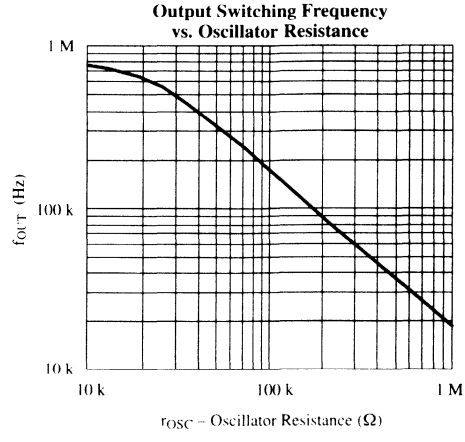


Figure 3.

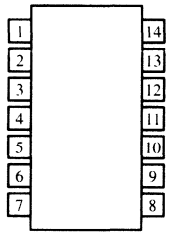
Typical Characteristics





Pin Configurations

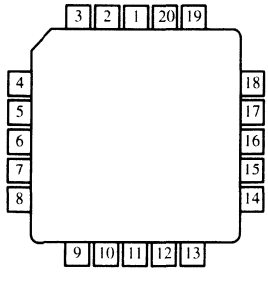
PDIP-14



Top View

Order Number
Plastic DIP: Si9102DJ02

PLCC-20



Top View

Order Number
Plastic PLCC: Si9102DN02

Function	Pin	
	14-Pin DIP	20-Pin PLCC*
BIAS	1	2
$+V_{IN}$	2	3
DRAIN	3	5
SOURCE	4	7
$-V_{IN}$	5	8
V_{CC}	6	9
OSC OUT	7	10
OSC IN	8	11
DISCHARGE	9	12
V_{REF}	10	14
SHUTDOWN	11	16
RESET	12	17
COMP	13	18
FB	14	20
*Pins 1, 4, 6, 13, 15, and 19 = N/C		

Detailed Description

Pre-Regulator/Start-Up Section

Due to the low quiescent current requirement of the Si9102 control circuitry, bias power can be supplied from the unregulated input power source, from an external regulated low-voltage supply, or from an auxiliary "bootstrap" winding on the output inductor or transformer.

When power is first applied during start-up, $+V_{IN}$ will draw a constant current. The magnitude of this current

is determined by a high-voltage depletion MOSFET device which is connected between $+V_{IN}$ and V_{CC}. This start-up circuitry provides initial power to the IC by charging an external bypass capacitance connected to the V_{CC} pin. The constant current is disabled when V_{CC} exceeds 9.4 V. If V_{CC} is not forced to exceed the 9.4-V threshold, then V_{CC} will be regulated to a nominal value of 9.4 V by the pre-regulator circuit.

As the supply voltage rises toward the normal operating conditions, an internal undervoltage (UV) lockout circuit keeps the output MOSFET disabled until V_{CC} exceeds the undervoltage lockout threshold (typically 8.8-V). This guarantees that the control logic will be functioning properly and that sufficient gate drive voltage is available before the MOSFET turns on. The design of the IC is such that the undervoltage lockout threshold will not exceed the pre-regulator turn-off voltage. Power dissipation can be minimized by providing an external power source to V_{CC} such that the constant current source is always disabled.

Note: During start-up or when V_{CC} drops below 9.4-V the start-up circuit is capable of sourcing up to 20 mA. This may lead to a high level of power dissipation in the IC (for a 48-V input, approximately 1 W). Excessive start-up time caused by external loading of the V_{CC} supply can result in device damage. Figure 4 gives the typical pre-regulator current at start-up as a function of input voltage.

BIAS

To properly set the bias for the Si9102, a 390-kΩ resistor should be tied from BIAS to $-V_{IN}$. This determines the magnitude of bias current in all of the analog sections and the pull-up current for the $\overline{\text{SHUTDOWN}}$ and RESET pins. The current flowing in the bias resistor is nominally 15 µA.

Reference Section

The reference section of the Si9102 consists of a temperature compensated buried zener and trimmable divider network. The output of the reference section is connected internally to the non-inverting input of the error amplifier. Nominal reference output voltage is 4 V. The trimming procedure that is used on the Si9102 brings the output of the error amplifier (which is configured for unity gain during trimming) to within ± 1% of 4 V. This automatically compensates for the input offset voltage in the error amplifier.

The output impedance of the reference section has been purposely made high so that a low impedance external voltage source can be used to override the internal voltage source, if desired, without otherwise altering the performance of the device.

Error Amplifier

Closed-loop regulation is provided by the error amplifier, which is intended for use with "around-the-amplifier" compensation. A MOS differential input stage provides for low input current. The noninverting input to the error amplifier (V_{REF}) is internally connected to the output of the reference supply and should be bypassed with a small capacitor to ground.

Oscillator Section

The oscillator consists of a ring of CMOS inverters, capacitors, and a capacitor discharge switch. Frequency is set by an external resistor between the OSC in and OSC out pins. (See Figure 5 for details of resistor value vs. frequency.) The DISCHARGE pin should be tied to $-V_{IN}$ for normal internal oscillator operation. A frequency divider in the logic section limits switch duty cycle to ≤ 50% by locking the switching frequency to one half of the oscillator frequency.

Remote synchronization can be accomplished by capacitive coupling of a synchronization pulse into the OSC IN terminal. For a 5-V pulse amplitude and 0.5-µs pulse width, typical values would be 100 pF in series with 3 kΩ to OSC IN.

Detailed Description (Cont'd)

$\overline{\text{SHUTDOWN}}$ and RESET

$\overline{\text{SHUTDOWN}}$ and RESET are intended for overriding the output MOSFET switch via external control logic. The two inputs are fed through a latch preceding the output switch. Depending on the logic state of RESET, $\overline{\text{SHUTDOWN}}$ can be either a latched or unlatched input. The output is off whenever $\overline{\text{SHUTDOWN}}$ is low. By simultaneously having $\overline{\text{SHUTDOWN}}$ and RESET low, the latch is set and $\overline{\text{SHUTDOWN}}$ has no effect until RESET goes high. The truth table for these inputs is given in Table 1.

Both pins have internal current source pull-ups and should be left disconnected when not in use. An added feature of the current sources is the ability to connect a capacitor and an open-collector driver to the $\overline{\text{SHUTDOWN}}$ or RESET pins to provide variable shutdown time.

Table 1. Truth Table for the $\overline{\text{SHUTDOWN}}$ and RESET Pins

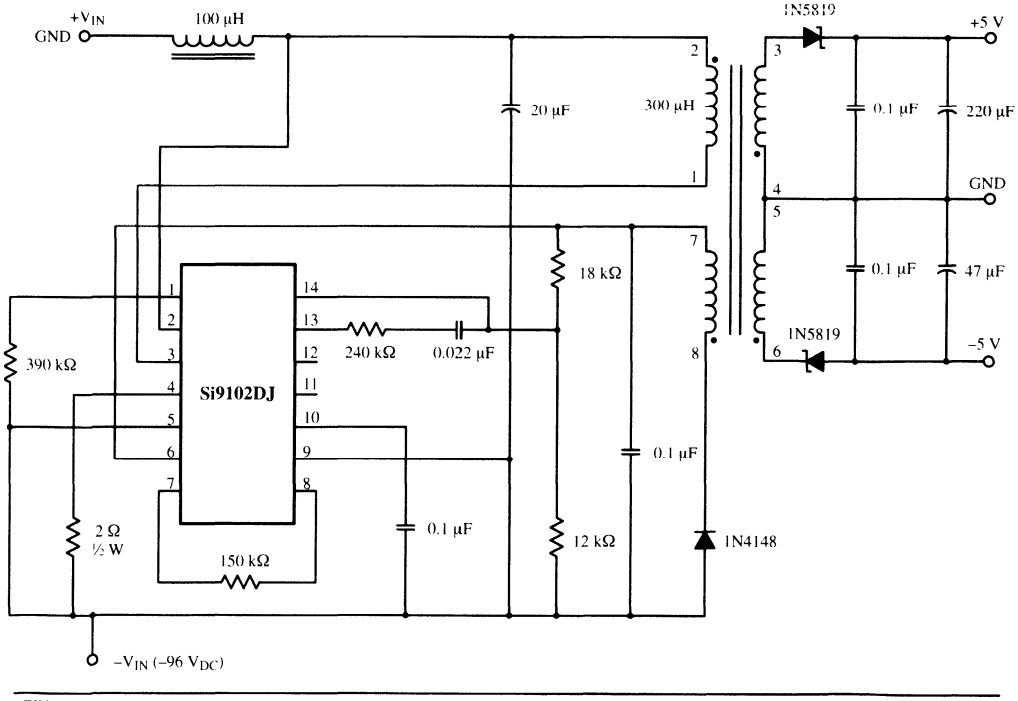
$\overline{\text{SHUTDOWN}}$	RESET	Output
H	H	Normal Operation
H	↓	Normal Operation (No Change)
L	H	Off (Not Latched)
L	L	Off (Latched)
↓	L	Off (Latched, No Change)

Output Switch

The output switch is a 7-Ω , 200-V lateral DMOS device. Like discrete MOSFETs, the switch contains an intrinsic body-drain diode. However, the body contact in the Si9102 is connected internally to $-V_{IN}$ and is independent of the SOURCE.

Applications

Flyback Converter for Double Battery Telecommunications Power Supplies



High-Voltage Switchmode Regulator

Features

- 10- to 120-V Input Range
- Current-Mode Control
- On-Chip 200-V, 5-Ω MOSFET Switch
- $\overline{\text{SHUTDOWN}}$ and RESET
- High Efficiency Operation (>80%)
- Internal Start-Up Circuit
- Internal Oscillator (1 MHz)

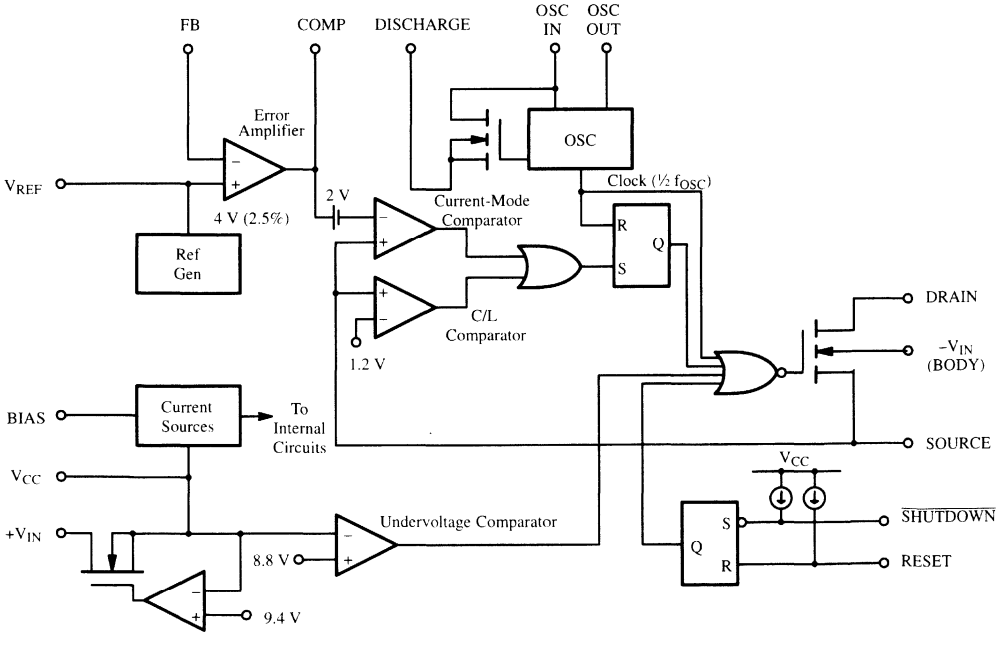
Description

The Si9104 high-voltage switchmode regulator is a monolithic BiC/DMOS integrated circuit which contains most of the components necessary to implement a high-efficiency dc-to-dc converter up to 3 watts. It can either be operated from a low-voltage dc supply, or directly from a 10- to 120-V unregulated dc power source.

This device may be used with an appropriate transformer to implement most single-ended isolated power converter topologies (i.e., flyback and forward).

The Si9104 is available in a 16-pin wide-body SOIC and is specified over the D suffix (–40 to 85°C) temperature range.

Functional Block Diagram



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Absolute Maximum Ratings

Voltages Referenced to $-V_{IN}$ ($V_{CC} < +V_{IN} + 0.3$ V)
V_{CC} ..... 15 V
$+V_{IN}$ ..... 120 V
V_{DS} ..... 200 V
I_D (Peak) (300 µs pulse, 2% duty cycle) ..... 2 A
I_D (rms) ..... 250 mA
Logic Inputs (RESET, $\overline{\text{SHUTDOWN}}$, OSC IN) ..... -0.3 V to $V_{CC} + 0.3$ V
Linear Inputs (FEEDBACK, SOURCE) ..... -0.3 V to 7 V
HV Pre-Regulator Input Current (continuous) ..... 3 mA

Storage Temperature ..... –65 to 125°C
Operating Temperature ..... –40 to 85°C
Junction Temperature (T_J) ..... 150°C
Power Dissipation (Package)[a]
16-Pin Plastic Wide-Body SOIC[b] ..... 900 mW
Thermal Impedance (Θ_{JA})
16-Pin Plastic Wide-Body SOIC ..... 140°C/W

Notes
a. Device mounted with all leads soldered or welded to PC board.
b. Derate 7.2 mW/°C above 25°C.

Recommended Operating Range

Voltages Referenced to $-V_{IN}$
V_{CC} ..... 10 V to 13.5 V
$+V_{IN}$ ..... 10 V to 120 V
f_{OSC} ..... 40 kHz to 1 MHz

R_{OSC} ..... 25 kΩ to 1 MΩ
Linear Inputs ..... 0 to 7 V
Digital Inputs ..... 0 to V_{CC}

Specifications[a]

Parameter	Symbol	Test Conditions Unless Otherwise Specified DISCHARGE = $-V_{IN}$ = 0 V, V_{CC} = 10 V $+V_{IN}$ = 48 V, R_{BIAS} = 390 kΩ R_{OSC} = 330 kΩ	Temp[b]	Limits D Suffix –40 to 85°C Min[d]	Typ[c]	Max[d]	Unit
Reference							
Output Voltage	V_R	OSC IN = $-V_{IN}$ (OSC Disabled) R_L = 10 MΩ	Room Full	3.92 3.85	4.0	4.08 4.15	V
Output Impedance[e]	Z_{OUT}		Room	15	30	45	kΩ
Short Circuit Current	I_{SREF}	$V_{REF} = -V_{IN}$	Room	70	100	130	µA
Temperature Stability[e]	T_{REF}		Full		0.25	1.0	mV/°C
Long Term Stability[e]		t = 1000 hrs., T_A = 125°C	Room		5	25	mV
Oscillator							
Maximum Frequency[e]	f_{MAX}	R_{OSC} = 0	Room	1	3		MHz
Initial Accuracy	f_{OSC}	R_{OSC} = 330 kΩ [f]	Room	80	100	120	kHz
		R_{OSC} = 150 kkΩ [f]	Room	160	200	240	
Voltage Stability	Δf/f	Δf/f = f(13.5 V) – f(10 V) / f(10 V)	Room	4	10	15	%
Temperature Coefficient[e]	T_{OSC}		Full		200	500	ppm/°C

1 Power Conversion

Specifications[a]

Parameter	Symbol	Test Conditions Unless Otherwise Specified DISCHARGE = $-V_{IN}$ = 0 V, V_{CC} = 10 V $+V_{IN}$ = 48 V, R_{BIAS} = 390 kΩ R_{OSC} = 330 kΩ	Temp[b]	Limits D Suffix –40 to 85°C Min[d]	Typ[c]	Max[d]	Unit
Error Amplifier							
Feedback Input Voltage	V_{FB}	FB Tied to COMP OSC IN = – V_{IN} (OSC Disabled)	Room	3.96	4.00	4.04	V
Input BIAS Current	I_{FB}	OSC IN = – V_{IN}, V_{FB} = 4 V	Room		25	500	nA
Input OFFSET Voltage	V_{OS}	OSC IN = – V_{IN} (OSC Disabled)	Room		± 15	± 40	mV
Open Loop Voltage Gain[e]	A_{VOL}		Room	60	80		dB
Unity Gain Bandwidth[e]	BW		Room	0.7	1		MHz
Dynamic Output Impedance[e]	Z_{OUT}		Room		1000	2000	Ω
Output Current	I_{OUT}	Source (V_{FB} = 3.4 V)	Room		–2.0	–1.4	mA
		Sink (V_{FB} = 4.5 V)	Room	0.12	0.15		
Power Supply Rejection	PSRR	10 V ≤ V_{CC} ≤ 13.5 V	Room	50	70		dB
Current Limit							
Threshold Voltage	V_{SOURCE}	R_L = 100 Ω from DRAIN to V_{CC}, V_{FB} = 0 V	Room	1.0	1.2	1.4	V
Delay to Output[e]	t_d	R_L = 100 Ω from DRAIN to V_{CC} V_{SOURCE} = 1.5 V, See Figure 1	Room		100	200	ns
Pre-Regulator/Start-Up							
Input Voltage	$+V_{IN}$	I_{IN} = 100 µA	Room	120			V
Input Leakage Current	$+I_{IN}$	V_{CC} ≥ 10 V	Room			10	µA
Pre-Regulator Start-Up Current	I_{START}	Pulse Width ≤ 300 µs, V_{CC} = 7 V	Room	8	15		mA
V_{CC} Pre-Regulator Turn-Off Threshold Voltage	V_{REG}	$I_{PRE-REGULATOR}$ = 10 µA	Room	7.8	9.4	9.8	V
Undervoltage Lockout	V_{UVLO}	R_L = 100 Ω from DRAIN to V_{CC} See Detailed Description	Room	7.0	8.8	9.3	
V_{REG} – V_{UVLO}	V_{DELTA}		Room	0.3	0.6		
Supply							
Supply Current	I_{CC}		Room	0.45	0.6	1.0	mA
Bias Current	I_{BIAS}		Room	10	15	20	µA
Logic							
$\overline{\text{SHUTDOWN}}$ Delay[e]	t_{SD}	V_{SOURCE} = –V_{IN}, See Figure 2	Room		50	100	ns
$\overline{\text{SHUTDOWN}}$ Pulse Width[e]	t_{SW}	See Figure 3	Room	50			
RESET Pulse Width[e]	t_{RW}		Room	50			
Latching Pulse Width[e] $\overline{\text{SHUTDOWN}}$ and RESET Low	t_{LW}		Room	25			
Input Low Voltage	V_{IL}		Room			2.0	V
Input High Voltage	V_{IH}		Room	8.0			

Specifications[a]

Parameter	Symbol	Test Conditions Unless Otherwise Specified DISCHARGE = $-V_{IN}$ = 0 V, V_{CC} = 10 V $+V_{IN}$ = 48 V, R_{BIAS} = 390 kΩ, R_{OSC} = 330 kΩ	Temp[b]	Limits D Suffix –40 to 85°C Min[d]	Typ[c]	Max[d]	Unit
Logic (Cont'd)							
Input Current Input Voltage High	I_{IH}	$V_{IN} = V_{CC}$	Room		1	5	µA
Input Current Input Voltage Low	I_{IL}	V_{IN} = 0 V	Room	–35	–25		µA
MOSFET Switch							
Breakdown Voltage	$V_{BR(DSS)}$	I_{DRAIN} = 100 µA	Full	200	220		V
Drain-Source On-Resistance[g]	$r_{DS(on)}$	I_{DRAIN} = 100 mA	Room		3	5	Ω
Drain Off Leakage Current	I_{DSS}	V_{DRAIN} = 150 V	Room		5	10	µA
Drain Capacitance[e]	C_{DS}		Room		35		pF

Notes
a. Refer to PROCESS OPTION FLOWCHART for additional information.
b. Room = 25°C, Cold and Hot = as determined by the operating temperature suffix.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
e. Guaranteed by design, not subject to production test.
f. C_{STRAY} @ OSC IN ≤ 5 pF.
g. Temperature coefficient of $r_{DS(on)}$ is 0.75% per °C, typical.

Timing Waveforms

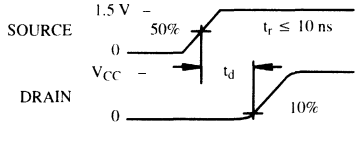


Figure 1.

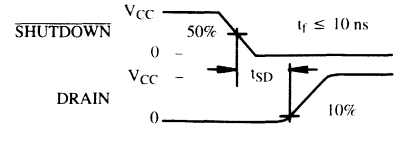


Figure 2.

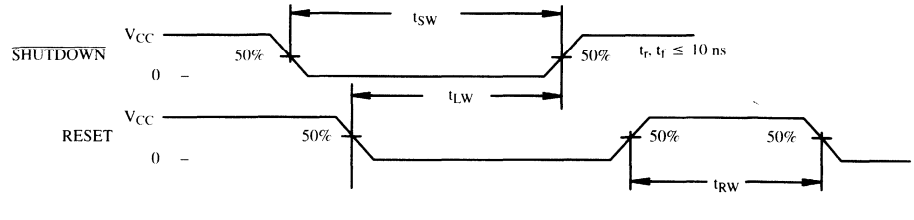
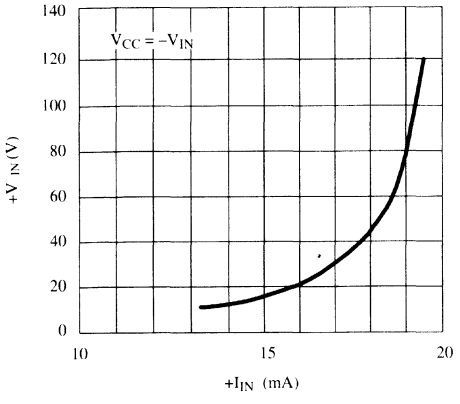


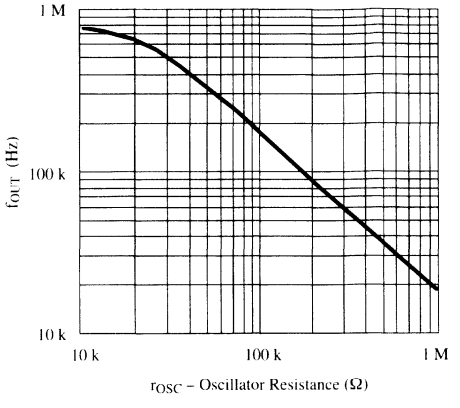
Figure 3.

Typical Characteristics

+V_{IN} vs. +I_{IN} at Start-Up

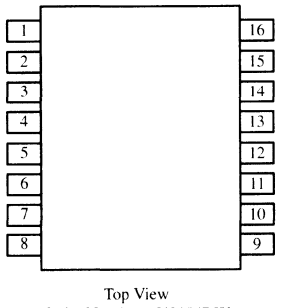


Output Switching Frequency vs. Oscillator Resistance



Pin Configurations

SO-16
(Wide-Body)



Top View
Order Number: Si9104DW

Pin Configurations (Cont'd)

Function	Pin Number		
	14-Pin Plastic DIP	16-Pin SOIC	20-Pin PLCC
SOURCE	4	1	7
$-V_{IN}$	5	2	8
V_{CC}	6	4	9
OSC_{OUT}	7	5	10
OSC_{IN}	8	6	11
DISCHARGE	9	7	12
V_{REF}	10	8	14
$\overline{\text{SHUTDOWN}}$	11	9	16
RESET	12	10	17
COMP	13	11	18
FB	14	12	20
BIAS	1	13	2
$+V_{IN}$	2	14	3
DRAIN	3	16	5
NC		3, 15	1, 4, 6, 13, 15, 19

Detailed Description

Pre-Regulator/Start-Up Section

Due to the low quiescent current requirement of the Si9104 control circuitry, bias power can be supplied from the unregulated input power source, from an external regulated low-voltage supply, or from an auxiliary "bootstrap" winding on the output inductor or transformer.

When power is first applied during start-up, $+V_{IN}$ will draw a constant current. The magnitude of this current is determined by a high-voltage depletion MOSFET device which is connected between $+V_{IN}$ and V_{CC}. This start-up circuitry provides initial power to the IC by charging an external bypass capacitance connected to the V_{CC} pin. The constant current is disabled when V_{CC} exceeds 9.4 V. If V_{CC} is not forced to exceed the 9.4-V threshold, then V_{CC} will be regulated to a nominal value of 9.4 V by the pre-regulator circuit.

As the supply voltage rises toward the normal operating conditions, an internal undervoltage (UV) lockout circuit keeps the output MOSFET disabled until V_{CC} exceeds the undervoltage lockout threshold (typically 8.8 V). This guarantees that the control logic will be functioning properly and that sufficient gate drive voltage is available before the MOSFET turns on. The design of the IC is such that the undervoltage lockout threshold will not exceed the pre-regulator turn-off voltage. Power dissipation can be minimized by providing an external power source to V_{CC} such that the constant current source is always disabled.

Note: During start-up or when V_{CC} drops below 9.4-V the start-up circuit is capable of sourcing up to 20 mA. This may lead to a high level of power dissipation in the IC (for a 48-V input, approximately 1 W). Excessive start-up time caused by external loading of the V_{CC} supply can result in device damage. For typical pre-regulator current at start-up as a function of input voltage see Typical Characteristics, "$+V_{IN}$ vs. $+I_{IN}$ at Start-Up" (page 1-66).

BIAS

To properly set the bias for the Si9104, a 390-kΩ resistor should be tied from BIAS to $-V_{IN}$. This determines the magnitude of bias current in all of the analog sections and the pull-up current for the $\overline{\text{SHUTDOWN}}$ and RESET pins. The current flowing in the bias resistor is nominally 15 μA.

Detailed Description (Cont'd)

Reference Section

The reference section of the Si9104 consists of a temperature compensated buried zener and trimmable divider network. The output of the reference section is connected internally to the non-inverting input of the error amplifier. Nominal reference output voltage is 4 V. The trimming procedure that is used on the Si9104 brings the output of the error amplifier (which is configured for unity gain during trimming) to within ± 1.0% of 4 V. This compensates for the input offset voltage in the error amplifier.

The output impedance of the reference section has been purposely made high so that a low impedance external voltage source can be used to override the internal voltage source, if desired, without otherwise altering the performance of the device.

Error Amplifier

Closed-loop regulation is provided by the error amplifier, which is intended for use with negative feedback compensation. A MOS differential input stage provides for low input current. The noninverting input to the error amplifier (V_{REF}) is internally connected to the output of the reference supply and should be bypassed with a capacitor to ground (0.1 µF typically).

Oscillator Section

The oscillator consists of a ring of CMOS inverters, capacitors, and a capacitor discharge switch. Frequency is set by an external resistor between OSC IN and OSC OUT. (See Applications section for details of resistor value vs. frequency.) The DISCHARGE should be tied to $-V_{IN}$ for normal internal oscillator operation. A frequency divider in the logic section limits switch duty cycle to ≤ 50% by locking the switching frequency to one half of the oscillator frequency.

Remote synchronization can be accomplished by capacitive coupling of a synchronization pulse into the OSC IN terminal. For a 5-V pulse amplitude and 0.5-µs pulse width, typical values would be 100 pF in series with 3 kΩ to OSC IN.

$\overline{\text{SHUTDOWN}}$ and RESET

$\overline{\text{SHUTDOWN}}$ and RESET are intended for overriding the output MOSFET switch via external control logic. The two inputs are fed through a latch preceding the output switch. Depending on the logic state of RESET, $\overline{\text{SHUTDOWN}}$ can be either a latched or unlatched input. The output is off whenever $\overline{\text{SHUTDOWN}}$ is low. By simultaneously having $\overline{\text{SHUTDOWN}}$ and RESET low, the latch is set and $\overline{\text{SHUTDOWN}}$ has no effect until RESET goes high. The truth table for these inputs is given in Table 2.

Table 2: Truth Table for the $\overline{\text{SHUTDOWN}}$ and RESET Pins

$\overline{\text{SHUT-DOWN}}$	RESET	Output
H	H	Normal Operation
H	⌝⌞	Normal Operation (No Change)
L	H	Off (Not Latched)
L	L	Off (Latched)
⌟⌜	L	Off (Latched, No Change)

Both pins have internal current source pull-ups and should be left disconnected when not in use. An added feature of the current sources is the ability to connect a capacitor and an open-collector driver to the $\overline{\text{SHUTDOWN}}$ or RESET pins to provide variable shutdown time.

Output Switch

The output switch is a 5-Ω , 200-V lateral DMOS device. Like discrete power MOSFETs, the switch contains an intrinsic body-drain diode. However, the body contact in the Si9104 is connected internally to $-V_{IN}$ and is independent of the SOURCE.

Applications

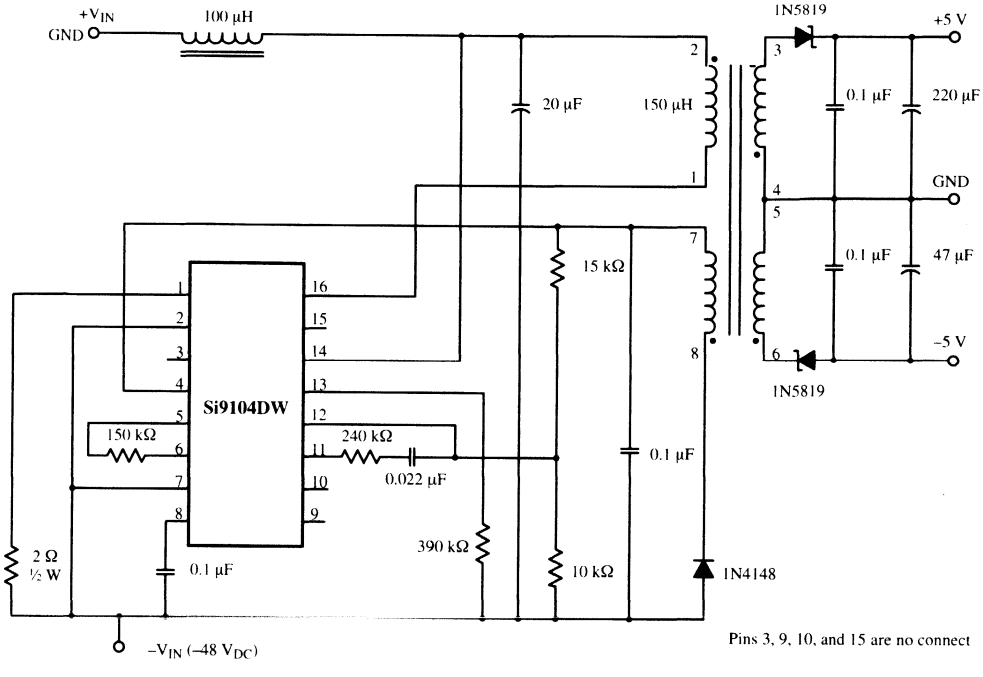


Figure 4. One-Watt Flyback Converter for Telecommunications Power Supplies

1-W High-Voltage Switchmode Regulator

Features

- CCITT Compatible
- Current-Mode Control
- Low Power Consumption (less than 5 mW)
- 10- to 120-V Input Range
- 200-V, 250-mA MOSFET
- Internal Start-Up Circuit
- Current-Mode Control
- $\overline{\text{SHUTDOWN}}$ and RESET

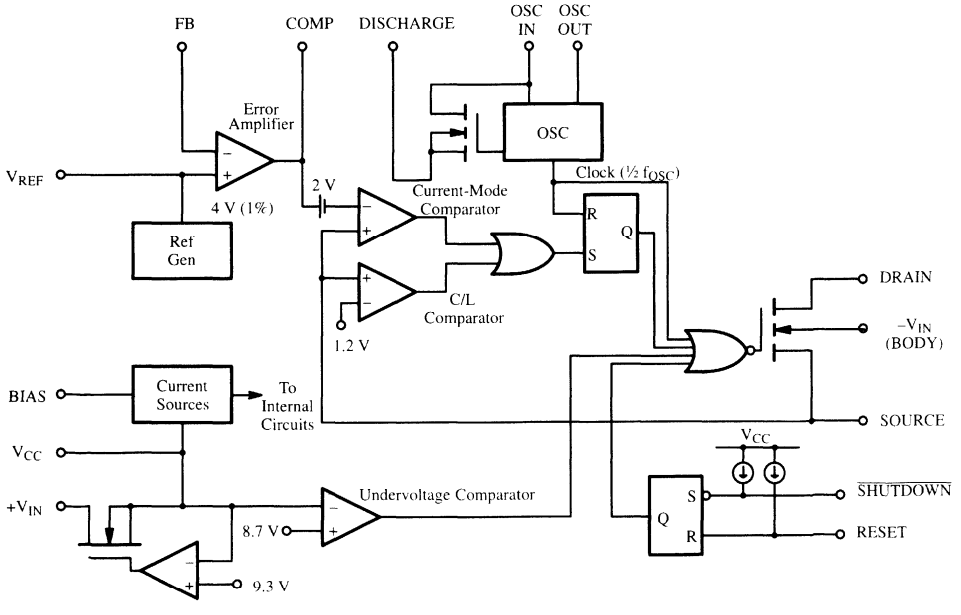
Description

The Si9105 high-voltage switchmode regulator is a monolithic BiC/DMOS integrated circuit which contains most of the components necessary to implement a high-efficiency dc/dc converter in ISDN terminals up to 3 watts. A 0.5-mA max supply current makes possible the design of a dc/dc converter with 60% efficiency at 25 mW, therefore meeting the recommended performance under the CCITT I.430 specifications.

This device may be used with an appropriate transformer to implement isolated flyback power converter topologies to provide single or multiple regulated dc outputs (i.e., ±5 V).

The Si9105 is available in 16-pin wide-body SOIC, 14-pin plastic DIP, and 20-pin PLCC packages, and is specified over the industrial, D suffix (–40 to 85°C) temperature range.

Functional Block Diagram



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Absolute Maximum Ratings

Voltages Referenced to $-V_{IN}$ ($V_{CC} < +V_{IN} + 0.3$ V)
V_{CC} ..... 15 V
$+V_{IN}$ ..... 120 V
V_{DS} ..... 200 V
I_D (Peak) (300 µs pulse, 2% duty cycle) ..... 2 A
I_D (rms) ..... 250 mA
Logic Inputs (RESET, $\overline{\text{SHUTDOWN}}$, OSC IN) ..... –0.3 V to V_{CC} + 0.3 V
Linear Inputs (FEEDBACK, SOURCE) ..... –0.3 V to 7 V
HV Pre-Regulator Input Current (continuous) ..... 5 mA
Storage Temperature ..... –65 to 125°C
Operating Temperature ..... –40 to 85°C
Junction Temperature (T_J) ..... 150°C

Power Dissipation (Package)[a]
14-Pin Plastic DIP (J Suffix)[b] ..... 750 mW
16-Pin Plastic Wide-Body SOIC (W Suffix)[c] ..... 900 mW
20-Pin PLCC (N Suffix)[d] ..... 1400 mW

Thermal Impedance (Θ_{JA})
14-Pin Plastic DIP ..... 167°C/W
16-Pin Plastic Wide-Body SOIC ..... 140°C/W
20-Pin PLCC ..... 90°C/W

Notes
a. Device mounted with all leads soldered or welded to PC board.
b. Derate 6 mW/°C above 25°C
c. Derate 7.2 mW/°C above 25°C
d. Derate 11.2 mW/°C above 25°C

Recommended Operating Range

Voltages Referenced to $-V_{IN}$
V_{CC} ..... 10 V to 13.5 V
$+V_{IN}$ ..... 10 V to 120 V
f_{OSC} ..... 40 kHz to 1 MHz
R_{OSC} ..... 25 kΩ to 1 MΩ
Linear Inputs ..... 0 to V_{CC} – 3 V
Digital Inputs ..... 0 to V_{CC}

Specifications[a]

Parameter	Symbol	Test Conditions Unless Otherwise Specified DISCHARGE = $-V_{IN}$ = 0 V V_{CC} = 10 V, $+V_{IN}$ = 48 V R_{BIAS} = 820 kΩ, R_{OSC} = 910 kΩ	Temp[b]	Limits D Suffix –40 to 85°C Min[d]	Typ[c]	Max[d]	Unit
Reference							
Output Voltage	V_R	OSC IN = V_{IN} (OSC Disabled) R_L = 10 MΩ	Room	3.92	4.00	4.08	V
Output Impedance[e]	Z_{OUT}	OSC IN = $-V_{IN}$	Room	15	300	45	kΩ
Short Circuit Current	I_{SREF}	OSC IN = – V_{IN}, V_{REF} = $-V_{IN}$	Room	70	100	130	µA
Temperature Stability[e]	T_{REF}	OSC IN = $-V_{IN}$	Full		0.25	1.0	mV/°C
Long Term Stability[e]		t = 1000 hrs, T_A = 125°C	Room		5.00	25.00	mV
Oscillator							
Maximum Frequency[e]	f_{MAX}	R_{OSC} = 0	Room	1	3		MHz
Initial Accuracy	f_{OSC}	See Note e	Room	32	40	48	kHz
Voltage Stability	$\Delta f/f$	$\Delta f/f$ = f (13.5 V) – f (9.5 V)/f (9.5 V)	Room		10	15	%
Temperature Coefficient[e]	T_{OSC}		Full		200	500	ppm/°C
Error Amplifier							
Feedback Input Voltage	V_{FB}	FB Tied to COMP OSC IN = $-V_{IN}$ (OSC Disabled)	Room	3.96	4	4.04	V
Input BIAS Current	I_{FB}	OSC IN = $-V_{IN}$, V_{FB} = 4 V	Room		25	500	nA
Open Loop Voltage Gain[e]	A_{VOL}	OSC IN = $-V_{IN}$ (OSC Disabled)	Room	60	80		dB

Specifications[a]

Parameter	Symbol	Test Conditions Unless Otherwise Specified DISCHARGE = $-V_{IN}$ = 0 V V_{CC} = 10 V, $+V_{IN}$ = 48 V R_{BIAS} = 820 kΩ, R_{OSC} = 910 kΩ	Temp[b]	Limits D Suffix –40 to 85°C Min[d]	Typ[c]	Max[d]	Unit
Error Amplifier (Cont'd)							
Input Offset Voltage	V_{OS}	OSC IN = $-V_{IN}$	Room		± 15	± 40	mV
Unity Gain Bandwidth[e]	BW		Room	0.5	0.8		MHz
Dynamic Output Impedance	Z_{OUT}		Room		1		kΩ
Output Current	I_{OUT}	Source (V_{FB} = 3.4 V)	Room		–1.2	–0.32	mA
		Sink (V_{FB} = 4.5 V)	Room	0.05	0.08		
Power Supply Rejection	PSRR	10 V ≤ V_{CC} ≤ 13.5 V	Room		70		dB
Current Limit							
Threshold Voltage	V_{SOURCE}	R_L = 100 Ω from DRAIN to V_{CC} V_{FB} = 0 V	Room	0.8	1.0	1.2	V
Delay to Output[e]	t_d	R_L = 100 Ω from DRAIN to V_{CC} V_{SOURCE} = 1.5 V, See Figure 1	Room		200	300	ns
Input Voltage	$+V_{IN}$	I_{IN} = 100 µA	Room	120			V
Input Leakage Current	$+I_{IN}$	V_{CC} ≥ 10 V	Room			10	µA
Pre-Regulator Start-Up Current	I_{START}	Pulse Width ≤ 300 µs, V_{CC} = 7 V	Room	8	15		mA
V_{CC} Pre-Regulator Turn-Off Threshold Voltage	V_{REG}	$I_{PRE-REGULATOR}$ = 10 µA	Room	7.5	9.3	9.7	V
Undervoltage Lockout	V_{UVLO}	R_L = 100 Ω from DRAIN to V_{CC} See Detailed Description	Room	7.0	8.7	9.2	
$V_{REG} - V_{UVLO}$	V_{DELTA}		Room	0.25	0.5		
Supply							
Supply Current	I_{CC}		Room		0.35	0.5	mA
Bias Current	I_{BIAS}		Room		7.5		µA
$\overline{\text{SHUTDOWN}}$ Delay	t_{SD}	V_{SOURCE} = $-V_{IN}$, See Figure 2	Room		50	100	ns
$\overline{\text{SHUTDOWN}}$ Pulse Width	t_{SW}	See Figure 3	Room	50			
RESET Pulse Width	t_{RW}		Room	50			
Latching Pulse Width $\overline{\text{SHUTDOWN}}$ and RESET Low	t_{LW}		Room	25			
Input Low Voltage	V_{IL}		Room			2.0	V
Input High Voltage	V_{IH}		Room	8.0			
Input Current Input Voltage High	I_{IH}	V_{IN} = 10 V	Room		1	5	µA
Input Current Input Voltage Low	I_{IL}	V_{IN} = 0 V	Room	–35	–25		

Specifications[a]

Parameter	Symbol	Test Conditions Unless Otherwise Specified DISCHARGE = $-V_{IN}$ = 0 V V_{CC} = 10 V, $+V_{IN}$ = 48 V R_{BIAS} = 820 kΩ, R_{OSC} = 910 kΩ	Temp[b]	Limits D Suffix −40 to 85°C Min[d]	Typ[c]	Max[d]	Unit
MOSFET Switch							
Breakdown Voltage	$V_{(BR)DSS}$	I_{DRAIN} = 100 µA	Full	200	220		V
Drain-Source On Resistance[g]	$r_{DS(on)}$	I_{DRAIN} = 100 mA	Room		5	7	Ω
Drain Off Leakage Current	I_{DSS}	V_{DRAIN} = 100 V	Room			10	µA
Drain Capacitance	C_{DS}		Room		35		pF

Notes
a. Refer to PROCESS OPTION FLOWCHART for additional information.
b. Room = 25°C, Cold and Hot = as determined by the operating temperature suffix.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
e. Guaranteed by design, not subject to production test.
f. C_{STRAY} Pin 8 = ≤ 5 pF
g. Temperature coefficient of $r_{DS(on)}$ is 0.75% per °C, typical.

Timing Waveforms

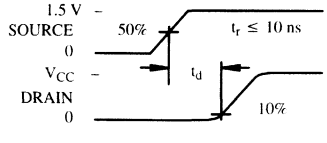


Figure 1.

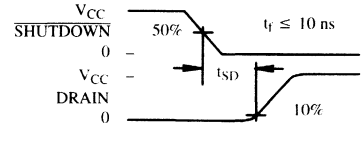


Figure 2.

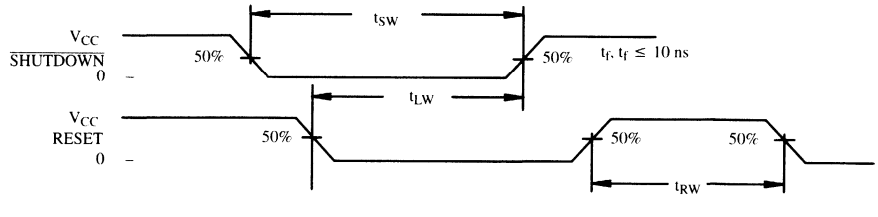
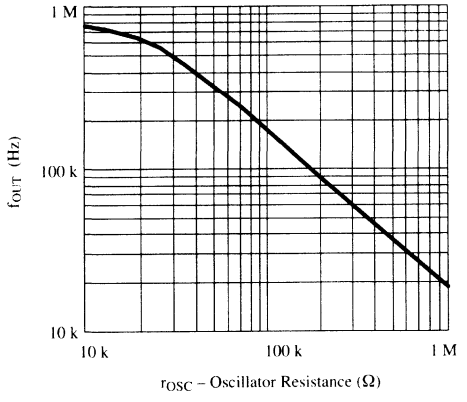


Figure 3.

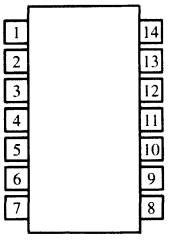
Typical Characteristics

Output Switching Frequency vs. Oscillator Resistance



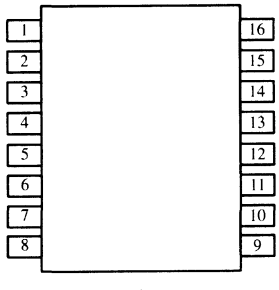
Pin Configurations

PDIP-14



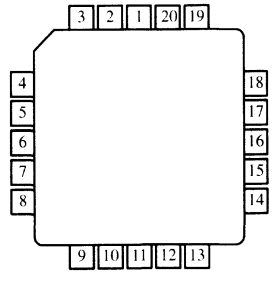
Top View
Order Number: Si9105DJ02

SO-16 (Wide-Body)



Top View
Order Number: Si9105DW

PLCC-20



Top View
Order Number: Si9105DN02

Function	Pin Number		
	14-Pin Plastic DIP	16-Pin SOIC	20-Pin PLCC
SOURCE	4	1	7
$-V_{IN}$	5	2	8
V_{CC}	6	4	9
OSC_{OUT}	7	5	10
OSC_{IN}	8	6	11
DISCHARGE	9	7	12
V_{REF}	10	8	14
$\overline{SHUTDOWN}$	11	9	16
RESET	12	10	17
COMP	13	11	18
FB	14	12	20
BIAS	1	13	2
$+V_{IN}$	2	14	3
DRAIN	3	16	5
NC		3, 15	1, 4, 6, 13, 15, 19

Detailed Description

Pre-Regulator/Start-Up Section

Due to the low quiescent current requirement of the Si9105 control circuitry, bias power can be supplied from the unregulated input power source, from an external regulated low-voltage supply, or from an auxiliary "bootstrap" winding on the output inductor or transformer.

When power is first applied during start-up, $+V_{IN}$ will draw a constant current. The magnitude of this current is determined by a high-voltage depletion MOSFET device which is connected between $+V_{IN}$ and V_{CC}. This start-up circuitry provides initial power to the IC by charging an external bypass capacitance connected to the V_{CC} pin. The constant current is disabled when V_{CC} exceeds 9.3 V. If V_{CC} is not forced to exceed the 9.3-V threshold, then V_{CC} will be regulated to a nominal value of 9.3 V by the pre-regulator circuit.

As the supply voltage rises toward the normal operating conditions, an internal undervoltage (UV) lockout circuit keeps the output MOSFET disabled until V_{CC} exceeds the undervoltage lockout threshold (typically 8.7 V). This guarantees that the control logic will be functioning properly and that sufficient gate drive voltage is available before the MOSFET turns on. The design of the IC is such that the undervoltage lockout threshold will not exceed the pre-regulator turn-off voltage. Power dissipation can be minimized by providing an external power source to V_{CC} such that the constant current source is always disabled.

BIAS

To properly set the bias for the Si9105, a 820-kΩ resistor should be tied from BIAS to $-V_{IN}$. This determines the magnitude of bias current in all of the analog sections and the pull-up current for the $\overline{\text{SHUTDOWN}}$ and RESET pins. The current flowing in the bias resistor is nominally 7.5 µA.

Reference Section

The reference section of the Si9105 consists of a temperature compensated buried zener and trimmable divider network. The output of the reference section is connected internally to the non-inverting input of the error amplifier. Nominal reference output voltage is 4 V. The trimming procedure that is used on the Si9105 brings the output of the error amplifier (which is configured for unity gain during trimming) to within ±1% of 4 V. This automatically compensates for the input offset voltage in the error amplifier.

The output impedance of the reference section has been purposely made high so that a low impedance external voltage source can be used to override the internal voltage source, if desired, without otherwise altering the performance of the device.

Error Amplifier

Closed-loop regulation is provided by the error amplifier, whose 1-kΩ dynamic output impedance enables it to be used with feedback compensation (unlike transconductance amplifiers). A MOS differential input stage provides for low input current. The noninverting input to the error amplifier (V_{REF}) is internally connected to the output of the reference supply and should be bypassed with a small capacitor to ground.

Oscillator Section

The oscillator consists of a ring of CMOS inverters, capacitors, and a capacitor discharge switch. Frequency is set by an external resistor between the OSC IN and OSC OUT pins. (See Typical Characteristics graph of resistor value vs. frequency.) The DISCHARGE pin should be tied to $-V_{IN}$ for normal internal oscillator operation. A frequency divider in the logic section limits switch duty cycle to a maximum of 50% by locking the switching frequency to one half of the oscillator frequency.

Remote synchronization can be accomplished by capacitive coupling of a synchronization pulse into the OSC IN terminal. For a 5-V pulse amplitude and 0.5-µs pulse width, typical values would be 100 pF in series with 3 kΩ to OSC IN.

$\overline{\text{SHUTDOWN}}$ and RESET

$\overline{\text{SHUTDOWN}}$ and RESET are intended for overriding the output MOSFET switch via external control logic. The two inputs are fed through a latch preceding the output switch. Depending on the logic state of RESET, $\overline{\text{SHUTDOWN}}$ can be either a latched or unlatched input. The output is off whenever $\overline{\text{SHUTDOWN}}$ is low. By simultaneously having $\overline{\text{SHUTDOWN}}$ and RESET low, the latch is set and $\overline{\text{SHUTDOWN}}$ has no effect until RESET goes high. The truth table for these inputs is given in Table 1.

Both pins have internal current source pull-ups and can be left disconnected when not in use. An added feature of the current sources is the ability to connect a capacitor and an open-collector driver to the $\overline{\text{SHUTDOWN}}$ pin to provide variable shutdown time.

Detailed Description (Cont'd)

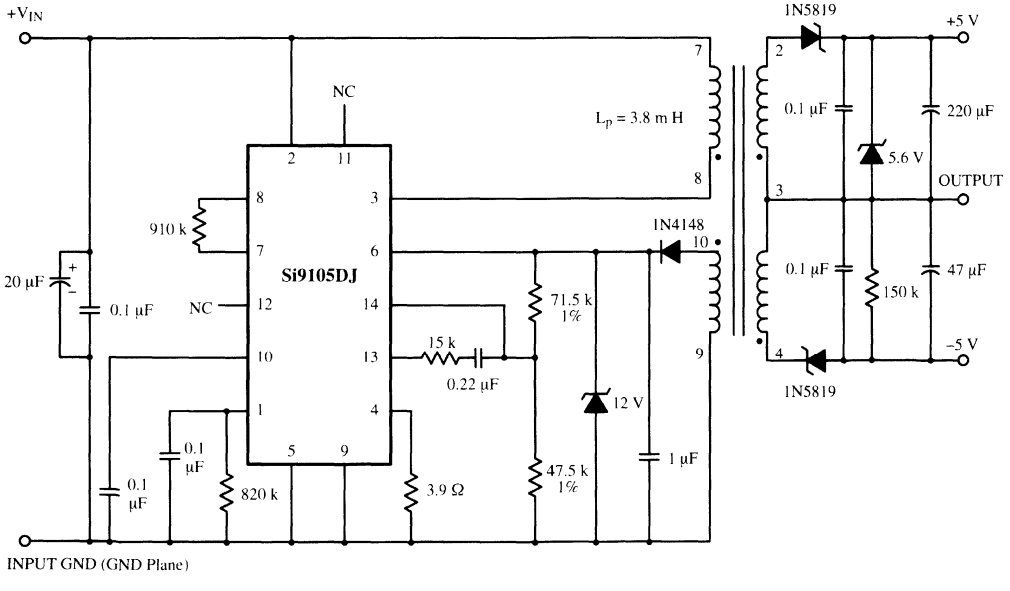
Output Switch

The output switch is a 7-Ω, 200-V lateral DMOS transistor. Like discrete MOSFETs, the switch contains an intrinsic body-drain diode. However, the body contact in the Si9105 is connected internally to $-V_{IN}$ and is independent of the SOURCE.

Table 1. Truth Table for the $\overline{\text{SHUTDOWN}}$ and RESET Pins

$\overline{\text{SHUTDOWN}}$	RESET	Output
H	H	Normal Operation
H	⌐	Normal Operation (No Change)
L	H	Off (Not Latched)
L	L	Off (Latched)
⌐	L	Off (Latched, No Change)

Applications



CCITT Compatible ISDN Terminal Power Supply

Designing DC/DC Converters to Meet CCITT Specifications for ISDN Terminals

James Blanc

Integrated Services Digital Network (ISDN) standards are a major step towards the realization of a worldwide information grid. Just as power system standards allow the connection of either a microwave oven or a television set into a power receptacle, so ISDN will allow information appliances, such as facsimile machines, computer terminals, and telephones to plug into a standard socket. It will be possible to move office equipment either down the hall or around the world and immediately "plug in" to the information grid. ISDN will allow the travelling worker to communicate (using portable computers and facsimile machines) with customers or manufacturing sites worldwide. And this will be accomplished without modems, which slow data transmission rates.

One of the larger technical problems in achieving such a powerful information network is that the existing telephone system was designed over eighty years ago for the more limited purpose of reliably transmitting voice signals. Plain old telephone service, or POTS, has such an excellent reliability record that the general public takes for granted that the phone still works when the lights go out. But the simple power feeding method (a central office battery connected to the telephone via a pair of copper wires) is inadequate for ISDN. Nonetheless, ISDN must not achieve upgraded data communication capability at the expense of voice communication reliability. That is, when the lights go out, the new digital telephones must still operate.

The Deutsche Bundespost (DBP) took the lead several years ago[1] in defining a methodology for feeding power to ISDN terminals which is compatible with the data transmission requirements of ISDN and the reliability requirements of POTS. The DBP proposals have been incorporated into the CCITT standard I.430, which defines the physical characteristics of the ISDN interfaces. [The Consultative Committee for International Telegraph and Telephone (CCITT) is part of the International Telecommunications Union of the United Nations.] The standard calls for galvanic isolation in terminal equipment (TE) connected to the subscriber- or S-bus. This requires the use of an efficient switchmode dc/dc converter in each TE. Also, while the older analog telephony circuits can get by on about 100 mW, the new digital telephones (D-phones) require approximately 300 mW.

Up to eight D-phones or other TEs can be connected to each S-bus, but the CCITT recommendation allows that only one terminal be operational during restricted power conditions. When the network terminal (NT) senses the loss of normal power, it reverses the polarity of the dc feeding voltage on the S-bus. Non-emergency-designated terminals have a reverse polarity diode which effectively removes their loads from the S-bus during the outage. The emergency-designated terminal uses a diode bridge at the input, so that it remains connected across the bus at all times. This application note specifically addresses design issues relating to emergency-designated ISDN terminals and presents design details for a dc/dc converter which conforms to the international standard.

CCITT Standard I.430

Table 1 summarizes the CCITT document as it applies to dc/dc converters in emergency-designated TEs. During normal-mode operation, terminals may have multiple power sources, including up to 1 W from the S-bus (Power Source 1), whose dc voltage must be between 24 and 42 V measured at the input to the TE. During the restricted power condition the designated TE in the active state must draw less than 380 mW from Power Source 1 (PS1), and the input voltage magnitude must be 32 to 42 V. Eighty percent efficiency has previously been demonstrated for dc/dc converters at these power levels[2].

The difficult problem presented by the CCITT specification occurs when the phone is on-hook (deactivated state) during the restricted power condition. In order that the terminal be capable of receiving incoming calls, the line activity detection circuitry in the TE must continue to operate while the total power consumption must be maintained below 25 mW. Also, the "Terminal Endpoint Identifier (TEI)" must be retained, which means that some power is required for memory holdup. These functions require approximately 13 mW, and the input voltage is still in the 32- to 42-V range.

Updates to this app note may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70578.

Needless to say, off-the-shelf +40-V to +5-V dc/dc converters with 55% worst-case efficiency at an output power level of 13 mW do not exist today. They can, however, be designed using readily available off-the-shelf components, but the methodology for their design is different from that of conventional power supplies.

Design Methodology

A flyback converter topology provides galvanic isolation while requiring only one magnetic energy storage device. This minimizes cost since inductors and transformers are the most expensive components in switch mode power converters. Selection of the primary inductance value was discussed in a previous Siliconix Application Note, AN702, which analyzes the start-up constraints of dc/dc converters fed from high-impedance sources. The result of that analysis was a primary inductance of 3.75 mH. Since the S-bus is relatively short compared to the subscriber loop, and it is fed from a dc/dc converter in the NT, the source impedance seen by the dc/dc converter in the TE is relatively low. This indicates that a lower primary inductance, L_P can be chosen, which allows the inductor to be smaller.

There is, however, another reason to utilize a high inductance value. The energy transferred to the inductor during each cycle is given by Equation 1.

$$E = \tfrac{1}{2} L_P I_{PK}^2 \qquad (1)$$

I_{PK} is the peak inductor current, and it is assumed that the initial current is zero. The same amount of energy transfer can be achieved with a small L_P and large I_{PK}, or vice versa. But the RMS value of the current is less for the case of large L_P and small I_{PK}. This reduces the conduction losses in the primary winding, MOSFET, and sense resistor, which is essential to achieving high efficiency at the milliwatt power level. With a total power budget of only 25 mW, every milliwatt lost causes a four percent reduction in efficiency.

To minimize dynamic losses, defined as those dependent upon operating frequency, it is advantageous to use the smallest switching frequency, f_S, which is practical. If possible, this frequency should be above the audible range. 18 kHz was selected for the nominal switching frequency when the oscillator is free-running (36 kHz for the oscillator, which includes a divide- by-two). This occurs during start-up or under restricted power conditions. For operating conditions other than the deactivated state in the restricted power mode, a system clock should be available. It is desirable to synchronize the dc/dc converter to a signal derived from this clock to minimize noise coupling into the A/D and D/A converter (CODEC) circuits. The synchronization frequency should be 10 to 20% above the free-running frequency.

Another choice must be made which has a large impact on the dc/dc converter cost, light load efficiency, and output voltage regulation. Voltage feedback must be implemented while at the same time maintaining galvanic isolation. There are two possible approaches. The first is to use optical isolation and place the error amplifier and voltage reference on the secondary side. This gives the best result in terms of load regulation, but it costs more and it decreases light load efficiency. The error amp and reference generator could be eliminated from the primary side controller and put into a separate IC on the secondary side. For these components, the power losses thus remain approximately the same. But the optical isolator consumes some additional power and increases total converter cost.

The second option, which is used here, is to employ an auxiliary winding to indirectly sense the output voltage. This winding is essentially free, since it must be used anyway to provide the bootstrap supply for the switchmode regulator IC. Using this technique, the output voltage regulation is dependent upon the coupling between the secondary and auxiliary windings as well as upon the switching frequency.

Table 1. Power Source 1 Requirements Emergency – Designated ISDN TE's

Power Mode	TE State	Voltage Range	Max Power to TE
Normal	Active	+ 24 to +42 V	1 W
Normal	Deactivated	+24 to +42 V	100 mW
Restricted	Active	–32 to –42 V	380 mW
Restricted	Deactivated	–32 to –42 V	25 mW

The total variation in output voltage as the load current is varied from the minimum (3 mA at +5 V, 0 mA at –5 V) to the maximum level (100 mA at +5 V, 30 mA at –5 V) was 10%. This should permit a specified regulation range of ±7% at the converter output. If tighter regulation is required for a given application, then the opto-isolation approach will be required.

Circuit Description

The complete schematic for the dc/dc converter is given in Figure 1, and the block diagram of the Si9105 switchmode regulator IC is shown in Figure 2. The Si9105 is a variation of the original Si9100 switchmode regulator which was introduced in March, 1987. It includes an oscillator, an error amplifier, a pre-regulator/start-up circuit, a trimmed voltage reference, low-power CMOS logic and comparators, undervoltage lockout and current-limit protection circuitry, and a high-voltage MOSFET transistor—all on a single chip in a 14-pin DIP or 20-pin PLCC for surface-mount assembly.

The block diagram of the Si9105 is the same as that for the Si9100, but several key specifications are upgraded. The most important specification here is the maximum power dissipation of the chip. The supply current, I_{CC}, is 0.5 mA maximum (0.35 mA typical), giving P_D = 5 mW maximum for V_{CC} = 10 V. The start-up circuit shuts off the 120-V rated pre-regulator transistor after start-up so that I_{CC} is taken from the auxiliary 10-V output rather than from the 40-V input bus. The power saved is approximately

$$P_{Saved} = (40\ V)(0.35\ mA) - (10\ V)(0.35\ mA)$$
$$= 14\ mW - 3.5\ mW = 11.5\ mW \quad (2)$$

Without such an auxiliary supply, it is easy to see from Equation 2 that 55% efficiency with 25 mW at the input is not possible.

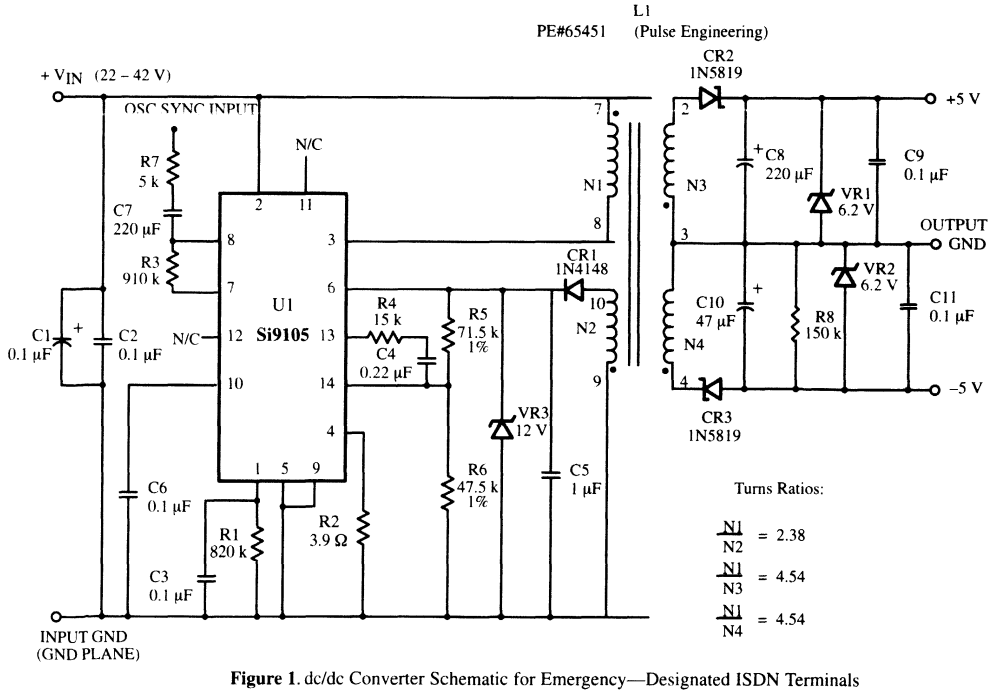


Figure 1. dc/dc Converter Schematic for Emergency—Designated ISDN Terminals

* Pulse Engineering, Inc., P.O. Box 12235, San Diego, CA 92112, (619) 268-2400

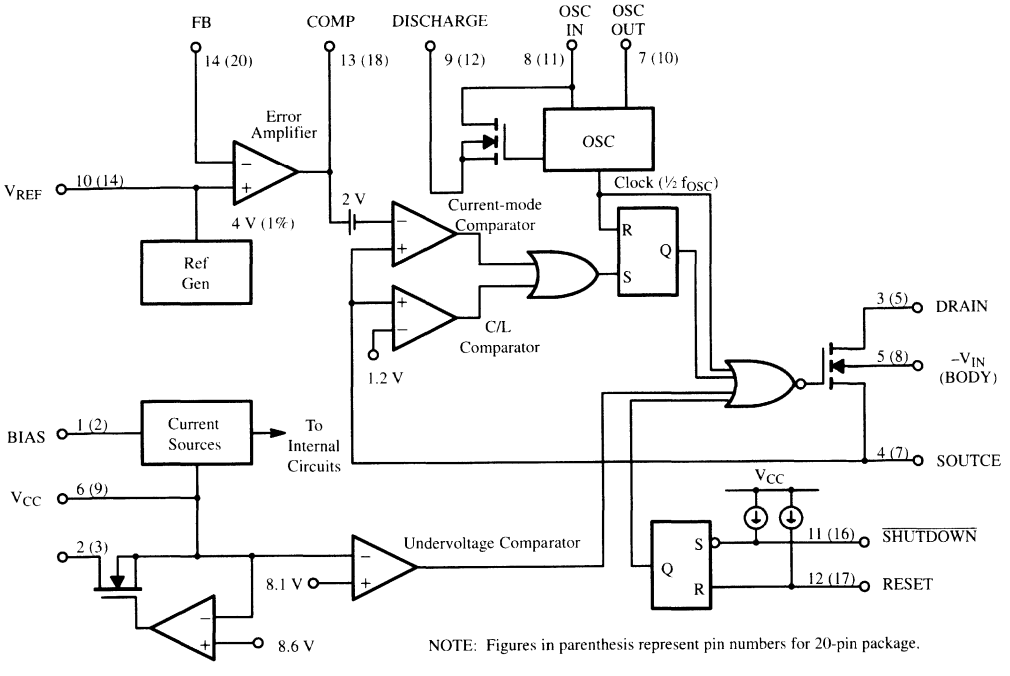


Figure 2. Si9105 Block Diagram

The 4-V reference of the Si9105 is a temperature compensated buried Zener, which is trimmed to 1% initial accuracy at a specified bias current of 7.5 µA. This is one-half of the bias current specified for the Si9100, and a bias resistor equal to 820 kΩ from pin 1 to ground is all that is required to program I_{BIAS}. Finally, the MOSFET switching transistor in the Si9105 has been rated at a higher breakdown voltage, 200 V versus 150 V, at the same time its $r_{DS(ON)}$ has been maintained at 5 Ω maximum.

The other key component in the converter circuit is the coupled inductor, L1. Pulse Engineering* has provided a cost-effective inductor design, part number PE65451, specifically designed for this ISDN terminal application. L1 has an isolation voltage specification of 1750 V_{RMS}.

Measured Circuit Performance

Figure 3 shows an oscilloscope photograph of the primary side voltage and current waveforms for operation under the emergency load conditions.

The calculated peak current is

$$P_{IN} = 25 \text{ mW} = \tfrac{1}{2} L_P I_{PK}^2 f_S$$

For L_P = 3.8 mH and f_S = 18 kHz, I_{PK} equals 27 mA. The MOSFET conduction time is calculated from

$$\frac{V_{IN}}{L_P} = \frac{I_{PK}}{t_{ON}}$$

For V_{IN} = 40 V, L_P = 3.8 mH, and I_{PK} = 27 mA, t_{ON} is equal to 2.6 µs and the duty cycle is (2.6 µs)•(18 kHz) = 0.046 (or about 5%). Figure 4 shows the corresponding waveforms during full load operation.

An efficient power supply which self-destructs when its output is shorted to ground is of limited value. Some additional components are needed to protect the power supply and its loads from overcurrent and overvoltage transients.

Figure 5 shows the converter waveforms with the output terminals shorted to ground. Note that the converter goes into the continuous conduction mode of operation (the current waveform is trapezoidal), but the dc input current was measured at 10.5 mA. The power dissipation of (10.5 mA) • (40 V) = 420 mW can be sustained indefinitely without damage to the converter.

When the short circuit is removed from the converter output, the control loop forces the duty ratio to increase to its maximum value since the error amplifier output will be near the positive rail. The control loop has been made purposely slow to prevent it from being susceptible to noise when operating at very light loads. This causes the recovery time from the short circuit condition to be long, and the output and auxiliary winding voltages become excessive unless clamped by Zener diodes VR1, VR2, and VR3. As a final note, the recommended procedure for oscillator synchronization is to feed a positive going SYNC pulse through an R-C network to pin 8. The recommended values are 5 kΩ and 220 pF.

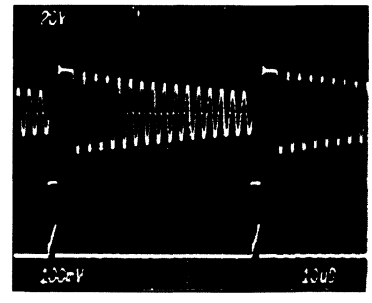
A summary of the dc/dc converter specifications is given in Table 2 for reference.

Circuit Analysis

It is instructive to calculate the converter losses for the restricted power condition in the inactive state to gain some insight as to the relative importance of the design parameters. In other words, how important are MOSFET $r_{DS(on)}$ and output capacitance, leakage inductance, switching frequency, etc. to the converter efficiency?

Table 2.

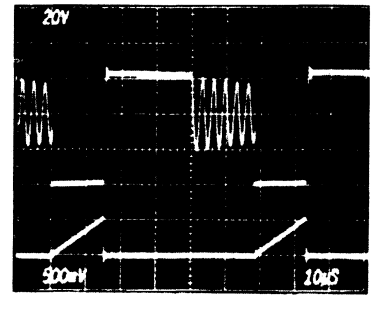
Input Voltage Range	Max. Load 22 – 42 V Min. Load 30 – 42 V
Output Load Current	Min. Load 3 mA @ +5 V 0 mA @ –5 V Max. Load 100 mA @ +5 V 30 mA @ –5 V
Regulation	±7% worst case (±5% typical)
Output Ripple	100 mV Max. at full load (60 mV typical) at full load
Conversion Efficiency	Max. Load 80% min (85% typical) Min. Load 55% min.(67% typical)
Isolation Voltage	1750 V_{RMS} primary to secondary



V_{DS} (20 V/div) U1 pin 3

V_{SENSE} (0.1 V/div) U1 pin 4

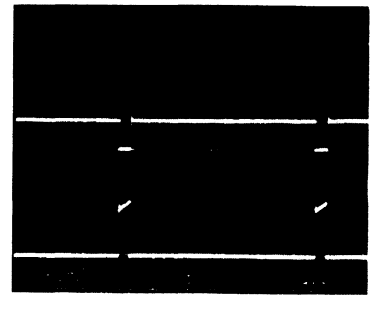
Figure 3. MOSFET drain voltage and current waveforms for emergency-power operation



V_{DS} (20 V/div) U1 pin 3

V_{SENSE} (0.5 V/div) U1 pin 4

Figure 4. MOSFET drain voltage and current waveforms for full-load operation



V_{DS} (50 V/div) U1 pin 3

V_{SENSE} (0.5 V/div) U1 pin 4

Figure 5. MOSFET drain voltage and current waveforms for the output short circuit condition.

Table 3. Power Loss Calculations (Emergency Power-Down State)

Source of Loss	Dynamic Losses (freq. dep.)	Static Losses (not freq. dep.)	Load-Dependent Losses	No-Load losses
MOSFET + R_{sense} (conduction)		0.09	0.09	
Feedback Voltage Divider Network		0.84		0.84
Rectifier Conduction		1.58	1.58	
–5 V Pre-Load		0.18		0.18
Si9105 Controller (REF Gen + Analog)		2.85		2.85
Si9105 Controller (Logic + OSC + Driver)	0.50			0.50
Turn-On ($\frac{1}{2}$ CV^2f_s)	1.08			1.08
TOTAL	**1.58 mW**	**5.54 mW**	**1.67 mW**	**5.45 mW**
	7.12 mW		7.12 mW	

Measured: P_{IN} = 22.92 mW, P_O = 15.25 mW, h = 66.6%, P_{loss} = 7.67 mW

The exercise of "counting the milliwatts" was performed and is included in Appendix A for reference. The summary appears in Table 3. Power losses are sorted in two different ways: 1) according to whether or not they should be expected to vary with the choice of operating frequency (dynamic vs. static losses) and 2) according to whether or not they vary with the output load current. The power consumption of the Si9105 is divided into two components: one which is frequency dependent (logic gates plus oscillator plus MOSFET drive) and the other which is constant (voltage reference plus analog circuits).

Several interesting conclusions can be drawn from Table 3. An observation which may well have been expected is that most of the losses are not load dependent at the 25 mW power level. But one may not have expected that the MOSFET conduction and sense resistor losses should be nearly negligible. These losses, together with the rectifier losses, totally dominate for the full load condition. A final observation is that MOSFET and transformer parasitic capacitances, which cause negligible losses at higher power levels, have significant effect at such low current levels.

As a final summary of the power converter efficiency. Figure 6 plots the measured efficiency as a function of output power. It should be noted that these efficiencies do not include losses in the input rectifier bridge to the emergency-designated terminal. The worst-case input current is given by Equation 5.

$$I_{IN(max)} = \frac{P_{IN(max)}}{V_{IN(min)}} = \frac{25\ mW}{32\ V} = 780\ \mu A$$

Assuming two diode drops at 0.6 V each gives a power loss of

$$P_D = (1.2\ V)\ (780\ \mu A) = 940\ \mu W.$$

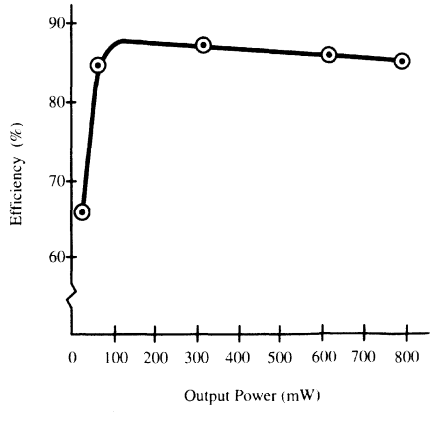


Figure 6. Measured Efficiency vs. Output Power

If the worst case for the Si9105 power consumption is taken into account, then an additional 1.5-mW loss is possible. The 7.7-mW measured loss plus 1.0 mW for the rectifier bridge, 1.5 mW for the regulator IC, and 1.0 mW for other miscellaneous circuit losses gives a worst-case power dissipation of 11.2 mW. Output power is a minimum of 13.8 mW, and the minimum efficiency is 55%.

Conclusion

Worst case efficiency of 55% is a realizable goal for dc/dc converters in ISDN terminals which meet CCITT specifications. The Si9105 switchmode regulator is the first fully-integrated solution which has been demonstrated to provide the required efficiencies over the 13 mW to 650 mW output power range.

References

1) Rosenbaum, D. and Stolp, K., "The Feeding Conception of the ISDN Basic Access," IEEE INTELEC Conference Proceedings, Munich, FRG, Oct 14–17, 1985, pp. 505–512.

2) "A One-Watt Flyback Converter Using the Si9100", Siliconix Application Note, AN713, March 1987.

APPENDIX A

Calculated Power Losses

1. MOSFET conduction losses –

RMS current is given by

$$I_{RMS} = I_{PK}\sqrt{\frac{D}{3}} = 27mA\sqrt{\frac{0.046}{3}} = 3.34\ mA$$

$$P_{COND} = I_{RMS}^2 \bullet r_{DS(ON)}$$
$$= (3.34\ mA)^2 \bullet 4\ \Omega = 45\ \mu W$$

2. Current sense resistor –

$$P_{SENSE} = (3.34\ mA)^2 \bullet 3.9\ \Omega = 44\ \mu W$$

3. Feedback divider resistor network –

$$P_{DIV} = \frac{V_{CC}^2}{R_5 + R_6} = \frac{(10\ V)^2}{71.5k\Omega + 47.5k\Omega} = 840\ \mu W$$

4. Rectifier conduction –
The inductance of the +5 V winding is

$$L_5 = L_P\left(\frac{N_3}{N_1}\right)^2 = 3.8\ mH\left(\frac{1}{4.54}\right)^2 = 184\ \mu H$$

Peak secondary current is

$$I_S = \left(\frac{N_1}{N_3}\right)I_{PK} = (4.54)(27\ mA) = 123\ mA$$

The diode conduction time is

$$t_{cond} = \frac{\Delta I}{\frac{dI}{dt}} = \frac{I_S}{\frac{V}{L}} = \frac{123\ mA}{\left(\frac{5.5\ V}{184\ \mu H}\right)} = 4.10\ \mu s$$

$$T_S = \frac{1}{f_s} = \frac{1}{18\ kHz} = 55.5\ \mu s$$

The duty ratio for rectifier condition is

$$D_R = \frac{4.10\ \mu s}{55.5\ \mu s} = 0.074$$

Assuming a constant diode drop, V_F, of 0.35 V at this current level gives

$$P_{RECT} = \left(\frac{I_S}{2}\right)(V_F)(D_R) = \frac{123mA}{2}(0.35\ V)(0.074)$$

$$= 1.58\ mW$$

5. Pre-load resistor on –5 V output –

$$P_{PL} = \frac{V_O^2}{R} = \frac{(-5.25)^2}{150\ K} = 184\ \mu W$$

6. Turn-on losses –
$P_{ON} = ½\ C_{STRAY}\ V_{DS}^2\ f_S$, where C_{STRAY} includes the transformer winding capacitance plus the MOSFET output capacitance.

$$C_{STRAY} = C_{DS} + C_{WIND}$$
$$\approx 35\ pF + 40\ pF = 75\ pF$$
$$P_{ON} = ½\ (75x10^{-12})(40)^2(18x10^3) = 1.08\ mW$$

7. Quiescent power for PWM IC –

Reference generator $(60\ \mu A)(10\ V) = 0.6\ mW$

Analog Circuits $(7.5\ \mu A)(30)(10\ V) = 2.25\ mW$

(30 internal current sources at 7.5 µA each)

Logic plus oscillator

$$\left(\frac{1.5\ \mu A}{kHz}\right)(18\ kHz)\ (10\ V) = 0.27\ mW$$

MOSFET Driver –

$$P_{DRIV} = C_{GS}\ S\ V_{GS}^2\ S\ f_S$$
$$= (125\ pF)(10\ V)^2(18\ kHz) = 0.225\ mW$$

Total quiescent power of Si9105 = 3.35 mW

High-Voltage Switchmode Controllers

Features

- 10- to 120-V Input Range
- Current-Mode Control
- High-Speed, Source-Sink Output Drive
- High Efficiency Operation (> 80%)
- Internal Start-Up Circuit
- Internal Oscillator (1 MHz)
- $\overline{\text{SHUTDOWN}}$ and RESET
- Reference Selection
  Si9110 – ± 1%
  Si9111 – ± 10%

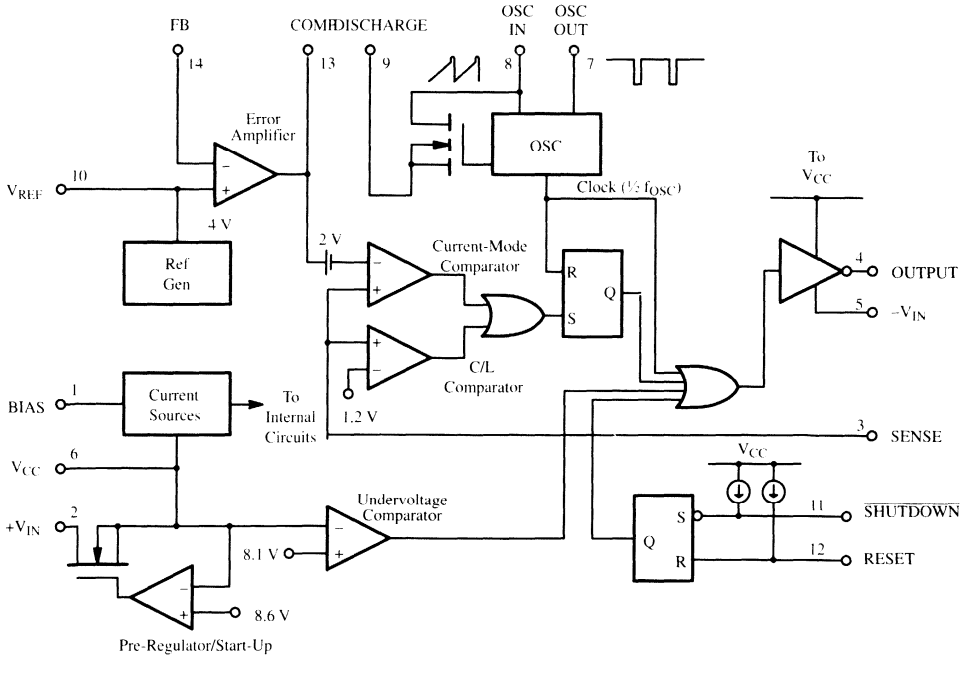
Description

The Si9110/9111 are BiC/DMOS integrated circuits designed for use as high-performance switchmode controllers. A high-voltage DMOS input allows the controller to work over a wide range of input voltages (10- to 120-VDC). Current-mode PWM control circuitry is implemented in CMOS to reduce internal power consumption to less than 10 mW.

A push-pull output driver provides high-speed switching for MOSPOWER devices large enough to supply 50 W of output power. When combined with an output MOSFET and transformer, the Si9110/9111 can be used to implement single-ended power converter topologies (i.e., flyback, forward, and cuk).

The Si9110/9111 is available in 14-pin plastic DIP and SOIC packages, and are specified over the and industrial, D suffix (–40 to 85°C) temperature ranges.

Functional Block Diagram



Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70004.

Absolute Maximum Ratings

Voltages Referenced to $-V_{IN}$ (Note: $V_{CC} < +V_{IN} + 0.3$ V)

V_{CC} ..... 15 V

$+V_{IN}$ ..... 120 V

Logic Inputs (RESET, $\overline{\text{SHUTDOWN}}$, OSC IN, OSC OUT) ..... –0.3 V to V_{CC} + 0.3 V

Linear Inputs (FEEDBACK, SENSE, BIAS, V_{REF}) ..... –0.3 V to V_{CC} + 0.3 V

HV Pre-Regulator Input Current (continuous) ..... 5 mA

Storage Temperature ..... –65 to 150°C

Operating Temperature ..... –40 to 85°C

Junction Temperature (T_J) ..... 150°C

Power Dissipation (Package)a

14-Pin Plastic DIP (J Suffix)[b] ..... 750 mW

14-Pin SOIC (Y Suffix)[c] ..... 900 mW

Thermal Impedance (Θ_{JA})

14-Pin Plastic DIP ..... 167°C/W

14-Pin SOIC ..... 140°C/W

Notes

a. Device mounted with all leads soldered or welded to PC board.
b. Derate 6 mW/°C above 25°C.
c. Derate 7.2 mW/°C above 25°C.

Recommended Operating Range

Voltages Referenced to $-V_{IN}$

V_{CC} ..... 9.5 V to 13.5 V

$+V_{IN}$ ..... 10 V to 120 V

f_{OSC} ..... 40 kHz to 1 MHz

R_{OSC} ..... 25 kΩ to 1 MΩ

Linear Inputs ..... 0 to V_{CC} – 3 V

Digital Inputs ..... 0 to V_{CC}

Specifications[a]

Parameter	Symbol	Test Conditions Unless Otherwise Specified DISCHARGE = $-V_{IN}$ = 0 V, V_{CC} = 10 V, $+V_{IN}$ = 48 V, R_{BIAS} = 390 kΩ, R_{OSC} = 330 kΩ		Temp[b]	Typ[c]	D Suffix –40 to 85°C Min[d]	D Suffix –40 to 85°C Max[d]	Unit
Reference								
Output Voltage	V_R	OSC IN = – V_{IN} (OSC Disabled) R_L = 10 MΩ	Si9110	Room	4.0	3.92	4.08	V
			Si9111	Room	4.0	3.60	4.40	
			Si9110	Full		3.86	4.14	
			Si9111	Full		3.52	4.46	
Output Impedance[e]	Z_{OUT}			Room	30	15	45	kΩ
Short Circuit Current	I_{SREF}	$V_{REF} = -V_{IN}$		Room	100	70	130	µA
Temperature Stability[e]	T_{REF}			Full	0.50		1.0	mV/°C
Oscillator								
Maximum Frequency[e]	f_{MAX}	R_{OSC} = 0		Room	3	1		MHz
Initial Accuracy	f_{OSC}	R_{OSC} = 330 k, See Note f		Room	100	80	120	kHz
		R_{OSC} = 150 k, See Note f		Room	200	160	240	
Voltage Stability	Δf/f	Δf/f=f(13.5 V) – f(9.5 V)/ f(9.5 V)		Room	10		15	%
Temperature Coefficient[e]	T_{OSC}			Full	200		500	ppm/°C
Error Amplifier								
Feedback Input Voltage	V_{FB}	FB Tied to COMP OSC IN = – V_{IN} (OSC Disabled)	Si9110	Room	4.00	3.96	4.04	V
			Si9111	Room	4.00	3.60	4.40	
Input BIAS Current	I_{FB}	OSC IN = – V_{IN}, V_{FB} = 4 V		Room	25		500	nA

Specifications[a]

Parameter	Symbol	Test Conditions Unless Otherwise Specified DISCHARGE = $-V_{IN}$ = 0 V V_{CC} = 10 V, $+V_{IN}$ = 48 V R_{BIAS} = 390 kΩ, R_{OSC} = 330 kΩ	Temp[b]	Typ[c]	D Suffix −40 to 85°C Min[d]	D Suffix −40 to 85°C Max[d]	Unit
Error Amplifier (Cont'd)							
Input OFFSET Voltage	V_{OS}	OSC IN = $-V_{IN}$ (OSC Disabled)	Room	± 15		± 40	mV
Open Loop Voltage Gain[e]	A_{VOL}		Room	80	60		dB
Unity Gain Bandwidth[e]	BW		Room	1.3	1		MHz
Dynamic Output Impedance[e]	Z_{OUT}		Room	1000		2000	Ω
Output Current	I_{OUT}	Source (V_{FB} = 3.4 V)	Room	−2.0		−1.4	mA
		Sink (V_{FB} = 4.5 V)	Room	0.15	0.12		
Power Supply Rejection	PSRR	9.5 V ≤ V_{CC} ≤ 13.5 V	Room	70	50		dB
Current Limit							
Threshold Voltage	V_{SOURCE}	V_{FB} = 0 V	Room	1.2	1.0	1.4	V
Delay to Output[e]	t_d	V_{SENSE} = 1.5 V, See Figure 1	Room	100		150	ns
Pre-Regulator/Start-Up							
Input Voltage	$+V_{IN}$	I_{IN} = 10 µA	Room		120		V
Input Leakage Current	$+I_{IN}$	V_{CC} ≥ 9.4 V	Room			10	µA
Pre-Regulator Start-Up Current	I_{START}	Pulse Width ≤ 300 µs, V_{CC} = V_{ULVO}	Room	15	8		mA
V_{CC} Pre-Regulator Turn-Off Threshold Voltage	V_{REG}	$I_{PRE\ REGULATOR}$ = 10 µA	Room	8.6	7.8	9.4	V
Undervoltage Lockout	V_{UVLO}		Room	8.1	7.0	8.9	
$V_{REG} - V_{UVLO}$	V_{DELTA}		Room	0.6	0.3		
Supply							
Supply Current	I_{CC}	C_{LOAD} < 75 pF (Pin 4)	Room	0.6	0.45	1.0	mA
Bias Current	I_{BIAS}		Room	15	10	20	µA
Logic							
$\overline{\text{SHUTDOWN}}$ Delay[e]	t_{SD}	C_L = 500 pF, V_{SENSE} $-V_{IN}$ See Figure 2	Room	50		100	ns
$\overline{\text{SHUTDOWN}}$ Pulse Width[e]	t_{SW}	See Figure 3	Room		50		
RESET Pulse Width[e]	t_{RW}		Room		50		
Latching Pulse Width $\overline{\text{SHUTDOWN}}$ and RESET Low[e]	t_{LW}	See Figure 3	Room		25		
Input Low Voltage	V_{IL}		Room			2.0	V
Input High Voltage	V_{IH}		Room		8		

1 Power Conversion

Specifications[a]

Parameter	Symbol	Test Conditions Unless Otherwise Specified DISCHARGE = $-V_{IN}$ = 0 V V_{CC} = 10 V, $+V_{IN}$ = 48 V R_{BIAS} = 390 kΩ, R_{OSC} = 330 kΩ	Temp[b]	Typ[c]	D Suffix −40 to 85°C Min[d]	D Suffix −40 to 85°C Max[d]	Unit
Logic (Cont'd)							
Input Current Input Voltage High	I_{IH}	V_{IN} = 10 V	Room	1		5	µA
Input Current Input Voltage Low	I_{IL}	V_{IN} = 0 V	Room	−25	−35		µA
Output							
Output High Voltage	V_{OH}	I_{OUT} = −10 mA	Room Full		9.7 9.5		V
Output Low Voltage	V_{OL}	I_{OUT} = 10 mA	Room Full			0.30 0.50	V
Output Resistance	R_{OUT}	I_{OUT} = 10 mA, Source or Sink	Room Full	20 25		30 35	Ω
Rise Time[e]	t_r	C_L = 500 pF	Room	40		75	ns
Fall Time[e]	t_f	C_L = 500 pF	Room	40		75	ns

Notes
a. Refer to PROCESS OPTION FLOWCHART for additional information.
b. Room = 25°C, Full = as determined by the operating temperature suffix.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum.
e. Guaranteed by design, not subject to production test.
f. C_{STRAY} Pin 8 = ≤ 5 pF.

Timing Waveforms

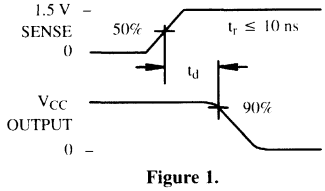


Figure 1.

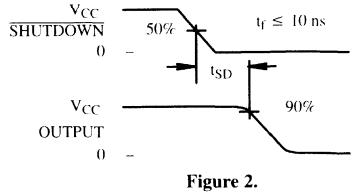


Figure 2.

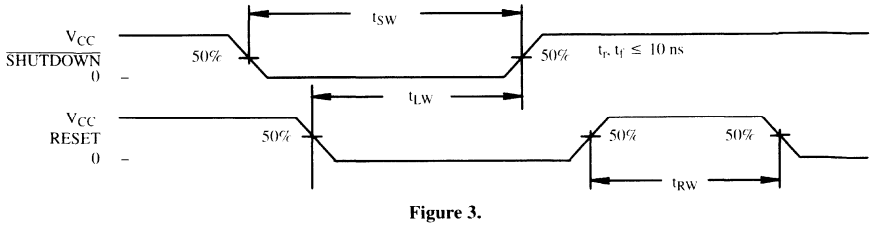
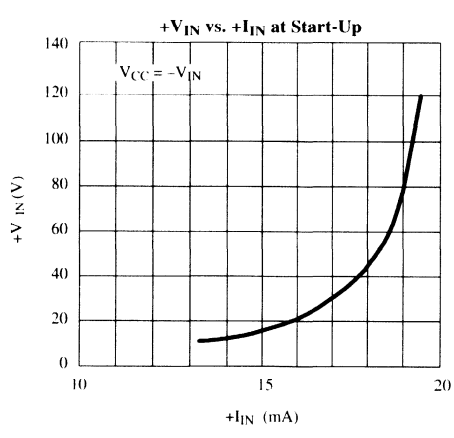
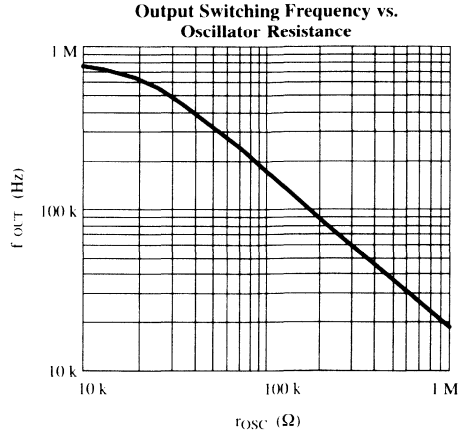


Figure 3.

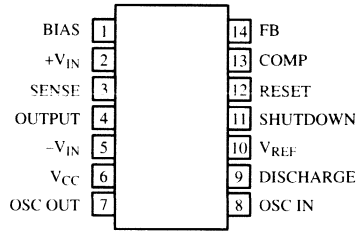
Typical Characteristics





Pin Configurations

Dual-In-Line and SOIC



Top View

Order Numbers:
Plastic DIP: Si9110DJ, Si9111DJ
SOIC: Si9110DY, Si9111DY

Detailed Description

Pre-Regulator/Start-Up Section

Due to the low quiescent current requirement of the Si9110/9111 control circuitry, bias power can be supplied from the unregulated input power source, from an external regulated low-voltage supply, or from an auxiliary "bootstrap" winding on the output inductor or transformer.

When power is first applied during start-up, $+V_{IN}$ (pin 2) will draw a constant current. The magnitude of this current is determined by a high-voltage depletion MOSFET device which is connected between $+V_{IN}$ and V_{CC} (pin 6). This start-up circuitry provides initial power to the IC by charging an external bypass capacitance connected to the V_{CC} pin. The constant current is disabled when V_{CC} exceeds 8.6 V. If V_{CC} is not forced to exceed the 8.6-V threshold, then V_{CC} will be regulated to a nominal value of 8.6 V by the pre-regulator circuit.

As the supply voltage rises toward the normal operating conditions, an internal undervoltage (UV) lockout circuit keeps the output driver disabled until V_{CC} exceeds the undervoltage lockout threshold (typically 8.1 V). This guarantees that the control logic will be functioning properly and that sufficient gate drive voltage is available before the MOSFET turns on. The design of the IC is such that the undervoltage lockout threshold will be at least 300 mV less than the pre-regulator turn-off voltage. Power dissipation can be minimized by providing an external power source to V_{CC} such that the constant current source is always disabled.

Detailed Description (Cont'd)

Note: During start-up or when V_{CC} drops below 8.6 V the start-up circuit is capable of sourcing up to 20 mA. This may lead to a high level of power dissipation in the IC (for a 48-V input, approximately 1 W). Excessive start-up time caused by external loading of the V_{CC} supply can result in device damage. Figure 4 gives the typical pre-regulator current at BiC/DMOS as a function of input voltage.

BIAS

To properly set the bias for the Si9110/9111, a 390-kΩ resistor should be tied from BIAS (pin 1) to $-V_{IN}$ (pin 5). This determines the magnitude of bias current in all of the analog sections and the pull-up current for the $\overline{\text{SHUDOWN}}$ and RESET pins. The current flowing in the bias resistor is nominally 15 µA.

Reference Section

The reference section of the Si9110 consists of a temperature compensated buried zener and trimmable divider network. The output of the reference section is connected internally to the non-inverting input of the error amplifier. Nominal reference output voltage is 4 V. The trimming procedure that is used on the Si9110 brings the output of the error amplifier (which is configured for unity gain during trimming) to within ± 1% of 4 V. This compensates for input offset voltage in the error amplifier.

The output impedance of the reference section has been purposely made high so that a low impedance external voltage source can be used to override the internal voltage source, if desired, without otherwise altering the performance of the device.

Applications which use a separate external reference, such as non-isolated converter topologies and circuits employing optical coupling in the feedback loop, do not require a trimmed voltage reference with 1% accuracy. The Si9111 accommodates the requirements of these applications at a lower cost, by leaving the reference voltage untrimmed. The 10% accurate reference thus provided is sufficient to establish a dc bias point for the error amplifier.

Error Amplifier

Closed-loop regulation is provided by the error amplifier, which is intended for use with "around-the-amplifier" compensation. A MOS differential input stage provides for low input current. The noninverting input to the error amplifier (V_{REF}) is internally connected to the output of the reference supply and should be bypassed with a small capacitor to ground.

Oscillator Section

The oscillator consists of a ring of CMOS inverters, capacitors, and a capacitor discharge switch. Frequency is set by an external resistor between the OSC IN and OSC OUT pins. (See Figure 5 for details of resistor value vs. frequency.) The DISCHARGE pin should be tied to $-V_{IN}$ for normal internal oscillator operation. A frequency divider in the logic section limits switch duty cycle to ≤ 50% by locking the switching frequency to one half of the oscillator frequency.

Remote synchronization is accomplished by capacitive coupling of a positive SYNC pulse into the OSC IN (pin 8) terminal. For a 5-V pulse amplitude and 0.5-µs pulse width, typical values would be 100 pF in series with 3 kΩ to pin 8.

$\overline{\text{SHUTDOWN}}$ and RESET

$\overline{\text{SHUTDOWN}}$ (pin 11) and RESET (pin 12) are intended for overriding the output MOSFET switch via external control logic. The two inputs are fed through a latch preceding the output switch. Depending on the logic state of RESET, $\overline{\text{SHUTDOWN}}$ can be either a latched or unlatched input. The output is off whenever $\overline{\text{SHUTDOWN}}$ is low. By simultaneously having $\overline{\text{SHUTDOWN}}$ and RESET low, the latch is set and $\overline{\text{SHUTDOWN}}$ has no effect until RESET goes high. The truth table for these inputs is given in Table 1.

Table 1: Truth Table for the $\overline{\text{SHUTDOWN}}$ and RESET Pins

$\overline{\text{SHUT-DOWN}}$	RESET	Output
H	H	Normal Operation
H	⅂	Normal Operation (No Change)
L	H	Off (Not Latched)
L	L	Off (Latched)
⌡	L	Off (Latched, No Change)

Both pins have internal current source pull-ups and should be left disconnected when not in use. An added feature of the current sources is the ability to connect a capacitor and an open-collector driver to the $\overline{\text{SHUTDOWN}}$ or RESET pins to provide variable shutdown time.

Detailed Description (Cont'd)

Output Driver

The push-pull driver output has a typical on-resistance of 20 Ω. Maximum switching times are specified at 75 ns for a 500-pF load. This is sufficient to directly drive MOSFETs such as the 2N7004, 2N7005, IRFD120 and IRFD220. Larger devices can be driven, but switching times will be longer, resulting in higher switching losses. In order to drive large MOSPOWER devices, it is necessary to use an external driver IC, such as the Siliconix D469A. The D469A can switch very large devices such as the SMM20N50 (500 V, 0.3 Ω) in approximately 100 ns.

Applications

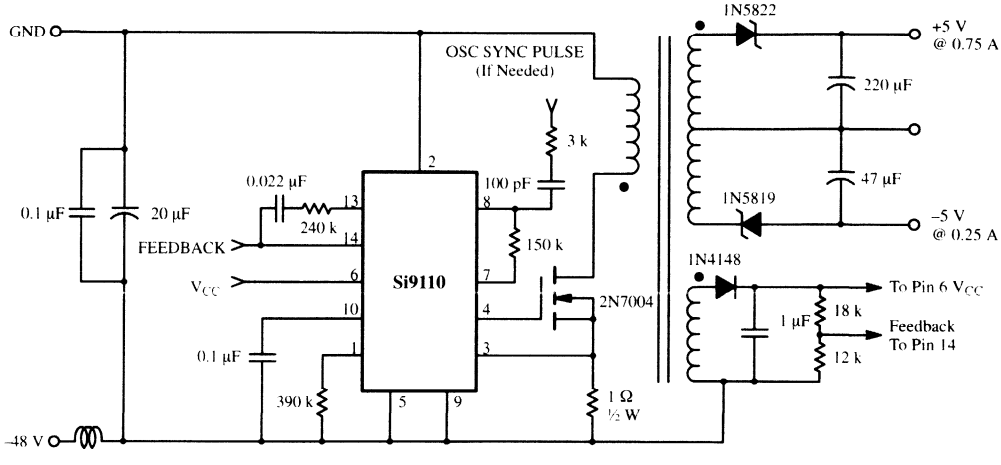


Figure 4. 5-Watt Power Supply for Telecom Applications

Designing DC/DC Converters with the Si9110 Switchmode Controller

James Blanc

In distributed power systems and battery-powered equipment, the advantages of MOS over bipolar technology for pulse-width modulation (PWM) controllers are significant. First, by using a BiC/DMOS power IC process, a high-voltage DMOS transistor can be integrated with a CMOS PWM controller to serve as a pre-regulator stage. This reduces the number of external components by permitting the power controller IC to interface directly to the power bus.

The second advantage of MOS is speed. Bipolar PWM controllers can be made fast, but only with a significant increase in supply current. Logic gate delays of 5 ns are readily achievable using 5-µm CMOS, comparator propagation delays are in the 50- to 100-ns range, and the supply current is maintained *below 1 m*A.

How does speed translate into power supply performance? The answer is first in reliability and second in power density. If the delay time is long between the sensing of an overcurrent condition in the power switch and the turn-off of the switch, then the peak and RMS current values reach excessive levels and the switch fails. A well-designed power supply should tolerate a continuous short circuit on any output. To accomplish this with a slow controller IC, extra protection circuitry or an oversized switching transistor and heatsink are required. But that costs money.

Power supply density (often expressed as output power in watts divided by volume in cubic inches) has steadily been increasing over the past 5 to 10 years. By increasing the switching frequency, the size of magnetics and filter capacitors has been reduced, allowing smaller and less expensive power supplies to be built. To increase the switching frequency to the 100- to 500-kHz range and still achieve high reliability requires that the current limit delay time be kept under approximately 100 ns.

The first BiC/DMOS switchmode controller IC to meet these requirements is the Si9110. Its 500-kHz rating for maximum switching frequency is fully usable, thanks to the high-speed current limit comparator and the efficient output driver stage, which essentially eliminates the shoot-through current found in bipolar totem-pole circuits. The DMOS transistor in the input pre-regulator has a breakdown voltage rating of 120 V, which provides ample headroom for operation from typical bus voltages in distributed power systems (where 12, 24, 48, and 60 V are frequently encountered).

The appeal of such distributed power processing systems is in their flexibility and reliability. By bussing power at a higher voltage, smaller conductors can be used, as well as fewer connector pins to get the power to where it is needed—on the circuit card. An on-card power supply can then provide the voltages needed in that part of the system. The power bus voltage is usually chosen to be low enough to eliminate the need for safety agency approvals, and a battery can be connected through a diode to the power bus to provide emergency back-up. The distributed power approach is employed in telecom systems, large minicomputers, and in other applications where reliability is a primary concern.

To illustrate some of the performance capabilities of this BiC/DMOS switchmode controller IC, a 15-W forward converter design is presented. The converter provides +5-V and ±12-V outputs from a 9- to 36-V input range. This permits the power supply to operate from 12-V or 24-V batteries, or from a 28-V aircraft power source. Before describing the forward converter example, it is instructive to review the operation of each of the Si9110 switchmode controller's functional blocks.

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Functional Description

Pre-Regulator

A BiC/DMOS power integrated circuit process is used to integrate a high-voltage (120-V rated) lateral DMOS transistor with the CMOS PWM controller. By using an ion implant to shift the gate threshold to a negative value, as shown in Figure 1, the transistor is made to operate as a depletion-mode device. This eliminates the need for a pull-up voltage above V_{IN} to turn the device on, and an amplifier and voltage reference can be used to implement a linear regulator, as shown in Figure 2. The CMOS circuitry is thus protected from transients which appear on the input power bus.

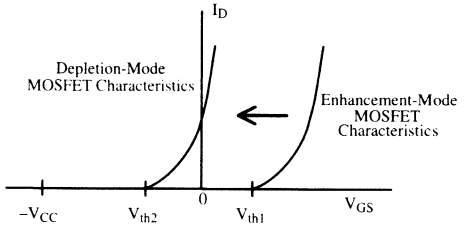


Figure 1. Depletion-Mode MOSFET Characteristics

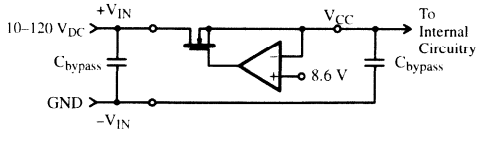


Figure 2. Pre-Regulator/Start-Up Circuit

In some applications it is useful to turn off the pre-regulator after start-up. This is easily accomplished by using an auxiliary winding on the transformer to develop a bootstrap supply voltage. After the converter starts, its own output feeds 10 to 12 V to pin 6 (V_{CC}), and the amplifier pulls the gate of the MOSFET to the $-V_{IN}$ rail. Thus, $V_{GS} = -V_{CC}$, and the device is turned off.

Oscillator

A ring of inverters and internal MOS capacitors forms the oscillator circuit, as shown in Figure 3. This circuit requires only a resistor (no external capacitor) to program the frequency. The internal capacitance is charged towards V_{CC} through R_{OSC}. When the capacitor voltage reaches $V_{CC}/2$, the CMOS logic threshold, inverter INV1 changes state (from high to low), and the INV2 output goes from a low to a high output. The capacitor, C2, provides positive feedback to ensure stable operation without frequency jitter. It also causes the "bump" at the end of the ramp until INV2 can turn on the discharge switch, Q1, to terminate the cycle.

Oscillator synchronization is achieved by prematurely terminating each clock cycle using a positive going pulse capacitively coupled onto the oscillator ramp voltage. The pulse forces INV1 to change states, Q1 discharges C = C1 + C2, and the cycle repeats. An internal flip-flop blanks out the output during every other clock cycle, so the switch duty ratio is limited to a maximum of 50%. Therefore, the oscillator frequency and SYNC pulse repetition rate must be set at two times the switching frequency, f_s.

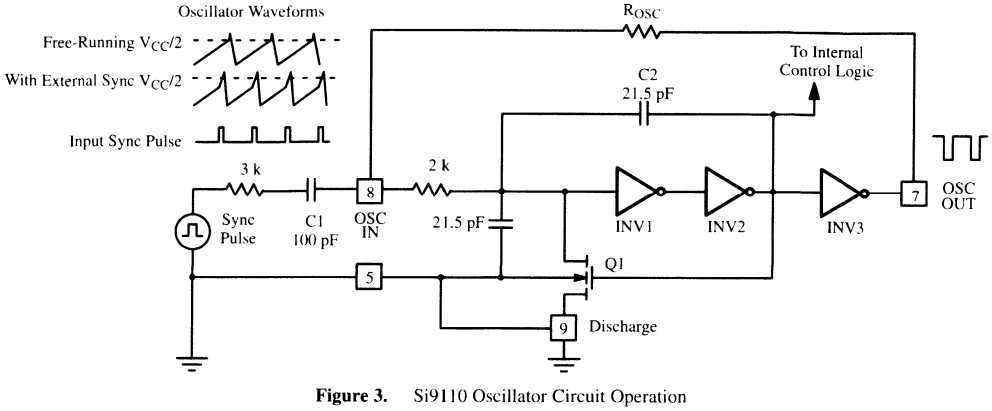


Figure 3. Si9110 Oscillator Circuit Operation

Error Amplifier

The bias resistor connected from pin 1 (BIAS) to pin 5 ($-V_{IN}$) programs the current sources in the analog portion of the current-mode controller – including the error amplifier, the current-mode and current-limit comparators, and the voltage reference. The Si9110 data sheet guarantees the performance of these functions at one value of bias current – 15 µA. It is possible to change the performance characteristics of these functions by changing the bias current, and Appendix A explains how this is accomplished.

The error amplifier circuit employs PMOS transistors in a differential input stage to achieve a high input impedance of 40 MΩ typically (2 MΩ minimum). This input impedance, combined with a 1-kΩ small-signal output impedance, enables the amplifier to be used with feedback compensation, unlike transconductance error amplifiers. The amplifier can source 2 mA and sink 0.140 mA, as can be seen from the output stage equivalent circuit in Figure 4. Yes, an NPN transistor is used here. Most of the PWM controller is CMOS, but the process allows the flexibility of using bipolar devices where they are advantageous.

The error amplifier is unity gain stable with a typical bandwidth of 1 MHz and 60° phase margin. Bias current values of from 5 µA to 50 µA have been tested, and the error amplifier does remain stable over this range. Actually, the bandwidth and phase margin increase somewhat as I_{BIAS} is increased above 15 µA. Higher bias currents may, therefore, be useful when compensating higher frequency converters (above 250 kHz).

Voltage Reference

A buried zener with merged temperature compensating diode (patent pending) is used to achieve stability of 0.25 mV/°C.

The Si9110 voltage reference is trimmed to 4 V plus or minus 1% with a bias current of 15 µA. This voltage varies by about 1% as I_{BIAS} is varied from 5 to 50 µA. If 1% reference accuracy must be guaranteed, I_{BIAS} should be set at 15 µA.

For circuits employing an external reference on the secondary side, such as those used with optically coupled feedback, the Si9111 is an economical approach. Its voltage reference provides a dc bias point at the input to the error amplifier where its 10% accuracy is more than sufficient. The reference accuracy is the only difference between the Si9110 and Si9111.

Comparators

The delay time of the current-limit and current-mode comparators can be modeled as a current source charging an internal nodal capacitance, as shown in Figure 5. The current-mode comparator is intentionally made to be four times slower than the current-limit comparator. In many circuits, this permits the elimination of the RC filter in the current-sense circuit, which is used to prevent false trips by the leading edge current spike. After one of the comparator outputs goes high, there is an additional 20 ns of gate propagation delay before the output driver can begin switching.

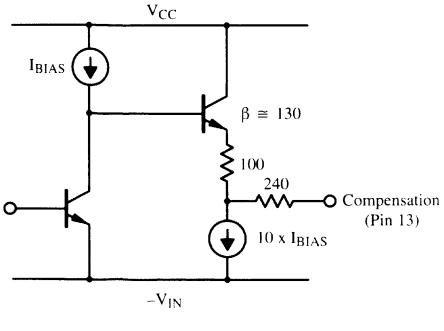


Figure 4. Error Amplifier Output Stage

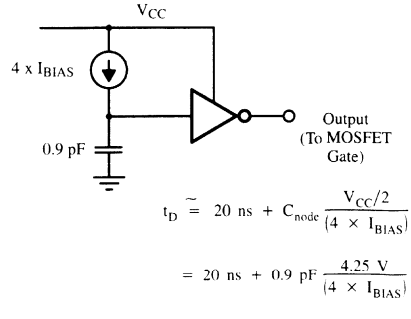


Figure 5. Current-limit Comparator Delay (Equivalent Circuit Model)

The total current-limit delay to output versus I_{BIAS} is shown in Figure 6 for V_{CC} equal to 8.5 V. The delay time is 180 ns for I_{BIAS} = 5 µA, but decreases to 50 ns for I_{BIAS} = 30 µA. As operating frequency is increased, I_{BIAS} may be increased to speed up the current limiting and reduce the minimum MOSFET pulse width. As I_{BIAS} is increased, however, the current-limit trip voltage also increases. Figure 7 shows how the trip voltage is established and how it varies with I_{BIAS}. The current sense resistor and I_{BIAS} determine the peak value of switch current. Since this current limiting is very fast, the trip level of current is usually set to be well above the maximum normal operating current (by a factor of 1.5 to 2). This prevents false trips but still protects the MOSFET switch from exceeding its pulse current ratings.

MOSFET Driver

The driver circuit is a CMOS inverter whose typical characteristics are shown in Figure 8. The n-channel (turn-off) peak drive current is about 20% higher than that of the p-channel (turn-on) device. Although the on-resistance ($r_{DS(on)}$) of the output drive is specified, usually the saturation current (where $\Delta I_D/\Delta V_{DS}$ is very small) determines the switching speed. This is due to the vertical load line of capacitive loads. In other words, the MOSFET gate capacitance appears as a short circuit across the driver's output.

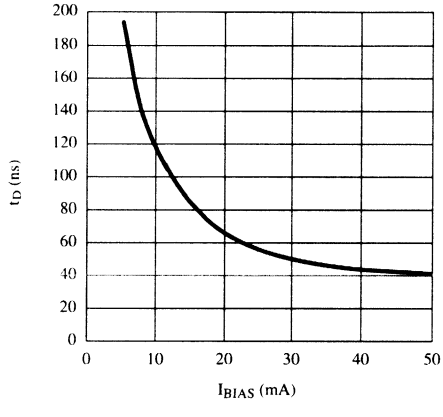
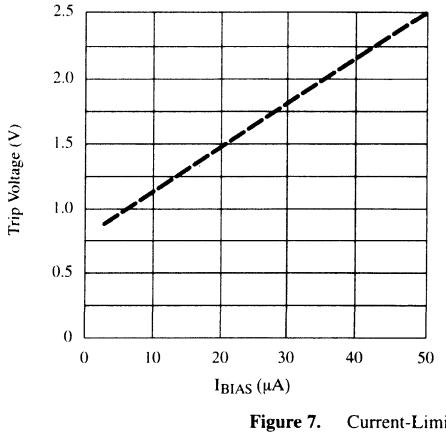


Figure 6. Current-Limit Comparator Delay vs. Bias Current



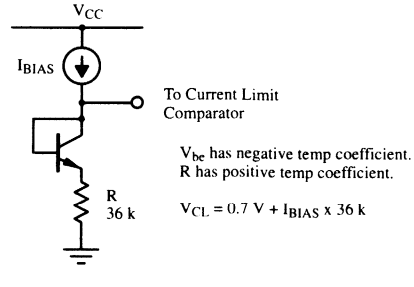


Figure 7. Current-Limit Trip Voltage vs. Programmed Bias Current

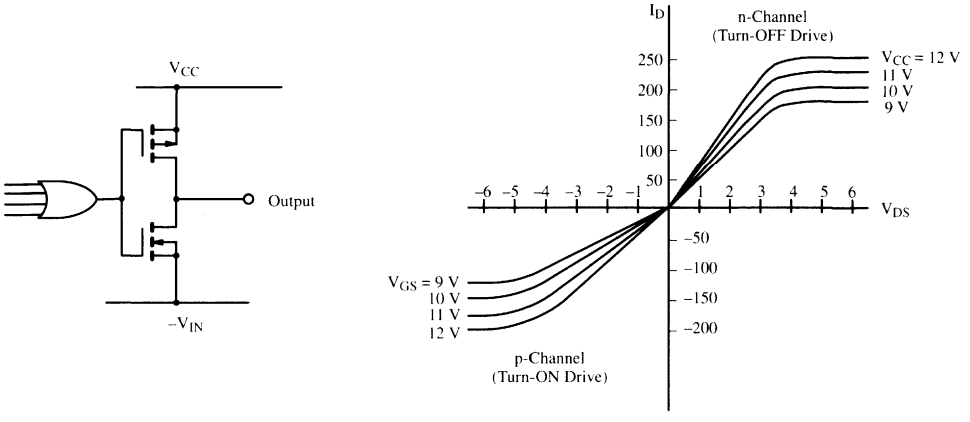


Figure 8. Output Drive Characteristics

The CMOS driver is fast enough to effectively eliminate cross-conduction current during switching transitions, at least when $V_{CC} \leq 10$ V. Above this level, a small amount of cross conduction occurs. Therefore, the greatest gate drive efficiency (approaching 100%) is achieved by keeping $V_{CC} \leq 10$ V, and the gate drive power is given by

$$P_{gate} = Q_g \times f_s \times V_{CC} \quad (1)$$

where

Q_g = MOSFET gate charge
f_s = switching frequency
V_{CC} = supply voltage

Shutdown Logic

The shutdown logic employs an RS flip-flop to disable the output drive. Both the SHUTDOWN and RESET inputs have internal current-source pull-ups (equal to I_{BIAS}), so they can be left open when unused. As long as the SHUTDOWN input is held low, the output is OFF. If the RESET input is hard wired to $-V_{IN}$ (through a normally closed reset button if desired), any LOW input to SHUTDOWN will latch the output in the "off" state. It will remain off until power is recycled (or the reset button is pushed).

Undervoltage Lockout

During start-up, the depletion transistor charges the capacitance connected to the V_{CC} pin with a typical charging current of 18 mA. The output is disabled until V_{CC} reaches the UV lockout voltage (typically 8.1 V). The IC requires less than 0.5 mA of current during this time, since the largest component of supply current is usually for the gate drive (see Appendix B). When V_{CC} reaches 8.1 V, the output is enabled and the MOSFET begins switching. The supply current increases by $Q_g \times f_s$, and V_{CC} charges more slowly until it reaches the pre-regulator voltage (8.5 V). If too much current is drawn from V_{CC}, for instance to supply other circuitry, it may be possible that the converter will be prevented from starting. Or it may oscillate on and off as it starts up, loads down the V_{CC} pin, shuts off, and then repeats this cycle.

Forward Converter

Specifications

Input Voltage: 9 to 36 V

Output Voltages

	Minimum Load (mA)	Maximum Load (A)	Regulation (%)	Ripple (mV_{p-p})
+5	50	1.5	2	150
+12	50	0.310	5	40
–12	20	0.310	5	40

Efficiency:
V_{IN} = 12 V, Full Load: 78% typical, 76% minimum
V_{IN} = 12 V, ½ Load: 82% typical, 80% minimum
Switching Frequency 100 kHz

Circuit Description

The forward converter schematic is shown in Figure 9, and a block diagram of the Si9110/Si9111 controller IC appears in Figure 10 for easy reference. The circuit employs a TL431C voltage reference/amplifier to drive the LED of the opto-isolator, U3. This maintains galvanic isolation between input and output voltages. Since a reference is needed on the secondary side, external to the PWM controller IC, it is not necessary to have a precision reference on the primary side. The voltage reference of the Si9111 is specified at 4 V ±10%, which is accurate enough to establish a dc bias point for the collector current of U3. If galvanic isolation is not required, then the feedback circuitry in the box can be replaced by a voltage divider network, and the input and output grounds must be tied together. In this configuration, the reference accuracy of the PWM controller IC limits the accuracy of the output voltages, and the Si9110 with its 1% reference should be specified. The two ICs are identical in all other respects.

The SMP25N06 switching transistor (Q1) is a 25-A, 60-V MOSFET in a T0-220 package. The breadboard was operated without a heatsink on Q1, even with the power supply output shorted. Three secondaries on the transformer, T1, provide isolated voltages of +5 V and ±12 V. The output inductors are wound on a common core. This reduces the size and cost compared to separate output chokes, as well as improves the response to dynamic loads. The same core size is used for the transformer and the output inductor, the only difference being the air gap required by the inductor to sustain a dc flux. The transformer does not require a gap since the winding, N2, resets the core flux to zero during the "off" time of Q1.

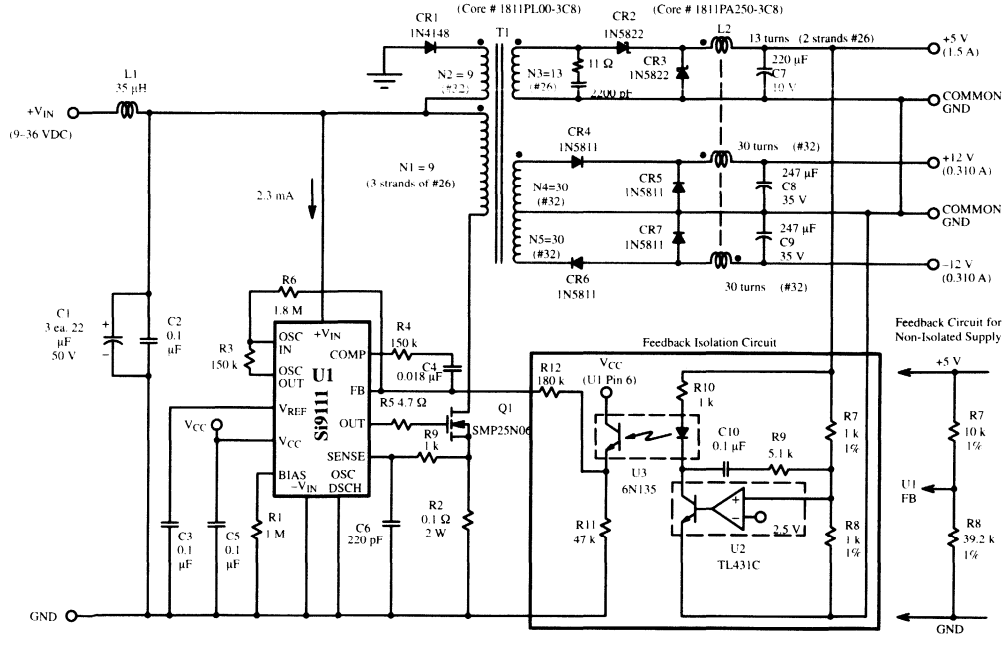


Figure 9. Multiple Output Forward Converter

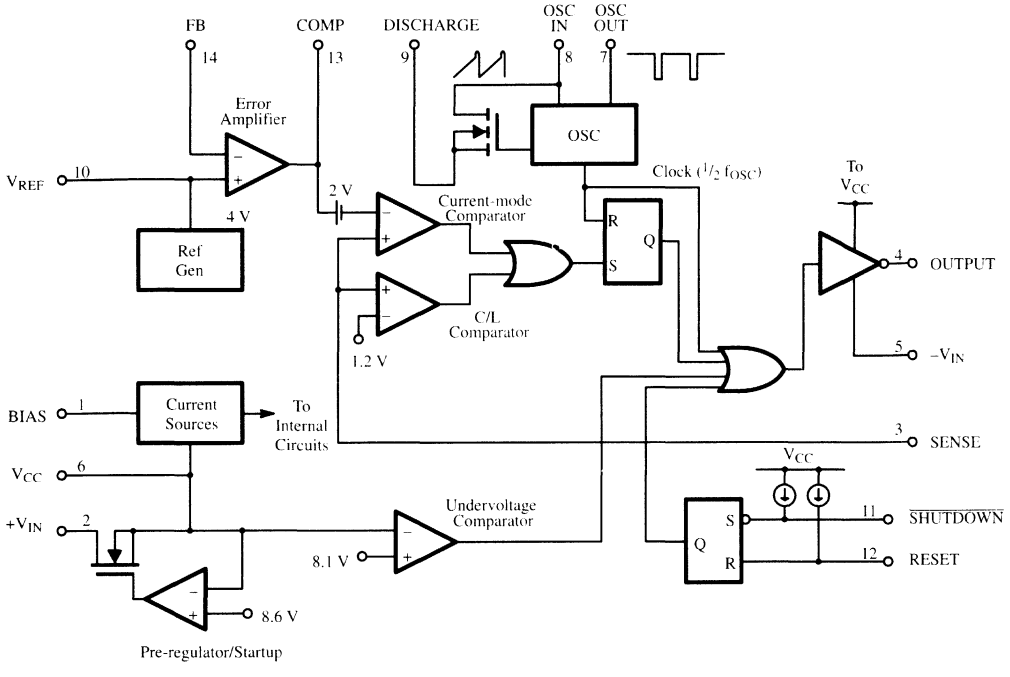


Figure 10. Si9110/Si9111 Block Diagram

Forward Converter Principle

The operating principle of forward converters is illustrated in Figure 11. When the switch, Q1, is on, the input voltage is applied across the primary winding, N_P. If, for example, the input voltage minus the voltage drop across Q1 and R2 is equal to 9 V, then 1 V per turn is applied across the primary. Since the same magnetic flux links all of the windings, the volts/turn is constant by Faraday's Law [$V = -N(d\phi/dt)$].

Therefore, V_{S1} equals 13 V, and V_{S2} and V_{S3} equal 30 V. The LC filter has a cut-off frequency well below the switching frequency, so that the average value of the pulsed secondary voltage appears at the output. For V_1 to equal 5 V, the duty ratio, neglecting diode drops, is given by

$$D = \frac{V_1}{V_{S1}} = \frac{5\ V}{13\ V} = 0.385 \qquad (2)$$

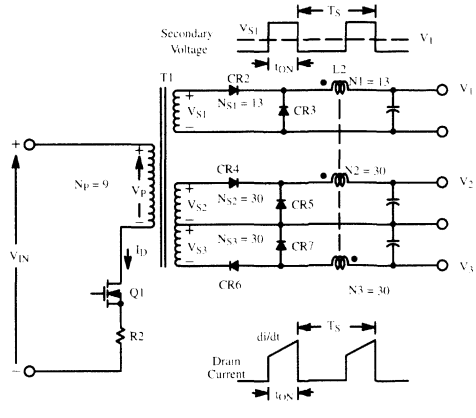


Figure 11. Forward Converter Operating Principle

The control loop will force the duty ratio to the value required to make the regulated output equal to 5 V. If the duty ratio equals 0.385, the secondary voltages V_2 and V_3 are given by

$$V_2 = V_3 = V_{S2} \times D = (30)(0.385) = 11.5\ V \qquad (3)$$

This is the ideal case. The diode drops cause the duty ratio to be higher, and V_2 and V_3 are very close to 12 V. (The measured value was 12.1 V.) When Q1 turns off, the free-wheeling diodes CR3, CR5, and CR7 carry the inductor currents. Again, if diode drops are neglected, each output voltage appears across its corresponding inductor winding. Since the volts per turn must be constant on each winding of L2, the number of turns must be proportional to the output voltage. Therefore, the number of turns and the inductance of each winding cannot be arbitrarily assigned as they can be for individual output chokes. The ratio of turns on L2 must be an integer multiple of the T1 secondary windings. In this case, the integer is 1. The amount of inductance is then determined by the core gap, specified as inductance per 1000 turns; 250 mH per 1000 turns was used, giving an inductance for the 5-V inductor as determined from

$$L_{5V} = 250\ mH \left(\frac{13}{1000}\right)^2 = 42\ \mu H \qquad (4)$$

Therefore, the current slope during the "on" time of Q1 (referred to the primary side of T1) is given by

$$\frac{di}{dt} = \left(\frac{13}{9}\right)\left(\frac{13\ V - 5\ V}{42\ \mu H}\right) = 0.275\ A/\mu S \qquad (5)$$

This current ramp is sensed by R2 to give a voltage ramp input to pin 3 of the Si9111. The current-mode comparator changes states and turns the MOSFET switch off when this sense voltage exceeds the control voltage, V_C, from the output of the error amplifier. Thus, the peak inductor current is controlled on a cycle-by-cycle basis. The same current sense signal is also compared to an internally-generated reference of 1.2 V by the current-limit comparator. This comparator is made four times faster than the current-mode comparator to minimize the delay time required to turn the MOSFET off when an overcurrent condition exists. Such dual-threshold current sensing enables power supply designs that can tolerate shorted outputs for an indefinite period. If the short is removed, then the converter returns to normal operation.

Measured Circuit Performance

Figure 12 shows how the power supply efficiency varies with load. Under the low-line condition (V_{IN} = 9 V), the full load efficiency is 77%. At higher input voltages, the conduction losses in the MOSFET and sense resistor are reduced, permitting full-load efficiency to exceed 80%. High efficiency at light loads is permitted by the CMOS controller's low supply current. At V_{IN} = 9 V, only 2.3 mA • 9 V = 20.7 mW are required by the Si9111.

The circuit operation at V_{IN}= 18 V with a 80% load is illustrated by the waveforms in Figure 13. The control voltage out of pin 13 is ac-coupled and shown above the current sense voltage. The downward slope of V_C is due to the slope compensation resistor connected between pin 8 and pin 14. Slope compensation is explained below in the section on loop analysis and in References 1 and 2.

When the +5-V output is shorted to ground, the waveforms appear as in Figure 14. The error amplifier output, V_C, goes to the positive rail, so the current-mode comparator would allow the duty ratio to increase to 50%. However, the faster current-limit comparator trips at about 9 A, and the duty ratio is limited to less than 10%.

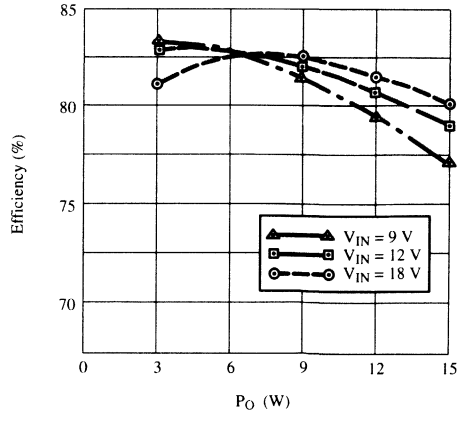
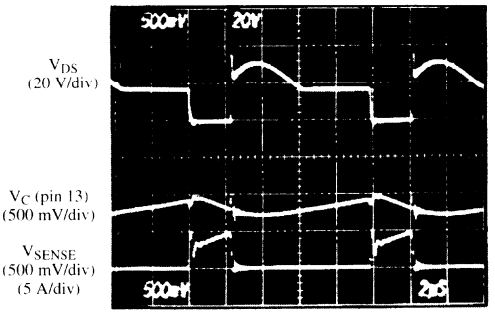


Figure 12. Percent Efficiency vs. Load Current



Loads: 1.2 A @ +5 V
0.25 A @ ± 12 V
V_{IN} = 18 V

Figure 13. Forward Converter Waveforms

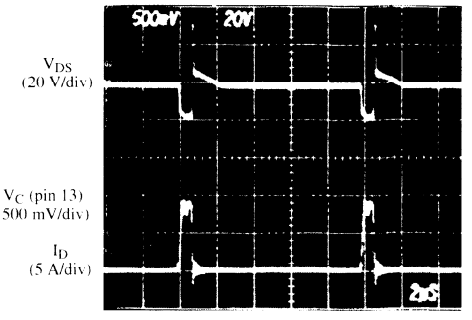


Figure 14. Forward Converter Waveforms with +5 V Output Shorted to GND (V_{IN} = 18 V)

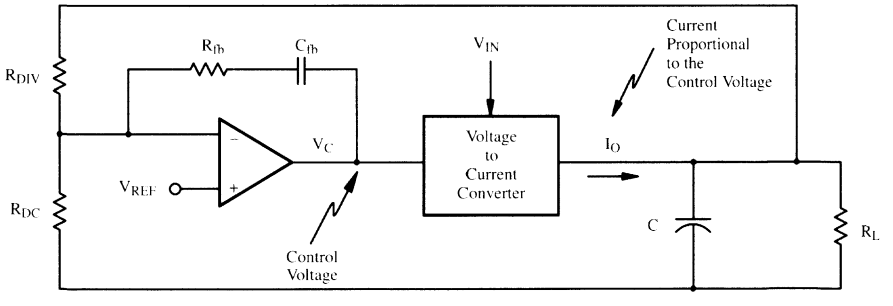


Figure 15. Power Converter with Current-mode Control

Control Loop Analysis

Current-Mode Control

Current-mode control of switching power converters offers several advantages over voltage-mode control. The reliability improvement offered by fast cycle-by-cycle current limiting was discussed above. A second major advantage of current programming is improved dynamic response of the regulator loop while at the same time requiring simpler error amplifier compensation.

The basic objective of current-mode control is to make the power stage behave as a voltage-to-current converter (transconductance amplifier), as shown in Figure 15. To regulate the output voltage, a feedback loop is employed. The control voltage, V_C , is generated by an error amplifier which compares the output voltage to a precision reference, just as in voltage-mode control.

There are several methods for implementing the transconductance power amplifier function—all of them employ an inner current feedback control loop.

The most common method uses a constant frequency clock and peak current sensing, as shown in Figure 16. A clock pulse initiates turn-on of the MOSFET switch, and current ramps up in the output inductor. This current, reflected through the transformer turns ratio, is sensed by the resistor in the MOSFET source to produce a voltage analog of the inductor current. When the voltage ramp reaches the control voltage, V_C, the current-mode comparator sets the latch and turns off the switch. In this way the inner current control loop programs the inductor current in proportion to the control voltage.

To achieve the same loop bandwidth as a current-programmed power converter, a voltage-mode PWM converter requires an error amplifier with compensation as shown in Figure 17a.

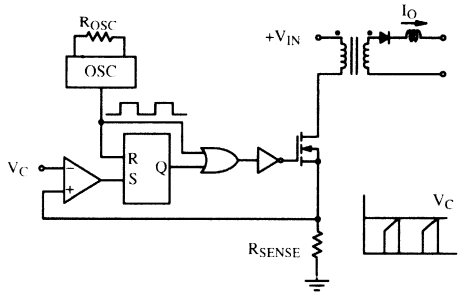


Figure 16. Voltage-to-Current Converter

Current-mode control requires fewer compensation components, as shown in Figure 17b, and the error amplifier has a simpler transfer function. The simplified compensation is due to the elimination of the double pole of the output LC filter, which must be compensated by the double zero at f_1. If the inner current-programmed loop were perfect, then the inductor would behave as a controlled current source, and the power stage would be a single-pole system. This doesn't happen. What does occur is a splitting of the two poles. One is shifted down in frequency to approximately $f_{p1} = \frac{1}{2}\pi R_L C_,$, which is the dominant low-frequency pole. The second pole in the voltage regulator loop occurs at the unity gain crossover frequency, $\omega_C/2\pi$, of the inner current-control loop. The inner current-control loop has less gain than the voltage loop but has more bandwidth.[1] The wide bandwidth of the current loop enables the power converter to respond more rapidly to step changes in load current, even if the small-signal loop bandwidth is the same. It must be realized that step load changes are large signal perturbations between two different small-signal operating points. With inductor current as a controlled parameter, the wideband current loop changes more rapidly between two operating points of load current. The measured response to a step change in load is given in Figure 18. The switch current and output voltage recover to steady-state within about 50 µs, or five switching cycles. Voltage-mode control generally yields a response which is slower by a factor of 5 to 10.

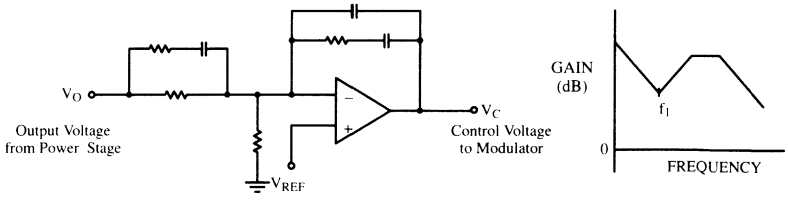


Figure 17a. Error Amplifier Compensation for Maximum Bandwidth Using Voltage-Mode Control

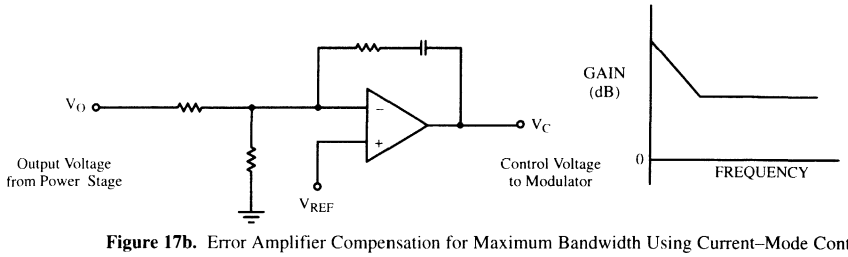


Figure 17b. Error Amplifier Compensation for Maximum Bandwidth Using Current–Mode Control

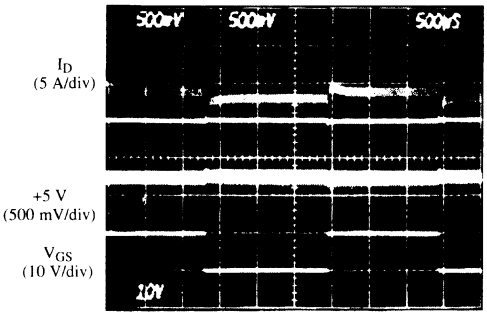


Figure 18. Step Load Response

Small-Signal Analysis

A very concise presentation of small-signal analysis of current-mode control loops can be found in Reference 1. In that paper, the Y-parameter model, shown here in Figure 19, is developed for current-programmed power stages since Y-parameters give an output current for a unit of control voltage input. The inner current loop is demonstrated to be stable, as long as slope compensation is employed for D > 0.5, and therefore, the current loop can be absorbed into the new power stage model. This has the advantage of allowing us to analyze the stability of only one (voltage) control loop.

The derivations will not be presented here, but the resulting control-to-output voltage transfer function of the buck regulator is shown in Figure 20. R_{22} is the low frequency value of the inverse of the output admittance, Y_{22}. It is a measure of how effectively current programming makes the power stage behave as a current source and, consequently, depends heavily upon the gain of the inner current loop. More inductance yields higher current loop gain and larger R_{22}. Smaller R_{22} causes the low frequency gain to be diminished, since R_{22} appears in parallel with the load, R_L. R_{22} also decreases the low-frequency pole by the same factor. In this case, R_{2C} is simply the sense resistance value of 0.1 Ω. For buck-derived converters, it is the ratio of voltage at the current-mode comparator input to inductor current, and it accounts for current amplifier gains and current transformer ratios. The second pole at $\omega_C/2\pi$ depends upon the switching frequency, the amount of slope compensation, and the duty ratio at the dc operating point (remember that this is a small-signal analysis of variations around a dc operating point); it does not depend on the load current.

An easy way to work through the calculations is to form a table, as shown in Figure 21. The voltage-control loop bandwidth, f_{vc}, and phase margin, ϕ_m, are calculated at full load for three different input voltages. The same symbols are used as in reference 1, with the exceptions that the current ramp slopes m_1, m_2, and m_3 are referenced to the current-mode comparator input. The result is the same as long as the current scale factor, R_f, is taken into account.

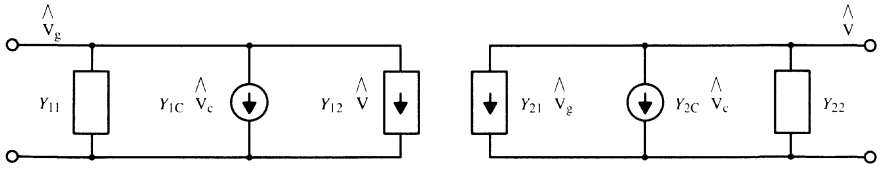


Figure 19. Y-parameter Model for Current-mode Regulators

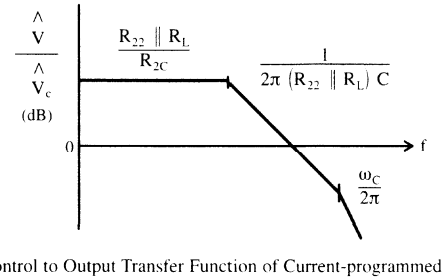


Figure 20. Small-signal Control to Output Transfer Function of Current-programmed Buck Regulators

V_{IN}	Di	M_1 (V/µs)	n	R_{2C}	R_{22}	f_p* (Hz)	$A_{cm} = \frac{R_{22} \parallel R_L}{R_{2C}}$	w_C (krad/s)	f_{VC} (kHz)	ϕ_m (deg)
9	0.59	0.044	1.6	0.1	7.6	141	7.5 (17.5dB)	2 p (33.7)	15.76	52
18	0.78	0.089	1.3	0.1	5.1	147	7.2 (17dB)	2 p (31.4)	15.77	50
32	0.88	0.158	1.16	0.1	4.5	152	7.0 (17dB)	2 p (31.2)	15.85	50

$$* f_p = \frac{1}{2\pi (R_{22} \parallel R_L) C}$$

Figure 21. 15-W Forward-Converter Stability Analysis

Ramp Slope: $m_C = \frac{V_{CC}/2}{T_S/2} = \frac{R_{fb}}{R_{SLOPE}}$

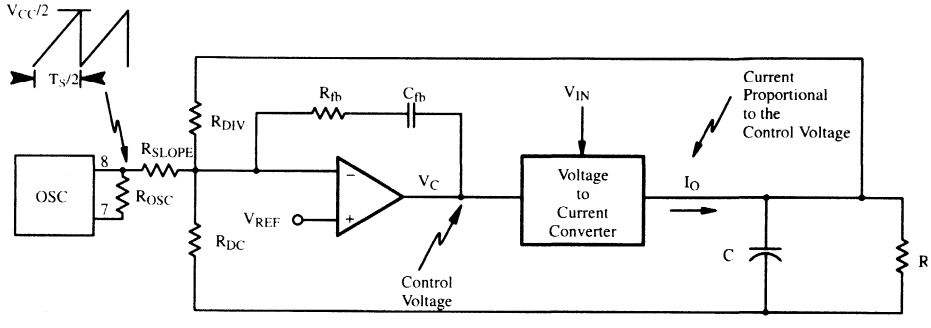


Figure 22. Implementation of Slope Compensation Using the Si9110.

The forward converter is a transformer-isolated derivative of a buck regulator. Therefore, the Y-parameter model for the buck regulator applies here, but the R, L, and C values used must be reflected through the transformer turns ratios. The resulting circuit parameters are

$$R = \frac{5\ V}{1.5\ A}\left(\frac{9}{13}\right)^2 \parallel \frac{12\ V}{0.31\ A}\left(\frac{9}{30}\right)^2 \parallel \frac{12\ V}{0.31\ A}\left(\frac{9}{30}\right)^2$$

$$= 1.6\ \Omega \parallel 3.5\ \Omega \parallel 3.5\ \Omega = 0.83\ \Omega \quad (6)$$

$$L = A_L\left(\frac{N_2}{1000}\right)^2\left(\frac{N_1}{N_2}\right)^2 = 20.3\ \mu H \quad (7)$$

$$C = 220\ \mu F\left(\frac{13}{9}\right)^2 + (47\ \mu F + 47\ \mu F)\left(\frac{30}{9}\right)^2 \quad (8)$$

$$= 1500\ \mu F$$

Slope compensation is achieved by feeding the oscillator ramp voltage into the inverting input of the error amplifier, as shown in Figure 22.

The amount of slope compensation is given by

$$m_C = \frac{V_{CC}}{T_S} \times \frac{R_{fb}}{R_{SLOPE}} = \frac{8.5\ V}{10\ \mu s} \times \frac{150\ k\Omega}{1.8\ M\Omega}$$

$$= 0.071\ V/\mu s \quad (9)$$

This calculation does not take into account the effect of ripple feedback upon slope compensation. For a buck regulator, during the "on" time of the switch, the output ripple voltage is ramping upward due to capacitor ESR. This ramp voltage is amplified and inverted by the error amplifier to provide additional slope compensation. If lower ESR capacitors are used, this effect is diminished. For film or ceramic filter capacitors, the ripple is also phase shifted, since ripple voltage is determined more by C than by ESR.

The slope compensation parameter, n, is given by

$$n = 1 + \frac{2\ m_C}{m_1} \qquad (10)$$

where m_1 is the current ramp slope (times the sense resistance) during t_{ON}, which is calculated from

$$m_1 = \frac{V_{IN}}{L} \times R_f = \frac{V_{IN}}{20.3\ \mu H} \times 0.1\ \Omega \qquad (11)$$

For a buck converter, R_{2C} is simply equal to R_f, the sense resistance.

The conduction parameter K is a measure of how far into continuous conduction the converter is operating. At full load

$$K = \frac{2L}{RT_S} = \frac{2\ (20.3\ \mu H)}{(0.83)\ (10\ \mu s)} = 4.86 \qquad (12)$$

This converter operates heavily into the continuous conduction mode and has a fairly high current-loop gain.

The output resistance parameter is

$$R_{22} = \frac{KR}{nD' - D} \qquad (13)$$

which varies with both input voltage and load. The frequency, f_P, of the power stage low-frequency pole is

$$f_P = \frac{1}{2\pi\ (R_{22} \parallel R_L)\ C} \qquad (14)$$

The low-frequency gain of the power stage is

$$A_{CM} = (R_{22} \parallel R_L)/R_{2C}$$

and the high-frequency pole is given by $\omega_C = \omega_S/\pi n D'$.

Once the gain of the power stage has been determined and plotted, as shown in Figure 23, the objective is to establish values for the error amplifier compensation to provide good loop bandwidth and phase margin. Some typical "rule-of-thumb" numbers are to use a bandwidth of one sixth to one fifth of the switching frequency and a phase margin of 45° to 60°. A series RC network in the feedback of the error amp gives a pole at the origin and a zero at $f_Z = \frac{1}{2}\pi R_{fb}C_{fb}$.

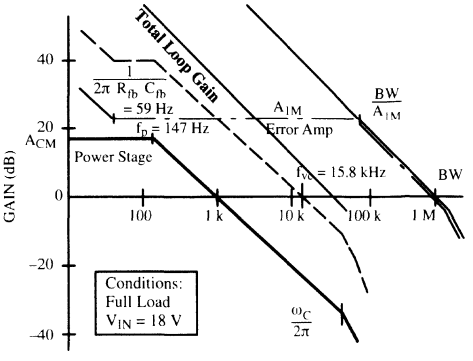


Figure 23. Bode Plot of Small-signal Loop Gain

The error amplifier gain remains constant at

$$A_{1M} = \frac{R_{fb}}{R_{div}} = \frac{R_4}{R_7} = \frac{150\ k\Omega}{10\ k\Omega} = 15\ (\text{or } 23.5\ dB) \qquad (15)$$

between f_Z and the point where the open–loop gain of the error amplifier takes over. This occurs at $A_{OL1} = BW/A_{1M}$, where BW is the error amplifier bandwidth. The gain of the loop is decreased to unity below the poles at $\omega_C/2\pi$, and A_{OL1}, but each can contribute significant phase shift. The voltage loop crossover frequency is calculated from

$$f_{VC} = A_{CM} \times A_{1M} \times f_P \qquad (16)$$

The feedback divider resistor, R_7, was first arbitrarily chosen to be 10 kΩ. (This is for the non-isolated configuration. For analysis of the optical-isolator circuit, see Appendix C.) To achieve $f_{VC} \simeq f_S/6 = 16$ kHz, A_{1M} was calculated from Equation 15. This requires

$$R_{fb} = A_{1M} \times R_{div} = 15 \times 10\ k\Omega = 150\ k\Omega$$

A standard capacitance value is then chosen such that f_Z falls somewhat below f_P. $C_{fb} = 0.018\ \mu F$ places the zero, f_Z, at about 60 Hz.

The phase margin, ϕ_m, of the ideal current-mode converter is 90°. Phase lags due to poles at $\omega_C/2\pi$ and A_{OL1} diminish the phase margin according to

$$\phi m \simeq 90\ \text{deg} - \tan^{-1}\left(\frac{f_{VC}}{\frac{\omega_C}{2\pi}}\right) - \tan^{-1}\left(\frac{f_{VC}}{A_{OL1}}\right) \qquad (17)$$

A more accurate analysis should account for the zero of the capacitor ESR. The tantalum capacitors used here (type 550D from Sprague) will cause a zero at approximately 30 to 50 kHz. This will just about cancel the pole at $\omega_C/2\pi$, and increase the phase margin. Higher ESR will cause the extra zero to fall below f_{VC}, and the loop bandwidth will be increased somewhat.

Magnetics Design

Transformer Core Selection

The core selection method used here employs the core geometry parameter, K_g, as proposed by McLyman.[3] Pot cores were chosen for both the transformer and the coupled inductor, but another design approach using toroids is recommended for applications requiring either the lower profile or the resilience to thermal shock that toroids provide.

Begin by calculating the output power of the transformer.

$$P_O = \Sigma (V_O + V_D) I_O \quad (18)$$

where

$V_O \equiv$ Output Voltage
$V_D \equiv$ Diode Drop
$I_O \equiv$ Output Current

$P_O = (5\ V + 0.5\ V)(1.5\ A) + 2(12\ V + 0.7\ V)(0.31\ A)$
$= 16.1\ W \quad (19)$

The apparent power, P_t, for a single-ended forward converter is

$$P_t = P_O \left(\sqrt{\frac{2}{\eta}} + \sqrt{2} \right) \quad (20)$$

where η transformer efficiency

$$P_t = (16.1) \left(\sqrt{\frac{2}{0.99}} + \sqrt{2} \right) = 45.8\ VA \quad (21)$$

The electrical conditions parameter, K_e, is given by

$$K_e = 0.145\ K_e^2 f^2 B_m^2 \times 10^{-4} \quad (22)$$

where

$K_f \equiv$ Waveform Factor ($\sqrt{2}$ for the forward converter)
$f \equiv$ Operating Frequency
$B_m \equiv$ Maximum Flux Density (0.15 tesla was chosen)

$$K_e = 9.145 \left(\sqrt{2}\right)^2 (10^5)^2 (0.15)^2 \times 10^{-4} = 6525 \quad (23)$$

Finally, the core geometry, K_g, is

$$K_g = \frac{P_t}{2\ K_e\ \alpha} \quad (24)$$

where $\alpha \equiv$ percent regulation (use 1%)

$$K_g = \frac{45.8}{2\ (6525)\ (1)} = 3.5 \times 10^{-3}\ cm^5 \quad (25)$$

This K_g calculation is based upon an assumed window utilization factor, K_u, of 40% or 0.4. This is difficult to achieve using small pot cores. Assuming a 25% window area, the core geometry is adjusted by

$$K_{g(new)} = (0.4/0.25)\ (3.5 \times 10^{-3}) = 5.6 \times 10^{-3}\ cm^5 \quad (26)$$

The closest pot core is number 1811PL00 from Ferroxcube, for which $K_g = 6.0 \times 10^{-3}\ cm^5$.

The toroidal cores which most nearly meet the transformer requirements are numbers T8-16-8 and T10-20-5 from TDK. Their K_g's are 0.007456 cm^5 and 0.007536 cm^5, respectively.

Transformer Winding Design (First Iteration)

Refer to Figure 11 for the nomenclature used here. The number of primary turns is calculated from Faraday's Law, which states that $V = -N(d\phi/dt)$.

$$\frac{V_p}{N_p} = A_C \frac{B_{max}}{t_{ON}} \quad (27)$$

$$N_p = \frac{V_p \times t_{ON}}{B_{max} \times A_C} \quad (28)$$

where

$A_C \equiv$ Cross-sectional Area of Core
$B_{max} \equiv$ Maximum Flux Density
$t_{ON} \equiv$ MOSFET On-time ($t_{ON} = D \times T_S$)

Design for $D_{max} = 0.475$ at $V_{IN} = 9$ V. V_p is calculated from

$$V_p = V_{IN} - I_D \times (r_{DS(on)} + R_{SENSE}) \quad (29)$$

$$I_D \simeq \frac{\left(\frac{P_O}{\eta}\right)}{V_{IN} \times D} = \frac{\left(\frac{15\ W}{0.8}\right)}{(9\ V)\ (0.475)} = 4.4\ A \quad (30)$$

$$V_p = 9 - 4.4\ (0.08 + 0.10) = 8.2\ V \quad (31)$$

and

$$N_p = \frac{(8.2\ V)\ (4.75\ \mu s)}{(0.15\ T)\ (0.433 \times 10^{-4}\ m^2)} = 6\ turns \quad (32)$$

Calculate the secondary turns as follows:

$$V_O = [(V_p)\ (N_S/N_p) - V_D] \times D \quad (33)$$

If $V_O = V_1 = 5$ V, $D = 0.475$, and $V_p = 8.2$ V, then $N_{S1} = 8.07$. (Assume the diode drop is 0.5 V for Schottky diodes and 0.7 V for fast recovery P-N diodes.)

Eight turns is close enough. Now find the number of turns for the 12-V secondary. During the off-time, the output voltages appear across each coupled inductor winding, which must have the same turns ratios as the transformer secondaries. Therefore,

$$\frac{5\ V + 0.5\ V}{N_{S1}} = \frac{12\ V + 0.7\ V}{N_{S2}} \quad (34)$$

$N_{S1} = 8$ gives $N_{S2} = 18.5$ turns; 18 turns give $V_2 \simeq 11.65$ V, and 19 turns give $V_2 \simeq 12.35$ V. Another option is to set $N_{S1} = 16$ and $N_{S2} = 37$. This will more closely achieve the desired turns ratios, but copper losses will be greatly increased. Remember that if the number of turns is doubled, then the copper cross section must be halved. Resistance, and copper losses, increase by a factor of four. If it doesn't matter that the 12-V output is off a bit, then use $N_p = 6$, $N_{S1} = 8$, and $N_{S2} = 19$.

Inductor Core Selection

The power handling capability of the core is independent of the number of windings used. The simplest approach is to refer all outputs to the 5-V winding and assume that

$$I_O = P_O/V_O = 15\ W/5\ V = 3\ A \quad (35)$$

To operate well into continuous conduction choose $K = 2L/RT_S \geq 4$.

Therefore, $L \geq (4/2)(5\ V/3\ A)10^{-5} = 33\ \mu H$.

This is a ball park number; 25 µH is acceptable, and so is 50 µH. However, if L is larger, a larger core is required for the same core losses.

The peak inductor current, at maximum load, is

$$I = I_{O(max)} + \frac{DI}{2} \quad (36)$$

ΔI is approximately given by

$$\frac{V_1 + V_D}{L_{S1}} = \frac{\Delta I}{t_{OFF}} \quad (37)$$

and the maximum ΔI occurs at maximum V_{IN} where $D \simeq 0.11$, $t_{OFF} = (1 - D)10\ \mu s = 8.9\ \mu s$.

$$\frac{5\ V + 0.5\ V}{33\ \mu H} = \frac{\Delta I}{8.9\ \mu s} \quad (38)$$

The inductor energy storage requirement is

$$E = \tfrac{1}{2}(LI^2) = \tfrac{1}{2}(33\ \mu H)(3.75)^2 = 232\ \mu J \quad (40)$$

The electrical conditions are

$$K_e = 0.145\ (P_O)\ (B_m)^2\ 10^{-4} = 0.145\ (15)\ (0.3)^2\ 10^{-4} = 19.6 \times 10^{-6} \quad (41)$$

The core geometry requirement is

$$K_g = \frac{(E)^2}{K_e \alpha} = \frac{(232\ \mu J)^2}{(19.6 \times 10^{-6})\ (1)} = 0.00275\ cm^5 \quad (42)$$

for 1% regulation. Adjust this for a 25% window utilization, and you get

$$K_g = \frac{0.4}{0.25}(0.000275) = 4.4 \times 10^{-3}\ cm^5 \quad (43)$$

We can use an 1811 pot core with a standard A_L value (160, 250, or 400 mH/10^3). For a toroid, use a number 55206 molypermalloy powder core, for which K_g = 0.007274 cm^5. The pot core was chosen here.

Inductor Winding Design

The transformer design was left with N_{S1} = 8 and N_{S2} = 19, which causes the 12-V output to be about 12.35 V. If A_L = 400 mH/1000 turns is used,

$$L_{S1} = (8/1000)^2 (0.4) = 25.6\ \mu H \quad (44)$$

This gives

$$K = \frac{2L}{RT_S} = \frac{2\ (25.6\ \mu H)}{(1.67)\ (10^{-5})} = 3.1 \quad (45)$$

which is still well into continuous conduction ($K_{crit} = D' =$ 1 – D for buck converters).

It could be done this way, but to make the 12-V output come out closer to 12 V, try some other turns ratios. N_{S1} = 13 and N_{S2} = 30 gives:

$$V_2 = (5.5/13)30 - 0.7 = 11.99\ V \quad (46)$$

A_L = 250 mH/1000 turns gives

$$L_{S1} = (13/1000)^2 (0.25) = 42\ \mu H \quad (47)$$

The maximum flux density is found from

$$L = \frac{\lambda}{I} = \frac{N\phi}{I} = \frac{NB_m A_C}{I} \quad (48)$$

$$Bm = \frac{LI}{NA_C} = \frac{(42\ \mu H)\ (3.75\ A)}{(13)\ (0.433 \times 10^{-4})} = 0.28\ T \quad (49)$$

Saturation occurs above 0.3 T = 3000 gauss, so this flux level is acceptable. Apportion the window area according to the output power of each winding. Total copper area is 0.25 W_A, where W_A = 0.285 cm^5 is the total window area. The copper cross section for the 5-V winding is

$$A_{CU} = \frac{(0.25)\ (0.285\ cm^2)}{30\ turns} \times \frac{(5\ V)\ (1.5\ A)}{15\ W} \quad (50)$$

$$= 2.74 \times 10^{-3}\ cm^2$$

Use two strands of AWG26 magnet wire, for which the copper area is

$$A_W = (2)\ (1.28 \times 10^{-3}\ cm^2) = (2.56 \times 10^{-3}\ cm^2) \quad (51)$$

for the 12-V winding,

$$A_{CU} = \frac{(0.25)\ (0.285\ cm^2)}{30\ turns} \times \frac{(12\ V)\ (0.31\ A)}{15\ W}$$

$$= 0.59 \times 10^{-3}\ cm^2 \quad (52)$$

Use one strand of AWG30, for which A_W = 0.507 x 10^{-3} cm^2.

Transformer Winding Design (Revisited)

As shown in the above analysis, the transformer and inductor designs are interdependent when coupled inductors are used. Calculations are made based upon some reasonable assumptions, and the results may not give the desired outcome (such as a fractional turn or a saturated core). Then choices must be made which are consistent with the requirements of the end application. The choice made here was to set the output voltages as close as possible to 5 and ±12 V.

The transformer secondary turns are N_{S1} = 13 and N_{S2} = 30. The primary turns are found from

$$V_S = V_O/D + V_D = V_p\ (N_S/N_p) \quad (53)$$

$$V_s = \frac{5\ V}{0.475} + 0.5 = 11\ V = 8.2\ V\left(\frac{13}{N_p}\right) \quad (54)$$

N_p = 9.67 turns

Set N_p = 9 turns so that the converter will continue to regulate down to V_{IN} = 9 V. Again, apportioning the copper according to power level (and equally split between primary and secondary) gives the following winding configuration.

Winding Turns Wire Size		
Primary	9	3 Strands AWG26
RESET	9	1 Strand AWG32
+ 5 V	13	1 Strand AWG26
+12 V	30	1 Strand AWG32
–12 V	30	1 Strand AWG32

The primary and RESET windings were wound together (multifilar) over the bobbin, followed by the 5-V output. The ±12-V windings were wound bifilar over the 5-V winding.

Prototyping Hints

A schematic and a parts list do not provide sufficient information to enable a CAD operator to lay out a switching power supply. Parasitic inductances and capacitances, which do not appear on the schematic, can cause major differences in performance. The number of layout iterations can be reduced (down to one with experience) if the following guidelines are followed.

1) Use a ground plane. However, do not assume that the ground plane impedance is zero so that you can ignore the need for good component placement. Every component cannot be placed near every other component. Know which components should be grouped closely together and when close proximity is unnecessary.

2) Keep loop areas small where the current changes rapidly. Loop inductance is proportional to loop area. Inductive voltage spikes are proportional to inductance, i.e, V = Ldi/dt. For example, the loop from C1, through the T1 primary, Q1, R2, and back to the bottom end of C1 carries a current which undergoes a high rate of change. Reducing this loop area reduces noise on the input power lines. Other examples are the loops defined by each secondary winding and the corresponding output rectifiers. Cross regulation of the ± 12-V outputs is worsened by the inductance of these loops. Conversely, the inductance of the loop defined by CR3, L2, and C7 is not critical. The parasitic inductance in series with an inductor is of little consequence.

3) Keep noise-sensitive nodes away from noise generators. The drain voltage of Q1 changes rapidly. If the trace between T1 (primary) and Q1 (drain) runs adjacent to the feedback input (pin 14) of U1, then noise is capacitively coupled into the feedback. The noise current is proportional to the parasitic capacitance by i = Cdv/dt. Injected noise currents are worse when the driving point impedance is high. Pins 1, 13, and 14 of the switchmode controller are such high-impedance nodes. Too much noise injection causes a random instability in the control loop.

Following these guidelines reduces headaches as well as costly design time. Using BiC/DMOS PWM controllers reduces component count and failure rates of dc/dc converters in distributed power systems.

References

1) Middlebrook, R.D., "Topics in Multiple-Loop Regulators and Current-Mode Programming," IEEE Power Electronics Specialists Conference, 985 Record, pp. 716-732 (IEEE Publication 85CH2117-0).

2) Hsu, et al., "Modelling and Analysis of Switching DC-to-DC Converters in Constant-Frequency Current-Programmed Mode," IEEE Power Electronics Specialist Conference, 1979 Record, pp. 284-301, (IEEE Publication 79CH1461-3 AES).

3) McLyman, Col. W. T., "Magnetic Core Selection for Transformers and Inductors," Marcel Dekker,1982.

Appendix A

Proper operation of the Si9110 requires that a programming resistor, R_{BIAS}, be connected from pin 1 to $-V_{IN}$, which is assumed here to be ground. This resistor programs internal current sources in the analog portion of the control circuitry. The value of the bias current depends upon two parameters, V_{CC} and R_{BIAS}, as shown in the circuit provided in Figure 24. The characteristic curve of the PMOS FET follows the familiar square law (I_D is proportional to V_{GS} squared). However, over the region of interest, between 5 µA and 50 µA, the curve can closely be approximated by a straight line, as shown in Figure 25. This line is defined by its slope (50 kΩ) and its point of intersection with the X-axis (3.5 V). The intersection of this curve with the load line defined by V_{CC} and R_{BIAS} determines the value of I_{BIAS}. The load line in Figure 2 identifies the conditions which are specified in the data sheet. When V_{CC} = 10 V and R_{BIAS} = 390 kΩ , I_{BIAS} = 15 µA.

If the pre-regulator is used continuously, as in the forward converter example above, then V_{CC} has a nominal value of 8.5 V. The 1-MΩ bias resistor gives I_{BIAS} = 5 µA. This is the lowest value recommended. On the high end, not much performance improvement in terms of comparator speed is obtained for I_{BIAS} above 30 µA (see Figure 6).

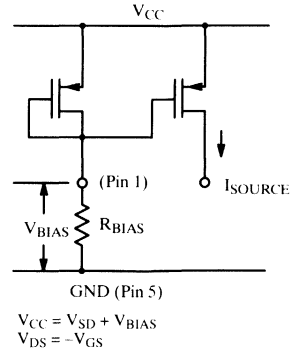


Figure 24. Internal Current Source Programming

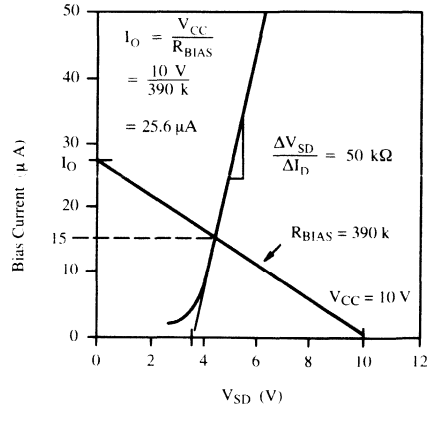


Figure 25. Programmable Current Regulator Characteristics

Appendix B

The supply current requirements of PWM controller ICs are specified at one operating frequency, with no load being driven. In many cases, it may be useful for the circuit designer to determine the supply current requirements needed to drive a specific MOSFET at a given frequency. The Si9110 has been well characterized in this regard.

Equation 1 provides a quick calculation of the supply current drawn by the Si9110.

$$I_{CC} = 60\ \mu A + \left[1.5\ \mu A \frac{f_S}{1000}\right] + [30 \times I_{BIAS}] + [Q_g \times f_S] \quad (1)$$

Each of the components has a straightforward explanation.

a. The voltage reference requires a constant current which is neither frequency nor load dependent. It has a typical value of 60 µA.

b. CMOS circuitry only uses power when a change in logic state occurs. Therefore, the quiescent current requirements of the oscillator and logic gates is proportional to the switching frequency. The proportionality constant is typically 1.5 µA per kHz.

c. The analog circuitry (error amplifier and comparators) utilizes constant-current sources which are programmed by the bias resistor connected from pin 1 to ground. Setting R_{BIAS} equal to 390 kΩ and V_{CC} = 10 V programs the bias current at 15 µA. At this current, the internally generated voltage reference levels (for undervoltage lockout, V_{REF}, and V_{CL}) have the best compensation over temperature. This is also the value at which the data sheet parameters are guaranteed.

d. The output drive current is typically the largest component of I_{CC}. The drive stage has been designed to minimize shoot-through current of the output inverter. Thus, the current requirement can be calculated as $I_{gate} = C_L V_{CC} f_S$. A MOSFET gate is a capacitive load, but a non-linear one. Therefore, MOSFET manufacturers specify the total gate charge required to turn a MOSFET on. In this case, $I_{CC} = Q_{g(on)} \times f_S$, where fs is the switching frequency.

For the forward converter example, the supply current should be

Voltage reference = 60 µA
Oscillator and logic = (1.5 µA)/kHz x 100 kHz = 150 µA
Analog circuitry = 30 x 5 µA = 150 µA
Gate drive 15 nC x 100 kHz = 1500 µA
Total supply current = 1860 µA
The measured value was 2.1 mA.

Appendix C

The gain of the error amplifier plus the feedback isolation circuit is

$$A_V = \left(\frac{R_9}{R_7}\right)(CTR)\left(\frac{R_{11}}{R_{10}}\right)\left(\frac{R_4}{R_{12}}\right)$$

$$= \left(\frac{5.1\ k\Omega}{1\ k\Omega}\right)(0.07)\left(\frac{47\ k\Omega}{1\ k\Omega}\right)\left(\frac{150\ k\Omega}{180\ k\Omega}\right) = 14$$

which is approximately equal to the gain of the non-isolated feedback circuit analyzed above.

The TL431C has a voltage reference with 2% accuracy equal to 2.5 V. R_7 and R_8 were both chosen to be 1 kΩ to establish a dc current much greater than the input bias current of U2, which is 4 µA. C_{10} causes the amplifier of U2 to behave as an integrator with a high dc gain, thus ensuring the accuracy of the output voltage. R_9 causes the gain of U2 to remain constant at R_9/R_7 above the crossover frequency, $1/(2\pi R_9 C_{10})$.

The minimum current transfer ratio (CTR) of U3 is 0.07. CTR is defined as the ratio of output current to anode current for the optical isolator. The small-signal variation of the LED current is equal to the output voltage of U2 divided by R_{10}. The output voltage of U3 is equal to the output current of U3 times R_{11}. Therefore, the gain from the output of U2 to the output of U3 is given by $CTR(R_{11}/R_{10})$. R_{11} was chosen to establish a dc operating current for U3 given approximately by

$$\frac{V_{REF}}{R_{11}} = \frac{4\ V}{47\ k\Omega} = 85\ \mu A$$

Likewise, R_{10} establishes the dc operating point for the LED at approximately 1 mA. R_9 and R_{12} are chosen last to achieve the desired overall gain.

High-Voltage Switchmode Controller

Features

- 9- to 80-V Input Range
- Current-Mode Control
- High-Speed, Source-Sink Output Drive
- High Efficiency Operation (> 80%)
- Internal Start-Up Circuit
- Internal Oscillator (1 MHz)
- $\overline{\text{SHUTDOWN}}$ and RESET

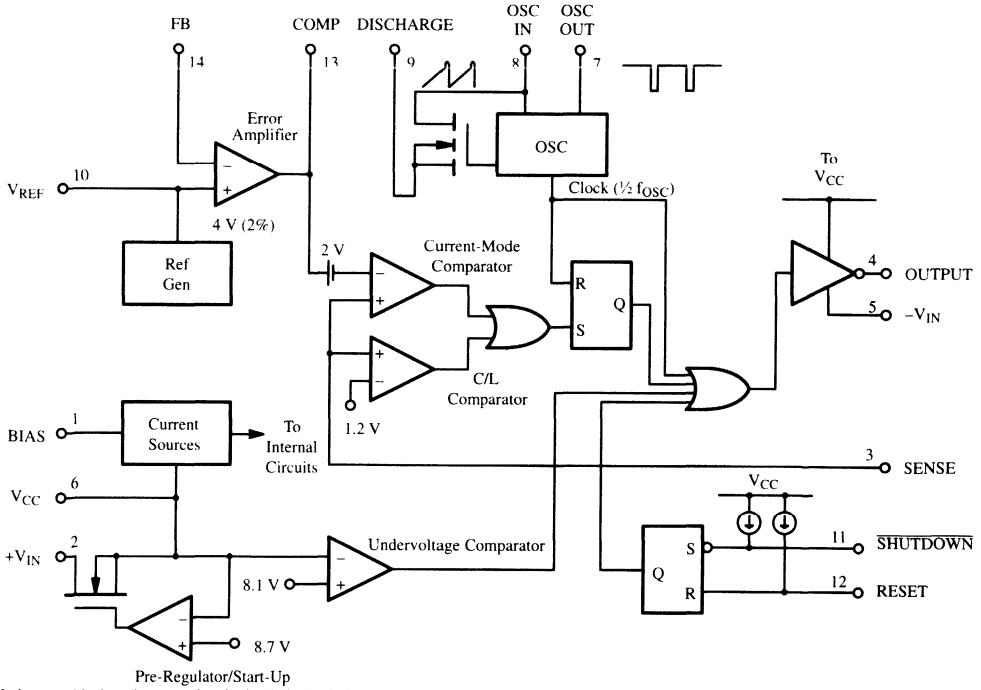
Description

The Si9112 is a BiC/DMOS integrated circuit designed for use in high-efficiency switchmode power converters. A high-voltage DMOS input allows this controller to work over a wide range of input voltages (9- to 80-VDC). Current-mode PWM control circuitry is implemented in CMOS to reduce internal power consumption to less than 10 mW.

A CMOS output driver provides high-speed switching of MOSPOWER devices large enough to supply 50 W of output power. When combined with an output MOSFET and transformer, the Si9112 can be used to implement single-ended power converter topologies (i.e., flyback, forward, and cuk).

The Si9112 is available in 14-pin plastic DIP, and SOIC packages, and is specified over the industrial, D suffix (–40 to 85°C) temperature range.

Functional Block Diagram



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Absolute Maximum Ratings

Voltages Referenced to $-V_{IN}$ ($V_{CC} < +V_{IN} + 0.3$ V)

V_{CC} ..... 15 V

$+V_{IN}$ ..... 80 V

Logic Inputs
(RESET, $\overline{\text{SHUTDOWN}}$, OSC IN) ..... –0.3 V to V_{CC} + 0.3 V

Linear Inputs (FEEDBACK, SENSE) ..... –0.3 V to V_{CC} to 0.3 V

HV Pre-Regulator Input Current (continuous) ..... 25 mA
(Power Dissipation Limited)

Storage Temperature ..... –65 to 150°C

Operating Temperature ..... –40 to 85°C

Junction Temperature (T_J) ..... 150°C

Power Dissipation (Package)a
14-Pin Plastic DIP (J Suffix)[b] ..... 750 mW
14-Pin SOIC (Y Suffix)[c] ..... 900 mW

Thermal Impedance (Θ_{JA})
14-Pin Plastic DIP ..... 167°C/W
14-Pin SOIC ..... 140°C/W

Notes
a. Device mounted with all leads soldered or welded to PC board.
b. Derate 6 mW/°C above 25°C.
c. Derate 7.2 mW/°C above 25°C.

Recommended Operating Range

Voltages Referenced to $-V_{IN}$

V_{CC} ..... 9 V to 13.5 V

$+V_{IN}$ ..... 9 V to 80 V

f_{OSC} ..... 40 kHz to 1 MHz

R_{OSC} ..... 25 kΩ to 1 MΩ

Linear Inputs ..... 0 to V_{CC} – 3 V

Digital Inputs ..... 0 to V_{CC}

Specifications[a]

Parameter	Symbol	Test Conditions Unless Otherwise Specified DISCHARGE = $-V_{IN}$ = 0 V V_{CC} = 9 V, $+V_{IN}$ = 12 V R_{BIAS} = 270 kΩ, R_{OSC} = 330 kΩ	Temp[b]	Limits D Suffix –40 to 85°C Min[d]	Typ[c]	Max[e]	Unit
Reference							
Output Voltage	V_R	OSC IN = – V_{IN} (OSC Disabled) R_L = 10 MΩ	Room Full[e]	3.88 3.82	4.0	4.12 4.14	V
Output Impedance[e]	Z_{OUT}		Room	15	30	45	kΩ
Short Circuit Current	I_{SREF}	$V_{REF} = -V_{IN}$	Room	70	100	130	µA
Temperature Stability[e]	T_{REF}		Full		0.5	1.0	mV/°C
Oscillator							
Maximum Frequency[e]	f_{MAX}	R_{OSC} = 0	Room	1	3		MHz
Initial Accuracy	f_{OSC}	R_{OSC} = 330 k, See Note f	Room	80	100	120	kHz
		R_{OSC} = 150 k, See Note f	Room	160	200	240	
Voltage Stability	Δf/f	Δf/f = f(13.5 V) – f(9.5 V) / f(9.5 V)	Room		9	15	%
Temperature Coefficient[e]	T_{OSC}		Full		200	500	ppm/°C
Error Amplifier							
Feedback Input Voltage	V_{FB}	FB Tied to COMP OSC IN = – V_{IN} (OSC Disabled)	Room	3.92	4.00	4.08	V
Input Offset Voltage	V_{OS}	OSC IN = – V_{IN} (OSC Disabled)	Room		± 15	± 40	mV
Input BIAS Current	I_{FB}	OSC IN = – V_{IN}, V_{FB} = 4 V	Room		25	500	nA
Open Loop Voltage Gain[e]	A_{VOL}	OSC IN = – V_{IN}	Room	60	80		dB
Unity Gain Bandwidth[e]	BW	OSC IN = – V_{IN} (OSC Disabled)	Room	1	1.5		MHz
Dynamic Output Impedance[e]	Z_{OUT}	Error Amp Configured for 60 dB gain	Room		1000	2000	Ω
Output Current	I_{OUT}	Source V_{FB} = 3.4 V	Room		–2.0	–1.4	mA
		Sink V_{FB} = 4.5 V	Room	0.12	0.15		
Power Supply Rejection[e]	PSRR	9 V ≤ V_{CC} ≤ 13.5 V	Room	50	70		dB

Specifications[a]

Parameter	Symbol	Test Conditions Unless Otherwise Specified DISCHARGE = $-V_{IN}$ = 0 V V_{CC} = 9 V, $+V_{IN}$ = 12 V R_{BIAS} = 270 kΩ, R_{OSC} = 330 kΩ	Temp[b]	Limits D Suffix –40 to 85°C Min[f]	Typ[c]	Max[g]	Unit
Current Limit							
Threshold Voltage	V_{SOURCE}	V_{FB} = 0 V	Room	1.0	1.2	1.4	V
Delay to Output[e]	t_d	V_{SENSE} = 1.5 V, See Figure 1	Room		100	150	ns
Pre-Regulator/Start-Up							
Input Voltage	$+V_{IN}$	I_{IN} = 10 µA	Room	80			V
Input Leakage Current	$+I_{IN}$	$V_{CC} \geq$ 9.4 V	Room			10	µA
Pre-Regulator Dropout Voltage	V_{CC}	$+V_{IN}$ = 10 V, R_{LOAD} = 4 k at Pin 6	Room	V_{UVLO} +0.1			V
V_{CC} Pre-Regulator Turn-Off Threshold Voltage	V_{REG}	$I_{PRE-REGULATOR}$ = 10 µA	Room	8.0	8.7	9.4	
Undervoltage Lockout	V_{UVLO}	See Detailed Description	Room	7.2	8.1	8.9	
$V_{REG} - V_{UVLO}$	V_{DELTA}		Room	0.3	0.6		
Supply							
Supply Current	I_{CC}	$C_L \leq$ 75 pF (Pin 4)	Room		0.6	1.0	mA
Bias Current	I_{BIAS}		Room		15		µA
Logic							
$\overline{\text{SHUTDOWN}}$ Delay[e]	t_{SD}	C_L = 500 pF $V_{SENSE} = -V_{IN}$, See Figure 2	Room		50	100	ns
$\overline{\text{SHUTDOWN}}$ Pulse Width[e]	t_{SW}	See Figure 3	Room	50			
RESET Pulse Width[e]	t_{RW}		Room	50			
Latching Pulse Width $\overline{\text{SHUTDOWN}}$ and RESET Low[e]	t_{LW}		Room	25			
Input Low Voltage	V_{IL}		Room			2.0	V
Input High Voltage	V_{IH}		Room	7.0			
Input Current Input Voltage High	I_{IH}	$V_{LOGIC} = V_{CC}$	Room		1	5	µA
Input Current Input Voltage Low	I_{IL}	V_{IN} = 0 V	Room	–35	25		
Output							
Output High Voltage	V_{OH}	I_{OUT} = –10 mA	Room Full	8.7 8.5			V
Output Low Voltage	V_{OL}	I_{OUT} = 10 mA	Room Full			0.3 0.5	
Output Resistance[e]	R_{OUT}	I_{OUT} = 10 mA, Source or Sink	Room Full		20 25	30 35	Ω
Rise Time[e]	t_r	C_L = 500 pF	Room		40	75	ns
Fall Time[e]	t_f		Room		40	75	

Notes
a. Refer to PROCESS OPTION FLOWCHART for additional information.
b. Room = 25°C, Full = as determined by the operating temperature suffix.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum.
e. Guaranteed by design, not subject to production test.
f. C_{STRAY} Pin 8 = ≤ 5 pF.

Timing Waveforms

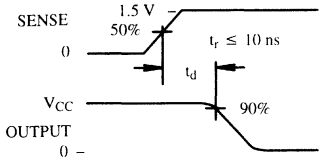


Figure 1.

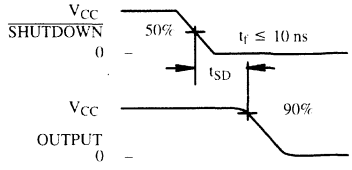


Figure 2.

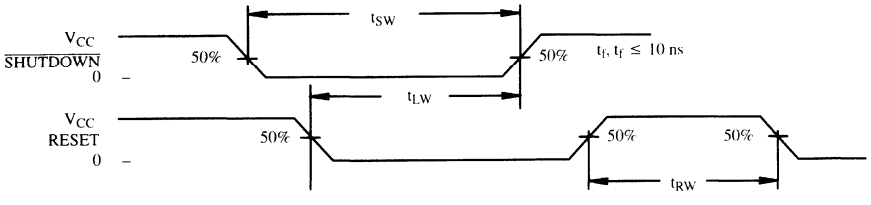
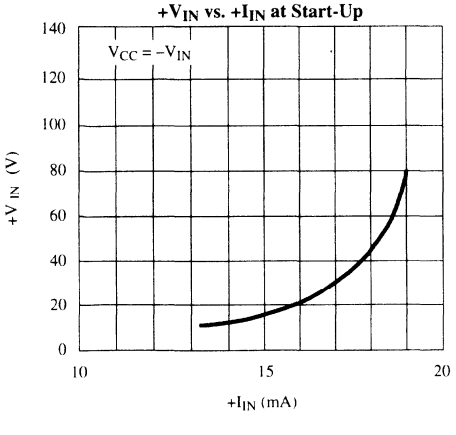
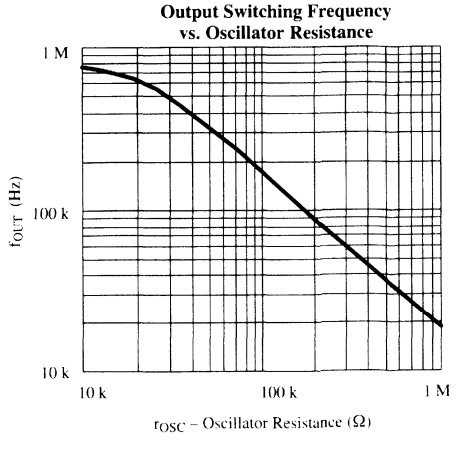


Figure 3.

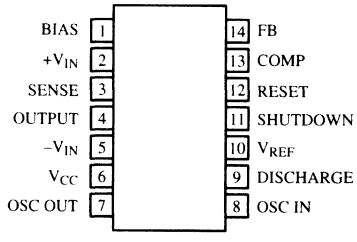
Typical Characteristics





Pin Configurations

Dual-In-Line and SOIC



Top View

Order Numbers
Plastic DIP: Si9112DJ
SOIC: Si9112DY

Detailed Description

Pre-Regulator/Start-Up Section

Due to the low quiescent current requirement of the Si9112 control circuitry, bias power can be supplied from the unregulated input power source, from an external regulated low-voltage supply, or from an auxiliary "bootstrap" winding on the output inductor or transformer.

When power is first applied during start-up, $+V_{IN}$ (pin 2) will draw a constant current. The magnitude of this current is determined by a high-voltage depletion MOSFET device which is connected between $+V_{IN}$ and V_{CC} (pin 6). This start-up circuitry provides initial power to the IC by charging an external bypass capacitance connected to the V_{CC} pin. The charging current is disabled when V_{CC} exceeds 8.7 V. If V_{CC} is not forced to exceed the 8.7-V threshold, then V_{CC} will be regulated to a nominal value of 8.7 V by the pre-regulator circuit.

As the supply voltage rises toward the normal operating conditions, an internal undervoltage (UV) lockout circuit keeps the output driver disabled until V_{CC} exceeds the UV lockout threshold (typically 8.1 V). This guarantees that the control logic will be functioning properly and that sufficient gate drive voltage is available before the MOSFET turns on. The design of the IC is such that the undervoltage lockout threshold will be at least 300 mV less than the pre-regulator turn-off voltage. Power dissipation can be minimized by providing an external power source to V_{CC} such that the pre-regulator circuit is disabled.

BIAS

To properly set the bias for the Si9112, a 270-kΩ resistor should be tied from BIAS (pin 1) to $-V_{IN}$ (pin 5). This determines the magnitude of bias current in all of the analog sections and the pull-up current for the $\overline{\text{SHUTDOWN}}$ and RESET pins. The current flowing in the bias resistor is nominally 15 μA.

Reference Section

The reference section of the Si9112 consists of a temperature compensated buried zener and trimmable divider network. The output of the reference section is connected internally to the non-inverting input of the error amplifier. Nominal reference output voltage is 4 V. The trimming procedure that is used on the Si9112 brings the output of the error amplifier (which is configured for unity gain during trimming) to within $\pm 2\%$ of 4 V. This automatically compensates for input offset voltage in the error amplifier.

The output impedance of the reference section has been purposely made high so that a low impedance external voltage source can be used to override the internal voltage source, if desired, without otherwise altering the performance of the device.

Error Amplifier

Closed-loop regulation is provided by the error amplifier. The emitter follower output has a typical dynamic output impedance of 1000 Ω, and is intended for use with "around-the-amplifier" compensation. A MOS differential input stage provides low input leakage current. The noninverting input to the error amplifier (V_{REF}) is internally connected to the output of the reference supply and should be bypassed with a small capacitor to ground.

Detailed Description (Cont'd)

Oscillator Section

The oscillator consists of a ring of CMOS inverters, capacitors, and a capacitor discharge switch. Frequency is set by an external resistor between the OSC IN and OSC OUT pins. (See Typical Characteristics for details of resistor value vs. frequency.) The DISCHARGE pin should be tied to $-V_{IN}$ for normal internal oscillator operation. A frequency divider in the logic section limits switch duty cycle to $\leq 50\%$ by locking the switching frequency to one half of the oscillator frequency.

Remote synchronization can be accomplished by capacitive coupling of a SYNC pulse into the OSC IN (pin 8) terminal. For a 5-V pulse amplitude and 0.5-µs pulse width, typical values would be 100 pF in series with 3 kΩ to pin 8.

$\overline{\text{SHUTDOWN}}$ and RESET

$\overline{\text{SHUTDOWN}}$ (pin 11) and RESET (pin 12) are intended for overriding the output MOSFET switch via external control logic. The two inputs are fed through a latch preceding the output switch. Depending on the logic state of RESET, $\overline{\text{SHUTDOWN}}$ can be either a latched or unlatched input. The output is off whenever $\overline{\text{SHUTDOWN}}$ is low. By simultaneously having $\overline{\text{SHUTDOWN}}$ and RESET low, the latch is set and $\overline{\text{SHUTDOWN}}$ has no effect until RESET goes high. The truth table for these inputs is given in Table 1.

Table 1: Truth Table for the $\overline{\text{SHUTDOWN}}$ and RESET Pins

$\overline{\text{SHUTDOWN}}$	RESET	Output
H	H	Normal Operation
H	↓	Normal Operation (No Change)
L	H	Off (Not Latched)
L	L	Off (Latched)
↓	L	Off (Latched, No Change)

Both pins have internal current source pull-ups and should be left disconnected when not in use. An added feature of the current sources is the ability to connect a capacitor and an open-collector driver to the $\overline{\text{SHUTDOWN}}$ or RESET pins to provide variable shutdown time.

Output Driver

The push-pull driver output has a typical on-resistance of 20 Ω. Maximum switching times are specified at 75 ns for a 500 pF load. This is sufficient to directly drive 60-V, 25-A MOSFETs. Larger devices can be driven, but switching times will be longer, resulting in higher switching losses.

For applications information refer to AN703.

Si9114A

High-Frequency Switchmode Controller

Features

- 15- to 200-V Input Range
- Current-Mode Control
- Internal Start-Up Circuit
- Latched $\overline{\text{SHUTDOWN}}$
- Soft-Start
- 1.8-MHz Error Amp

Description

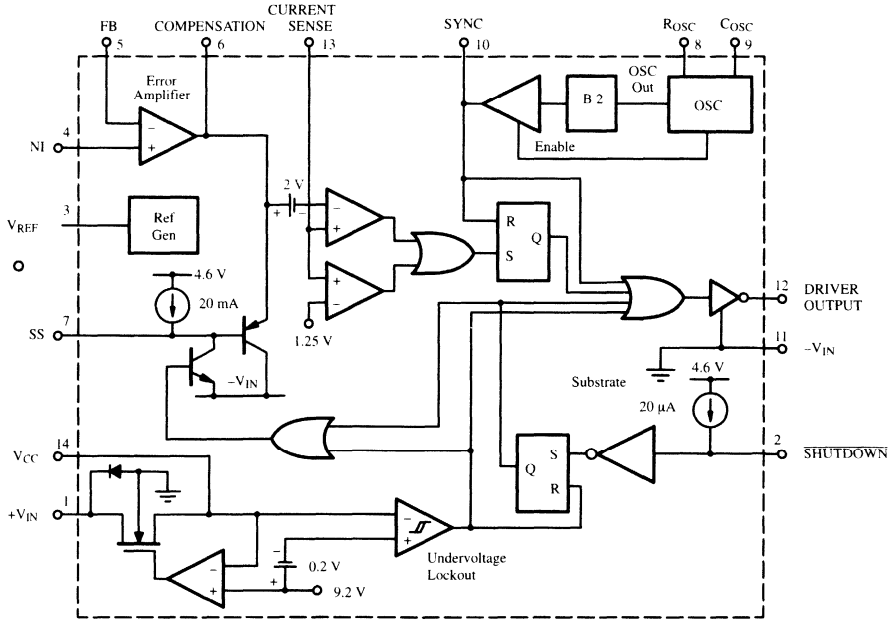
The Si9114A is a BiC/DMOS current-mode pulse width modulation (PWM) controller IC for high-frequency dc/dc converters. Single-ended topologies (forward and flyback) can be implemented at frequencies up to 1 MHz. The oscillator has an internal divide-by-two that limits the duty ratio to 50%. An oscillator sync output allows converters to be synchronized in phase as well as in frequency, in a master/slave configuration.

The output inverter can typically source 500 mA and sink 700 mA. Shoot-through current is all but eliminated to minimize supply current requirements.

The high-voltage DMOS transistor allows the IC to interface directly to bus voltages up to 200 V. Other features include a 1.5% accurate voltage reference, 1.8-MHz (min) bandwidth error amplifier, shutdown logic control, soft-start and undervoltage lockout circuits.

The Si9114A is available in 14-pin plastic DIP and SOIC packages, and is specified over the industrial, D suffix (–40°C to 85°C) temperature range.

Functional Block Diagram



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Absolute Maximum Ratings

Voltages Referenced to $-V_{IN}$
V_{CC} ..... 18 V
$+V_{IN}$ (Note: $V_{CC} < +V_{IN} + 0.3$ V) ..... 200 V
Logic Input ($\overline{SHUTDOWN}$, SYNC) ..... -0.3 V to $V_{CC} + 0.3$ V
Linear Inputs (FEEDBACK, SENSE, SOFT-START) ..... -0.3 V to $V_{CC} + 0.3$ V
HV Pre-Regulator Input Current (continuous) ..... 5 mA
Storage Temperature ..... -65 to 150°C
Operating Temperature ..... -40 to 85°C
Junction Temperature (T_J) ..... 150°C

Power Dissipation (Package)a
14-Pin Plastic Dip (J Suffix)[b] ..... 750 mW
14-Pin SOIC (Y Suffix)[c] ..... 900 mW

Thermal Impedance (Θ_{JA})
14-Pin Plastic Dip ..... 167°C/W
14-Pin SOIC ..... 140°C/W

Notes
a. Device mounted with all leads soldered or welded to PC board.
b. Derate 6 mW/°C above 25°C.
c. Derate 7.2 mW/°C above 25°C.

Recommended Operating Range

Voltages Referenced to $-V_{IN}$
V_{CC} ..... 9.5 V to 16.5 V
$+V_{IN}$ ..... 15 V to 200 V
f_{OSC} ..... 20 kHz to 2 MHz

R_{OSC} ..... 56 kΩ to 1 MΩ
C_{OSC} ..... 47 pF to 200 pF
Linear Inputs ..... 0 to $V_{CC} - 4$ V
Digital Inputs ..... 0 to V_{CC}

Specifications

Parameter	Symbol	Test Conditions Unless Otherwise Specified Oscillator Disabled $-V_{IN}$ = 0 V, V_{CC} = 10 V	Limits D Suffix –40 to 85°C Min[a]	Typ[b]	Max[a]	Unit
Reference						
Output Voltage	V_R	OSC Disabled, T_A = 25°C	3.94	4.0	4.06	V
		OSC Disabled Over Voltage and Temperature Ranges[c]	3.88	4.0	4.12	
Short Circuit Current	I_{SREF}	$V_{REF} = -V_{IN}$		–30	–5	mA
Load Regulation	$\Delta V_R/\Delta I_R$	I_{REF} = 0 to –1 mA		10	40	mV
Oscillator						
Initial Accuracy	f_{OSC}[d]	R_{OSC} = 374 kΩ, C_{OSC} = 200 pF	90	100	110	kHz
		R_{OSC} = 70 kΩ, C_{OSC} = 200 pF	450	500	550	
Voltage Stability[c]	Δf/f	R_{OSC} = 70 kΩ, C_{OSC} = 200 pF Δf/f = [f(16.5 V) – f(9.5 V)] / f(9.5 V)		1	2	%
Temperature Coefficient[c]	OSC TC	$-40 \le T_A \le 85$°C, f_{OSC} = 100 kHz		200	500	ppm/°C
Sync Output Current (Master Mode)	$I_{SYNC(M)}$	$V_{ROSC} \le 5$ V	± 1.0	± 3.0		mA
Sync Output Current (Slave Mode)	$I_{SYNC(S)}$	$V_{ROSC} = V_{CC}$		± 1	± 500	nA

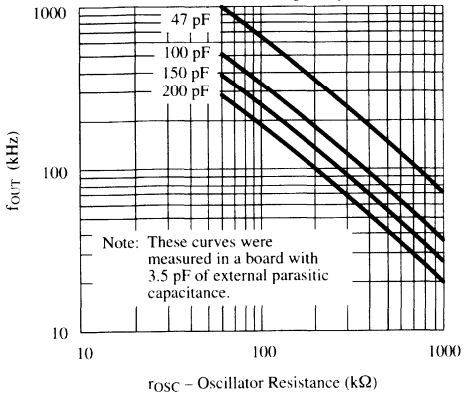
Specifications

Parameter	Symbol	Test Conditions Unless Otherwise Specified Oscillator Disabled $-V_{IN}$ = 0 V, V_{CC} = 10 V		Limits D Suffix –40 to 85°C Min[a]	Typ[b]	Max[a]	Unit
Error Amplifier (C_{OSC} = $-V_{IN}$ OSC Disabled)							
Input BIAS Current	I_{FB}	V_{FB} = 5 V, NI = V_{REF}			<1.0	±200	nA
Input OFFSET Voltage	V_{OS2}				±5	±25	mV
Open Loop Voltage Gain[c]	A_{VOL}			65	80		dB
Unity Gain Bandwidth[c]	BW			1.8	2.7		MHz
Output Current	I_{OUT}	Source (V_{FB} = 3.5 V, NI = V_{REF})			–2.7	–1.0	mA
		Sink (V_{FB} = 4.5 V, NI = V_{REF})		1.0	2.4		
Power Supply Rejection	PSRR	9.5 V ≤ V_{CC} ≤ 16.5 V		50	80		dB
Pre-Regulator/Start-Up							
Input Leakage Current	$+I_{IN}$	$+V_{IN}$ = 200 V, V_{CC} ≥ 10 V			< 1	10	µA
Pre-Regulator Start-Up Current	I_{START}	$+V_{IN}$ = 48 V, t_{PW} ≤ 300 µs, V_{CC} = V_{UVLO}		8	20		mA
V_{CC} Pre-Regulator Voltage	V_{PR}	$+V_{IN}$ = 48 V		8.8	9.1	9.4	V
V_{PR} – V_{UVLO} (Turn-On)	V_{DELTA}			0.1	0.25	0.7	
Undervoltage Lockout Hysteresis	V_{HYST}			0.18	0.28	0.4	
Supply							
Supply Current	I_{CC}	C_{LOAD} ≤ 50 pF	f_{OSC} = 100 kHz		1.5	2.5	mA
			f_{OSC} = 500 kHz		2.2	3.0	
Protection							
Current Limit Threshold Voltage	V_{SENSE}	V_{FB} = 0 V, NI = V_{REF}		1.15	1.23	1.30	V
Current Limit Delay to Output[c]	t_d	V_{SENSE} = 1.5 V, See Figure 1			77	100	ns
$\overline{\text{SHUTDOWN}}$ Logic Threshold	V_{SD}				2.8	0.5	V
$\overline{\text{SHUTDOWN}}$ Delay to Latched Output[c]	t_{SD}	See Figure 2			0.20	1.0	µs
$\overline{\text{SHUTDOWN}}$ Pull-Up Current	I_{SD}	V_{SD} = 0 V		12	23	30	µA
Soft-Start Current	I_{SS}			12	23	30	
Output Inhibit Voltage	$V_{SS(off)}$	Soft-Start Voltage to Disable Driver Output			1.6	0.5	V
MOSFET Driver							
Output High Voltage	V_{OH}	I_{OUT} = –10 mA		9.85	9.9		V
Output Low Voltage	V_{OL}	I_{OUT} = 10 mA			0.05	0.15	
Peak Output Current[c]	I_{SOURCE}	V_{OUT} = 0 V			–400	–200	mA
	I_{SINK}	V_{OUT} = V_{CC}		500	1000		

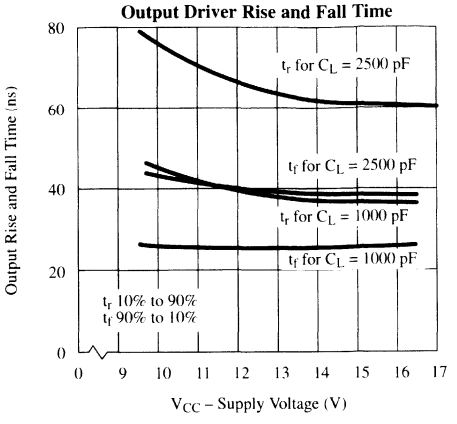
Notes
a. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum.
b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
c. Guaranteed by design, not subject to production test.
d. C_{STRAY} ≤ 5 pF on C_{OSC}.

Typical Characteristics (25°C Unless Otherwise Noted)

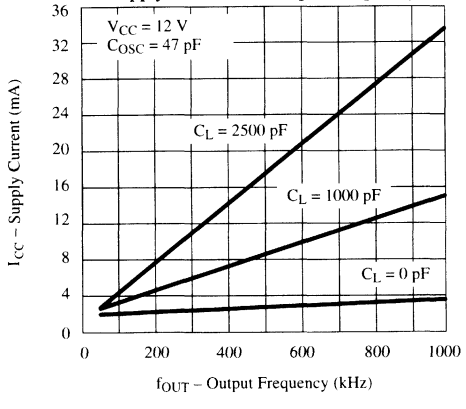
Oscillator Frequency



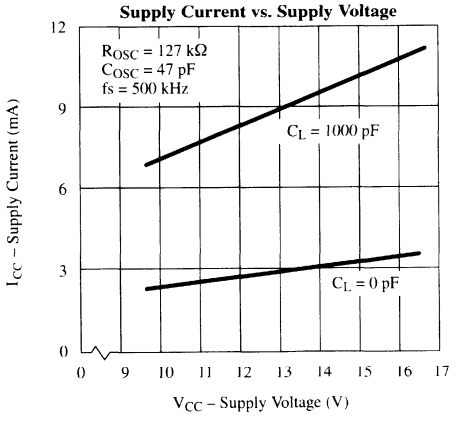
Output Driver Rise and Fall Time



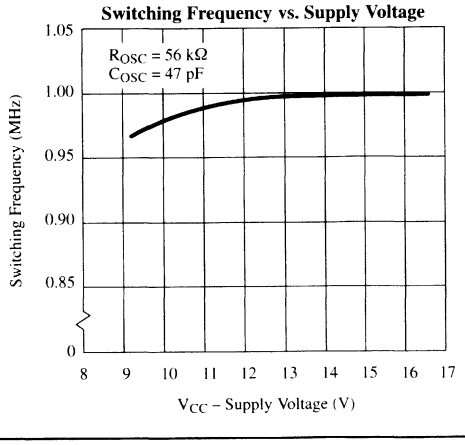
Supply Current vs. Output Frequency



Supply Current vs. Supply Voltage



Switching Frequency vs. Supply Voltage



Timing Waveforms

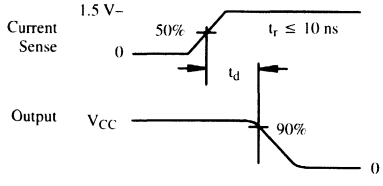


Figure 1.

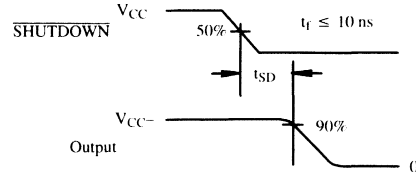
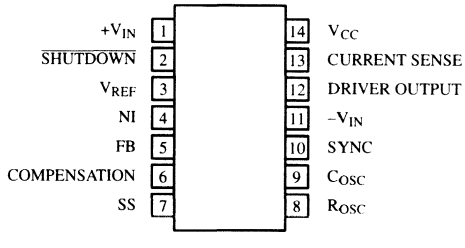


Figure 2.

Pin Configurations

Dual-In-Line and SOIC



Top View

Order Numbers
Plastic DIP: Si9114ADJ
SOIC: Si9114ADY

Applications

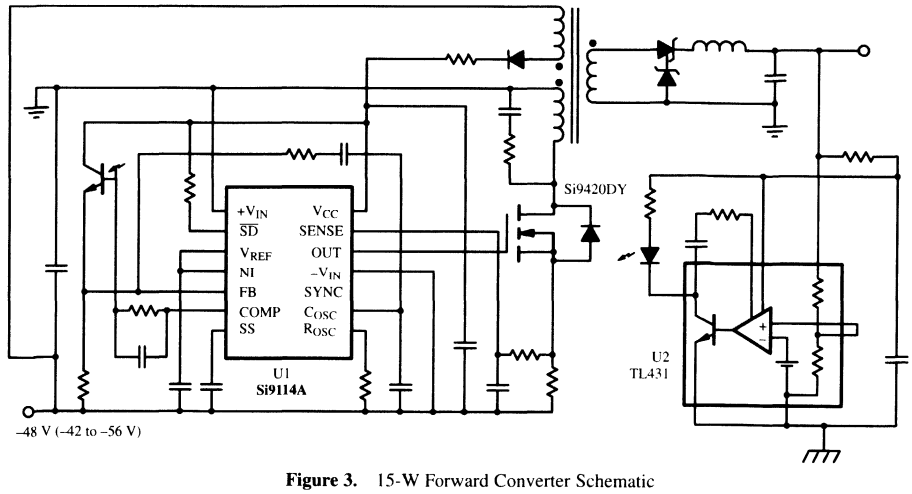


Figure 3. 15-W Forward Converter Schematic

Designing High-Frequency DC-to-DC Converters with the Si9114A Switchmode Controller

by Bijan E. Mohandes

Introduction

In 1987 Siliconix introduced the Si9100 monolithic switchmode PWM controller and established the trend for low-power, high-efficiency dc-to-dc converters. This versatile device integrated a number of useful features, including a power MOSFET, high-voltage start circuitry, and low power consumption. The new Si9114A controller pushes the limits for high-frequency power conversion by further reducing delay times and adding additional features. As a result, dc-to-dc converters can be designed for frequencies up to 1 MHz with simple PWM topologies instead of the complex resonant ones.

The Si9114A uses constant frequency current mode control. By increasing the conversion frequency, power supply designers will be able to:

- reduce the size of energy storage components
- increase reliability by using ceramic capacitors
- produce an all-surface-mount assembly solution
- lower system costs
- simplify the implementation of a distributed power architecture.

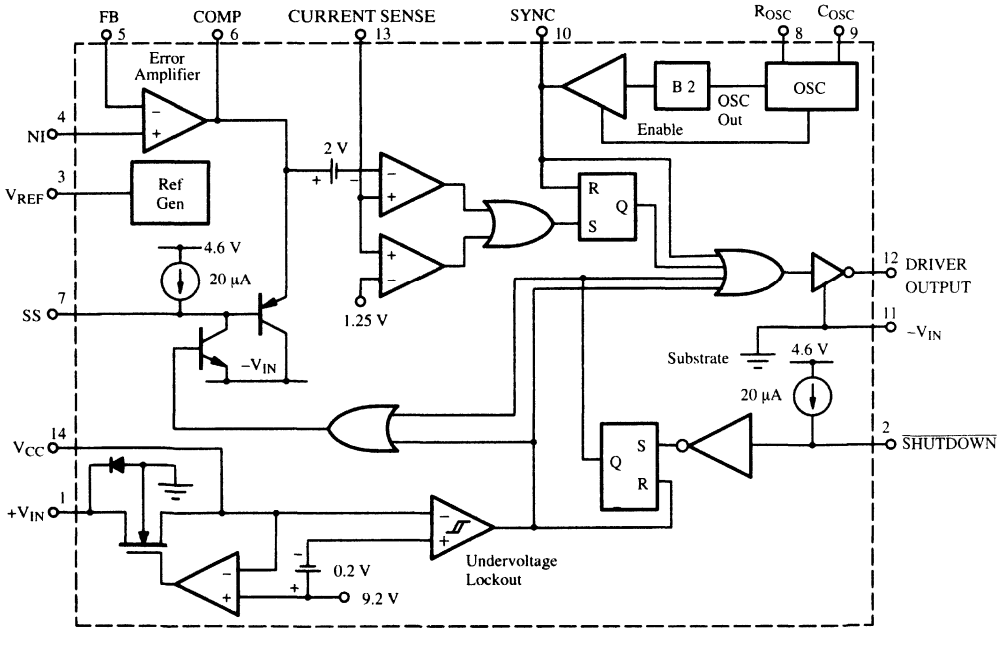


Figure 1 Si9114A Block Diagram

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Traditionally, distributed power has been regarded as costly and impractical to implement due to the high cost of local power conversion and the perceived complexity of resonant power supplies. But these decision criteria are now being changed by the availability of small-outline control ICs, LITTLE FOOT® MOSFETs, ceramic capacitors, and new magnetic components.

Functional Description of the Si9114A BiD/CMOS PWM Controller

The Si9114A controller is similar in configuration to the Si9110. It uses a traditional constant frequency current mode control, the most commonly used architecture. The duty cycle is limited to less than 50% to avoid problems with core reset.

Current mode control is presently the de-facto standard for PWM control circuits. Indeed, it is the only candidate that should be considered, given its many advantages:

- Cycle by cycle current limit protection
- Simple loop compensation, eliminating effect of output inductor
- Excellent fast transient response due to inner control loop
- Automatic input voltage feed-forward compensation

Pin 1 - High Voltage Pre-Regulator

All switchmode power supplies face a start-up problem caused by the large difference between dc bus voltage and the V_{CC} power rail for supplying the control circuit. The traditional technique has been to keep the control circuit in "sleep mode," while a small amount of energy is used to "top up" a large enough electrolytic capacitor to get the circuit started. When the circuit starts operating, a winding on the transformer is then used to power the control circuit. Disadvantages with this type of circuit include delayed start-up and large required capacitances for guaranteed operation over the full voltage range. The Si9114A overcomes these problems by using low power consumption, BiC/DMOS circuitry, and a unique high-voltage depletion mode MOSFET. (See 2)

When power is first applied, the depletion transistor is on, and current flows from the input capacitor C_{IN} into the V_{CC} capacitor C_{VCC} until V_{CC} reaches 9.2 V. The converter transformer will then supply the V_{CC} through a bias winding, which will raise V_{CC} to a level higher than 9.2 V. Ideally this will be between 11 and 13 V, thus turning off the high-voltage depletion mode MOSFET. The 9.2-V threshold has a hysteresis of 300 mV to prevent oscillations when the transition voltage is not clearly defined or when high-line supply impedance is encountered.

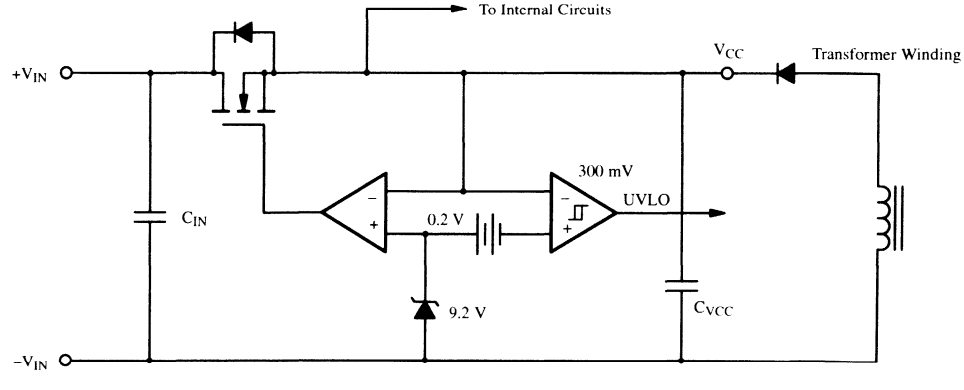


Figure 2 Start Circuit

For applications where the input dc voltage is not high, and the chip power consumption is not excessive, the feedback winding can be eliminated. In such cases, the pre-regulator circuit will behave just like a linear regulator with 9.2-V output and 10-kΩ series resistance. In this case, the parameters to be considered are the dropout voltage at lowest line condition and the power dissipation at highest voltage. The high-voltage depletion mode MOSFET contains an internal body diode, and in situations where the V_{CC} is being powered from a laboratory supply, care must be taken to avoid loading the $+V_{IN}$ rail beyond the current rating of this device. Typically, the reverse characteristics of the device will generate a voltage of 3.4 V on Pin 1 with 10-kΩ load when powering V_{CC} from a lab supply.

In some applications it is necessary to inhibit the start of a converter until a high enough voltage is present on the supply bus. This is the case for the following reasons:

- Circuitry fed from a high line impedance such as a telephone line will have difficulty starting, since the converter will behave like a negative impedance. As the dc voltage decreases, the input current increases because constant power is drawn. This causes severe oscillations, and can in some instances have a destructive effect on the converter. [4]
- During start-up, the Si9114A will begin operation as soon as the UVLO threshold is reached. Since the converter is designed to operate over a much higher range—for example, from 36 to 72 V—then between 10 and 36 V input the output voltage will be out of regulation and undefined. In some cases, digital circuitry will not accept this mode of operation, and system faults will be encountered without a RESET watchdog circuit.

To overcome these problems, a Zener diode of suitable value V_Z can be placed in series with the $+V_{in}$ pin, preventing start-up until $V_Z + 9.2$ V is reached.

Pin 2: Shutdown

The shutdown pin is configured to allow fast latched termination of the output pulse. The delay from shutdown to output is typically 300 ns. This delay is short enough to allow this pin to be used for over-voltage applications where fast orderly shutdown is desirable: for example, when control of the feedback loop is lost.

Using an opto-coupler and a TL431, interface is easy. (See 3) Once latched, the shutdown can only be reset from the UVLO circuit by re-cycling the power. In the event of an over-voltage, the latch can be reset by momentarily pulling the V_{CC} to a value lower than the UVLO threshold.

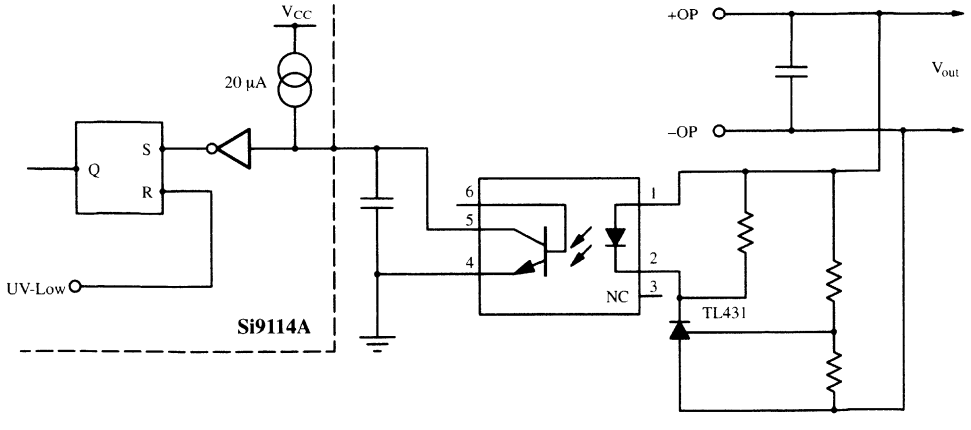


Figure 3 Shutdown

This approach will generally be acceptable, since the feedback winding will not be supplying power, and the only power maintaining the latch will be supplied by the depletion start transistor. Note, however, that this action will still be subject to the power dissipation limits of the Si9114A package and should ideally be applied as a short fast pulse.

Pin 3: Reference

The reference voltage is a fully buffered band gap type which can source 5 mA over the specified voltage tolerance range. The reference should be well de-coupled to prevent instability and jitter. A ceramic 100 nF or small tantalum is recommended, depending on the de-coupling present on the supply pins.

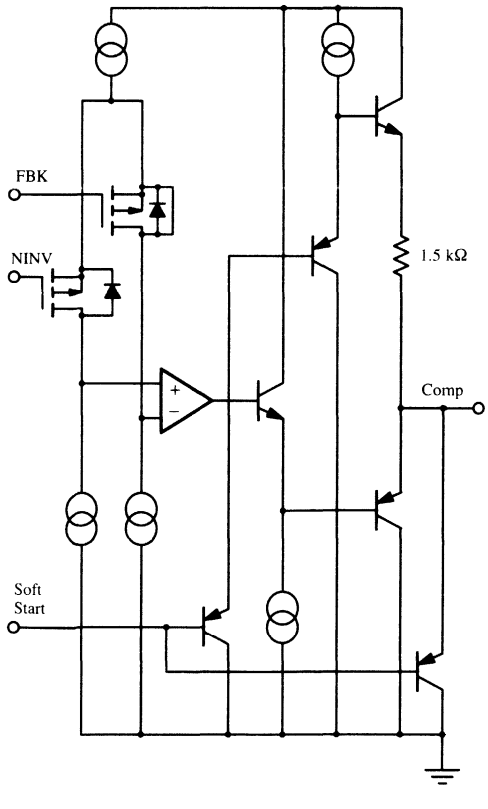


Figure 4 Operational Amplifier

Pins 4, 5 and 6: Error Amplifier

The error amplifier consists of a PMOS input folded cascade gain stage followed by a class AB unity gain amplifier.

Typical open loop voltage gain is 77 dB, and unity gain bandwidth is typically 2.7 MHz. The soft-start circuit (see Pin 7 description) forces the output to within 0.7 V above ground, and additional clamp diodes limit the positive output excursion to within $2xV_{BE}$ above V_{REF}. Operation at high frequency allows high closed loop bandwidths and permits excellent transient response to both input and output changes. Under normal operation, a small 100 pF bypass capacitor is recommended from N_{INV} to Comp to increase high-frequency noise rejection. This should be calculated, however, in conjunction with the loop dynamics.

Pin 7: Soft-Start

The soft-start circuit is designed to help dc-to-dc converters start in an orderly manner and reduce component stress. The output of the error amplifier is clamped by a PNP transistor.

The external capacitor C_{SS} is supplied by a 20-µA current source and will charge linearly to 4.6 V. In the event of an under-voltage lockout (or during start-up), this capacitor is held low.

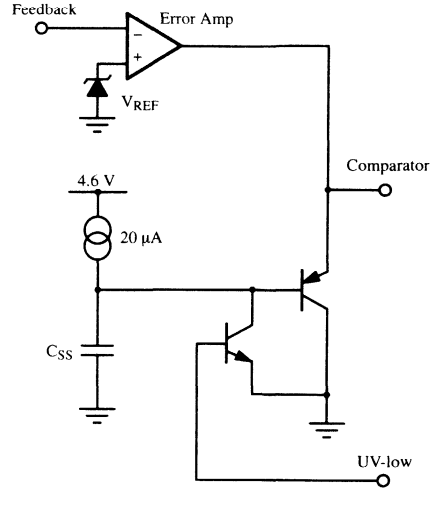


Figure 5 Soft-Start

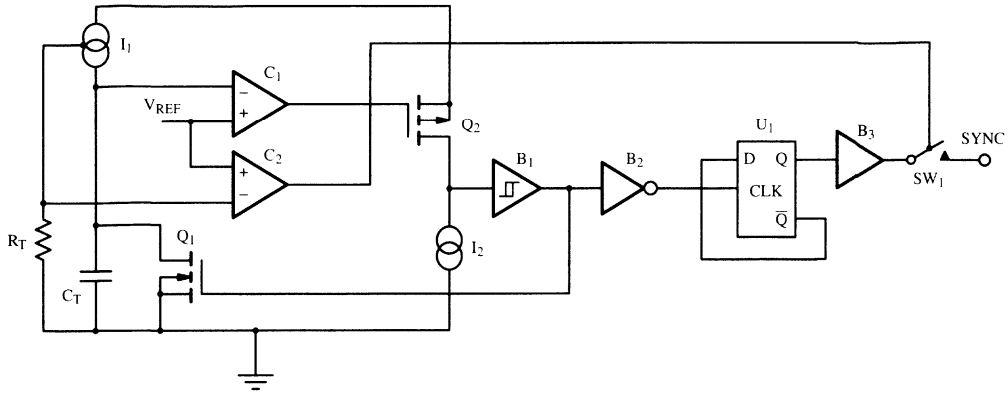


Figure 6 Oscillator

Soft-start is a very important feature and has many beneficial effects, especially in applications connecting to telecom lines where source impedances are high. In such cases, there is an initial start-up current caused by the input capacitor, followed by a secondary peak caused by the converter running at maximum duty cycle while trying to reach regulation. Where large output capacitances and peak loads are encountered, oscillations may occur. These can be prevented with the use of long soft-start times. The soft-start pin can also be used as a non-latching shutdown pin by connecting it to $-V_{IN}$. This approach allows a shutdown with soft re-start.

Pins 8 and 9 – Oscillator

The oscillator circuit uses external timing components R_T and C_T. An internal divide-by-two prevents pulses with greater than 50% duty cycle, so that core saturation can be avoided. When the R_T terminal is connected to V_{CC}, comparator C_2 disconnects the oscillator output from the SYNC terminal using SW_1, and allows an external oscillator circuit to take control of the current mode comparator circuit.

The current programmed by R_T defines the charging current of C_T and the on and off times with the following design equations:

$$T_{ON} = \frac{1.025 \times R_T \times C_T}{8} \quad (1)$$

$$T_{OFF} = 5 \times R_{ql} \times C_T \quad \text{where } R_{ql} = 25\ \Omega \quad (2)$$

$$F_{OSC} = \frac{1}{2} \times \frac{1}{(T_{ON} + T_{OFF})} \quad (3)$$

Actual values taken from a prototype board have been plotted (Figure 7), and are a close match (except for 47 pF, where stray parasitics have more significant effect).

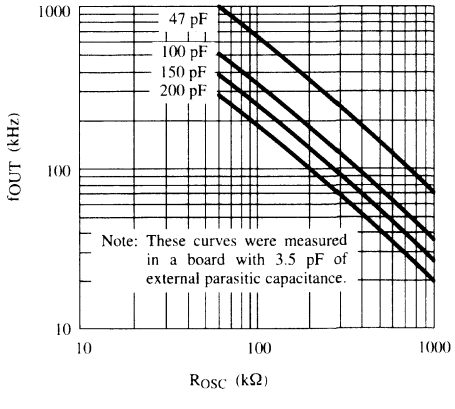
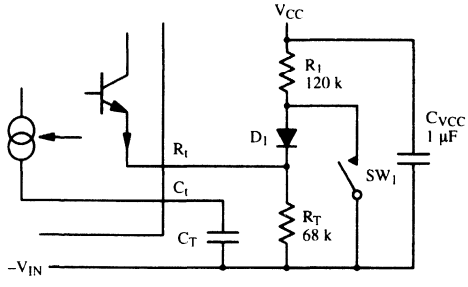


Figure 7 Oscillator Frequency Selection



SW_I Closed = Frequency High
SW_I Open = Frequency Low

Figure 8 Frequency Shifting Using R_I Current Change

In certain circumstances, such as current limiting, it may be desirable to change the frequency of the converter for a period of time to overcome current tails (see Figure 16 for further explanation). With the Si9114A, this is easily done by adding or subtracting some current into the R_T terminal:

- The charging current in C_T is set by 8 × R_T.
- The voltage at the R_T terminal is 4 V, as supplied by an internal emitter follower from the reference.

The frequency can be changed easily by supplying some of the current into R_T from the V_{CC} rail, thus "starving" the internal current source, and slowing the frequency down.

The current in R_T is set by V = IR where V = 4 V and R = R_T. Using a diode, and some type of switch, the frequency can be easily changed: when SW_I is closed, D_I is reverse biased, and has no effect on R_T. When SW_I is open, current flows through R_I and D_I into R_T and removes some of the current supplied by the internal emitter follower.

Pin 10 - Synchronization

The *SYNC* input allows operation from a master clock as the connection is made after the divide-by-two. As a result, synchronization in both frequency and phase is possible. This unique feature is important to systems designers who use multiple converters, where noise caused by an unsynchronized "beating" effect is present and causes difficult EMI/EMC problems. If an external clock is used, duty cycles of >50% are possible due to the position of the *SYNC* pin , after the divide-by-two. Where >50% conduction is used, core reset must be allowed, in order to prevent core saturation. Synchronization is in master/slave mode, with one device (the "master") setting the switching frequency and others (the "slaves") with disabled oscillators locked to it. Alternatively, all devices can be clocked using a master oscillator.

During slave mode, the unused C_T pin should be connected to ground, and the R_T to V_{CC}.

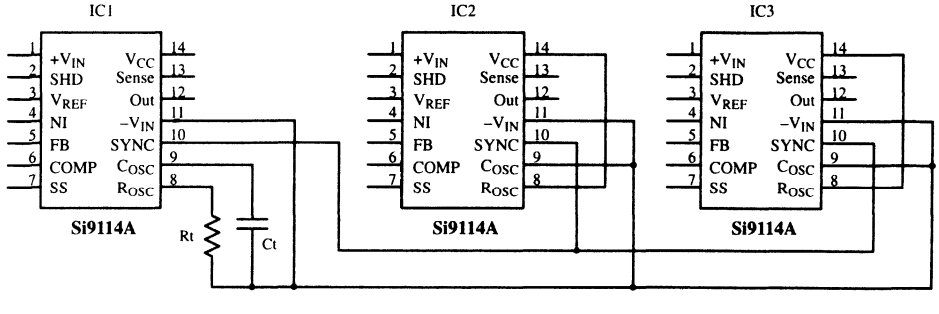


Figure 9 Oscillator Synchronization

Pin 11 & Pin 14 $-V_{IN}$ & V_{DD}

These pins are used for powering the Si9114A and should consequently be well de-coupled. In selecting the right de-coupling, the MOSFET gate drive requirements should be considered, as the de-coupling capacitor will also have to supply the required peak current. Generally speaking, the best combination would be a 1- to 10-µF electrolytic for bulk energy and a 100-nF ceramic for high-frequency bypass. The V_{CC} rail should be carefully observed at the switch on and off occurrences using ac de-coupling, and the peak voltage spikes should be measured. These should be less than 200 mV. Excessive noise on the V_{CC} will appear on other pins and may cause instability or jitter on the control waveforms.

Pin 12 - Output Driver

The output driver uses complementary n- and p-channel output stages, with break-before-make capability, preventing shoot-through conduction. The output is typically capable of sourcing 400 mA and sinking 700 mA. When driving power MOSFETs, remember that the relevant parameter for sizing the drive requirements is the total gate charge for the applied voltage, not the commonly used input capacitance, C_{ISS}. When driving a MOSFET in common source mode, the Miller effect will significantly affect the drive waveform applied to the gate: in particular, when the driving source impedance is high enough (Figure 10).

As the voltage is applied to the gate, the previously charged C_{gd} will need to discharge, and will thus oppose the application of any voltage to V_{gs}. Many designers commonly overestimate the drive requirements of the MOSFET and cause excessive noise in the converter by overdriving the MOSFET. To prevent this, designs typically require snubbers or other additional noise attenuation devices. The voltage that will be applied to the drain just prior to driving of the gate will need to be considered. In practice, most manufacturers are unable to publish this data for all voltages, so designers should use the curve nearest to the actual voltage applied.

The Si9420DY LITTLE FOOT MOSFET is designed specifically for converters in the 5- to 25-W power range. It has a 200-V V_{DS} rating with 1-Ω $r_{DS(on)}$. Using the Gate charge curve, for a gate drive of 12 V from the Si9114A, the total gate charge for 100-V V_{DS} will be 10 nC. From Q = i x t, it is easy to deduce that with 400 mA gate drive, a time of 50 ns will be obtained—which is more than adequate for this size MOSFET. To supply 400 mA, the gate drive circuit resistor will need to be 12 V/400 mA = 30 Ω (Figure 11).

Pin 13 - Current Sense

The current sense comparator performs the current mode control function by comparing the output of the error amplifier (V_C) with the current in the output inductor.

It is impractical to measure the output inductor current, but the rising slope of the current can supply all the necessary information if sampled in the MOSFET as a scaled equivalent.

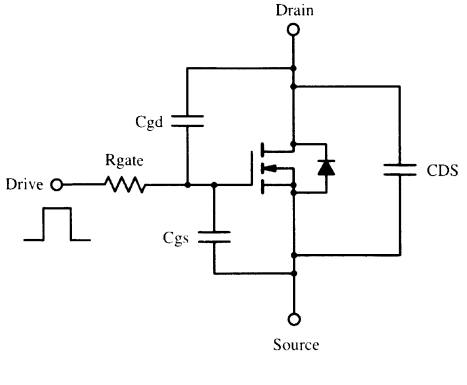


Figure 10

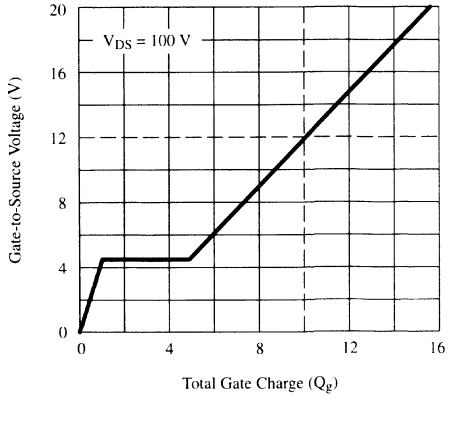


Figure 11 Si9420DY Gate Charge

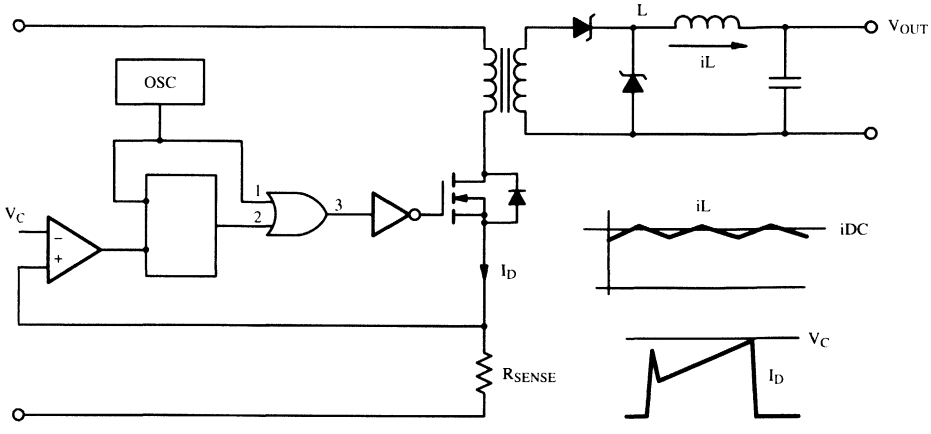


Figure 12. Constant Frequency Current Mode Control

Certain precautions are necessary, however, due to data distortion, noise, and the rarity of ideal operating conditions.

Sensed current waveforms often have leading-edge spikes or noise caused by reverse recovery of rectifiers, equivalent capacitive loading on the secondary, and inductive circuit effects. Inductive sense resistors must not be used, as they cause large damaging spikes and distort the sensed waveforms. These spikes can confuse the PWM comparator into believing that an overload condition is present. In addition, the Si9114A uses a single pin ($-V_{in}$) for all the return current requirements, including the output driver. As a result, the current pulse from the gate charge transfer into the MOSFET will appear on the sense pin and be filtered out.

Waveform A has an ideal textbook appearance, but is in fact rarely encountered. Waveforms B and C are typical yet close to the threshold limit, and thus could lead to instability. The addition of a simple RC network on the sensed waveform suppresses this leading-edge spike. The low pass filter should be selected so that only the leading-edge spike is suppressed and the overall waveform is not distorted. The waveform must contain a clean rising slope for the error amplifier to intersect. If the RC time constant is too long, then the waveform will be distorted and lead to falling-edge jitter on the turn-off edge.

Slope compensation can also be used to eliminate noise or jitter. A sample of the oscillator voltage is superimposed on the error amplifier to produce a clean crossing of the thresholds and to avoid any hunting.

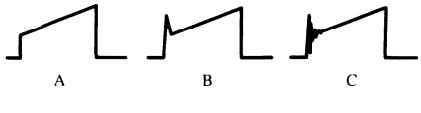


Figure 13 Current Waveforms

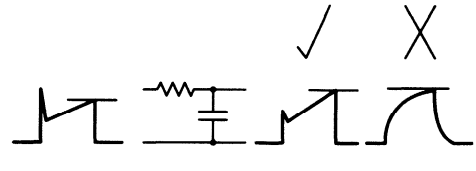


Figure 14 Current Sense Filtering Network

The Si9114A has built-in leading-edge blanking/ suppression to eliminate some of the effects of these spikes. The two comparators comparators used to operate the circuit have different delay times as follows:

- The current mode comparator needs more noise immunity, and therefore has a deliberately slower delay time to block out noise and spikes which are present on the leading edge. Typical delay times should be around 100 ns.
- The peak current limiting comparator has the fastest response time, since it is used only to protect the circuit in the event of an overload. The delay times for this comparator should be around 70 ns.

High-Frequency Design Requirements

When designing converters for high switching frequency, a certain discipline is required to determine the right choice of components. This process should be an iterative choice and the board layout should be properly planned before CAD layout is undertaken.

Layout Considerations

The main current loop flows from the input capacitor—through the transformer, MOSFET, and sense resistor—and returns to the capacitor. This current will have high rates of change and associated fast voltage and current edges. It is essential to avoid the injection of noise into the other circuitry.

To prevent this result, a "fishbone" type arrangement is recommended (Figure 15). Designers are encouraged to separate different grounds with "imaginary" dummy resistors. These can be removed at a later stage. Main current loops must be designed to be as short as possible: from C_{IN} to the transformer, through the MOSFET and Sense resistor, and back into C_{IN}. It is obvious that signals switching 50 V or 1 A in 25 ns should not be mixed with signals that are controlling a closed-loop, high-gain feedback system which is capable of regulating the output voltage to less than 1 mV.

Choosing the Switching Frequency

When selecting the switching frequency, it is usually best to choose the lowest possible frequency that the design solution will accept. In PWM control topologies, the maximum switching frequency will be strongly governed by short circuit behavior. When a short circuit is applied to the output, the control circuit is required to reduce the duty cycle to the smallest possible value to maintain constant current operation (Figure 16).

Ideally, the converter should deliver 105% of the output current within regulation and no more than 115% under short circuit. At 500 kHz, the period of conversion is 2 µs and the maximum on time is 1 µs.

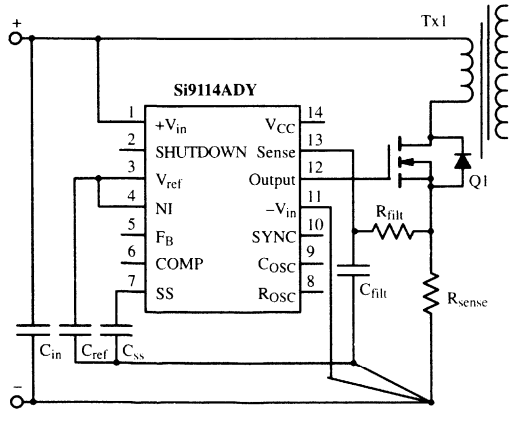


Figure 15

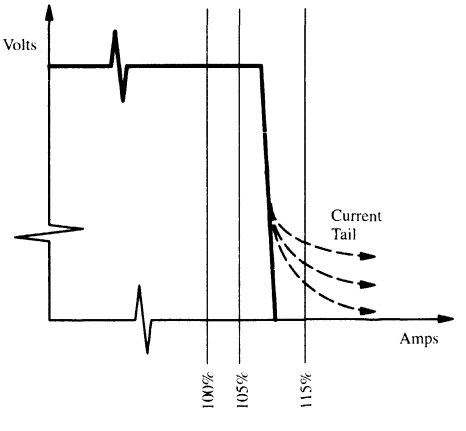


Figure 16

High minimum duty ratios will result in current tails and require rectifier oversizing to avoid destructive currents under overload conditions.

The Si9114A has a sync-to-output delay of less than 70 ns, so the minimum duty cycle for operation at 500 kHz would be 70 ns/1 µs = 7%. This minimum should be considered when the short circuit current is determined. Designers should note that a shunt placed across the output of the converter is probably not a realistic load in the event of a failure, and the real circuit impedance will probably be substantially lower. In such circumstances, it may be necessary to shift the frequency of the converter to a lower value during overload. Frequency shifting can be accomplished by altering the steady state values of the oscillator programming components (see oscillator section, Figure 8).

Short Circuit Behavior

Short circuit behavior is different for both common topologies, and must be paid special attention.

- In flyback converters, all windings appear in "parallel" with each other. When one winding is shorted, all other flyback windings are also shorted though it. In multiple output converters, therefore, any single winding without a separate secondary current-limiting protection will "drag down" all the other windings. As a result, if a bias winding is used to power the control circuit, it will stop delivering power. When this occurs, the Si9114A depletion device will turn on and regulate the supply rail to 9.2 V, as in its normal starting mode. In this event, designers should calculate the worst-case power dissipation caused by the voltage drop across the depletion transistor at the highest applied voltage across it and with the current flowing through it.

- In forward converters, traditionally the bias winding is also taken in forward conduction mode, but without any series inductance. In the event of a short circuit, the pulse width is reduced to minimum, but it is sufficient to supply enough power to the control circuit. This is an advantage, and avoids the problems encountered with flyback converters. Power may also be taken in flyback mode, however, when the duty cycle is low. There will be very little flyback voltage present, since the applied volt/microseconds is low and the core need not, therefore, fly back very far to reset.

Choosing the Topology

The choice of topology is usually based on the designer's previous experience. The two best candidates for the Si9114A are the forward and flyback types, although other types, such as Cuk, are also possible.

In general, forward converters are best for higher-power applications, and flyback converters are best for lower-power applications. Both topologies have their merits, and the designer will have to select the one most suited to his or her own application. See appendices A and B for brief descriptions of topologies and magnetic design equations.

Selecting the Semiconductors

For power switching, the recommended device is the Si9420DY. The Si9420DY is a 200-V, 1-Ω MOSFET housed in an industry-standard SO-8 package. Since the die is mounted on a copper header, cooling can be accomplished using the PCB area directly below the Drain pins. The combined performance of the Si9420DY's features makes it the best low-profile device available on the market. It is suitable for designing power supplies ranging from 10 to 25 W. Other such single and dual LITTLE FOOT devices are available in both n- and p-channel versions with voltages starting from 12 V.

Rectification for low-voltage outputs (< 5 V) is accomplished using Schottky diodes. In this case, the rectifier selected exhibited forward voltage drops of 0.4 V at 4 A. A 5-V output will require a rectifier with a 40-V reverse voltage rating. Where lower voltages, such as 3 V, are required, devices with lower reverse blocking should be used, since these will have lower forward voltage drops. Designers should avoid using an oversized Schottky diode, since all such devices have parasitic capacitances that need to be charged and discharged to the applied voltages. Driving and commutating oversize devices will not necessarily yield better efficiency, especially at higher frequencies.

Rectification for voltages above 12 V is generally accomplished using fast or ultra-fast rectifiers. Look for devices that have recovery times below 50 ns. An excellent example is Telefunken Semiconductors' BYG22B rated for 100 V and 2 A with 25 ns recovery, and Forward voltage of 0.7 V for 0.5 A current. This device is available in a DO-214 surface-mount package.

Opto-isolators are now available in SO-8 packages with 3000 Vrms isolation rating. These are by far the least expensive and simplest isolated feedback devices now available. Their reliability, once considered questionable, has been greatly improved, and manufacturers now have quality data demonstrating their suitability under the correct operating conditions. A typical device would be the Telefunken Semiconductors' TCMT1020.

Choosing Ferrite Materials

Ferrites suitable for operation at high frequencies have recently been introduced to the market. Two such offerings are the Philips 3F3 and 3F4, designed for operation up to 500 kHz and 2 MHz respectively. Many different geometries and good supporting data are now available. Appropriate choices for low-profile and surface-mount capability include devices in the EFD series, which have been extended down to 10 mm. It is better to choose core geometries with shallow and wide bobbins, since these permit good coupling from winding to winding when using high frequencies.

Choosing Ceramic Capacitors

High-frequency operation allows the use of very low-value capacitances not generally associated with switchmode power supply output stages. As substantially lower energy storage is required, multilayer ceramic capacitors can be used, and suppliers have made good advances in quality and manufacturing to supply low-cost, high-performance designs. In the sub-25-µF area, a number of good dielectric devices are now available, such as X7R, Z5U, and Y5T.

From manufacturers' data sheets, the following observations were made:

- Z5U has the lowest cost, highest unit capacity, and worst dynamic variations
- X7R has the highest cost, lowest unit capacity, and best dynamic stability
- Y5T has an average of each of the above.

The recently introduced Marcon TCCR series uses the Y5T dielectric, which offers good all-around volumetric, cost, and high-frequency impedance performance, and is available in a surface-mount package with values such as 10 µF at 25 V and 3.3 µF at 100 V. For input and output energy storage, two of each of these devices were selected with the following considerations:

- Realistic market price.
- Voltage variation with applied dc voltage and temperature. Most ceramic capacitors suffer from a drop of capacitance with applied voltage and with temperature. The device needs to be selected so that at the extremes of operation the minimum energy storage is present.

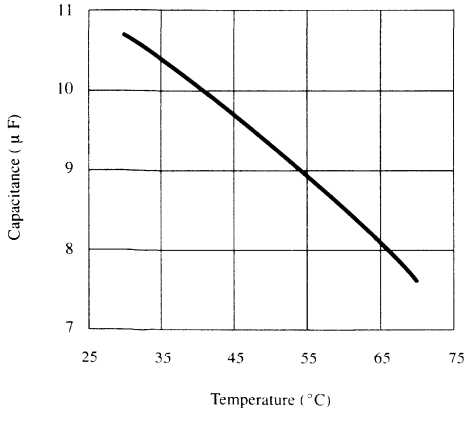


Figure 17. Marcon 10 µF 25 V, Capacitance Versus Temperature

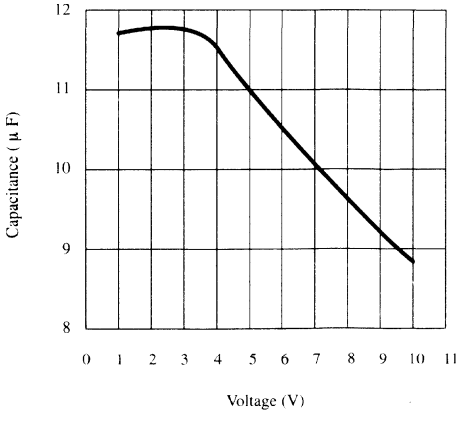


Figure 18 Marcon 10 µF 25 V, Capacitance Change with Voltage

- Equivalent Series Resistance (ESR). ESR will determine the output ripple voltage, and the heating of the device. This should be selected on the basis of the value of output choke, insofar as its design sets the ripple current present in the output capacitor.

The following data was obtained from commercially obtained samples:

At 70°C, the 10-µF device has dropped to 75% of its nominal value. With 5 V applied, the same device has retained 110% of its nominal value.

Care should be taken in selecting these devices to consider worst case requirements and minimum/ maximum operating conditions.

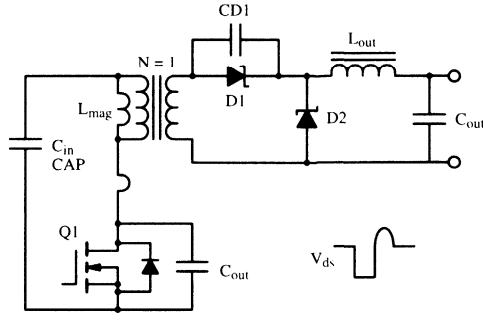


Figure 19 Resonant Reset Forward Converter

Design Example: A 15-W, 500-kHz, 48-V/5-V DC-to-DC Converter

Resonant Reset Forward Converter

Most forward converters are designed using a clamp circuit. While at low frequencies this technique may be acceptable, at high frequencies it becomes unnecessary: the parasitic elements of the circuit will reset the transformer flux automatically, provided a few precautions are taken.

It has been shown that [1] the resonant reset concept is dominated by the parasitic capacitance of the MOSFET and the magnetizing inductance of the transformer. Yet the capacitance of the output diode should also be considered. The correct equivalent circuit of the converter the approximates to Figure 19.

During the off time, D_2 is conducting and C_{D1} appears connected across the primary of the transformer, in parallel with L_{MAG}. The leakage inductance has a small and insignificant effect on the waveform—as the primary current has ceased flowing—and the only remaining current is the current that is charging C_{OUT}.

In effect, the magnetizing inductance of the transformer forms a parallel tuned circuit across the transformer and resonates at a frequency determined by the parasitic elements. The reset period needs to be short enough to allow full reset of the core, before the next switching interval occurs. This will be governed by the selection of the MOSFET and the Schottky diode.

Component Selection

The following information is supplied in order to help designer select correct components for use with the Si9114A. Siliconix does not necessarily recommend or approve these components for specific applications. Designers should contact manufacturers directly to obtain correct and current data sheets.

Capacitor Selection

As stated previously, ceramic capacitors are a good choice when operating at high frequency, due to the extremely low ESR, and high reliability, and long operating lifetimes.

In the design example, the required size of capacitors was defined as follows:

Input capacitor:

A 15-W output converter with 85% efficiency will require 15/0·85 = 17.65 W of input power. Assuming that operation at nominal conditions is 48 V, with duty cycle of δ=0.376 (measured), the switching current will be governed by the size of the output inductor (Figure 20).

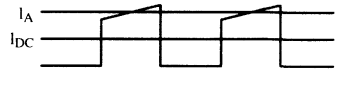


Figure 20

The average input current will be determined by:

$$I_{DC} = \frac{P_{in}}{V_{in}} = \frac{17.65}{48} = 0.358 \text{ A}$$

$$I_A = \frac{P_{in}}{V_{in} \times \delta} = \frac{17.65}{48 \times 0.376} = 0.98 \text{ A}$$

From this equation the RMS value can also be calculated to be approximately 0.475 A.

The Marcon TCCR70E2A335 3.3-µF, 100-Vdc capacitor has an ESR rating of 20 mΩ at 500 kHz. This type will therefore dissipate $P = 0.475^2 \times 0.020 = 4.5$ mW due to the switching current. The ripple produced across this device will be governed by the discharging current of the capacitor less the input dc voltage in accordance with:

$$Q = i \times t = C \times V$$

$$\therefore V_{ripple} = \frac{I_C \times t}{C} \text{ where } t = t_{sw} \times \delta \text{ and } I_C = I_A - I_{DC}$$

$$\therefore V_{ripple} = \frac{0.612 \text{ A} \times 2 \text{ µs} \times 0.376}{3.3 \text{ µF}} = 0.14 \text{ V}$$

140 mV of ripple is probably acceptable as a first stage of filtering. If lower ripple is required at the input, then a two stage filter will yield better results.

Output capacitor:

$$C_{out} = \frac{\Delta I_{out}}{8 f \Delta V_{out}} \text{ where } \Delta I_{out} = 0.1 \times I_{out}$$

ΔV_{out} = maximum output ripple voltage
f = operating frequency

$$C_{out} = \frac{0.3 \text{ A}}{8 \times 500 \text{ kHz} \times 50 \text{ mV}} = 1.5 \text{ µF}$$

The required ESR for obtaining 50 mV of ripple would be defined by:

$$ESR_{max} = \frac{\Delta V_{out}}{\Delta I_{out}}$$

$$ESR_{max} = \frac{50 \text{ mV}}{0.3 \text{ A}} = 167 \text{ mΩ}$$

In practice, it is impossible to precisely match the value of a capacitor with the required ESR, and the values of the capacitors must often be selected to cover all operating conditions including voltage and temperature.

The above equations and calculations are meant to help the designer select the approximate size of the components required, with the final selection based on practical values that meet the minimum required. In designs operating below 500 kHz, the choice of the capacitor is dictated by the ESR, and the best high-frequency electrolytics often require large-size and micro-farad values to meet these requirements. When operating at 500 kHz, the choice becomes more based on the practical value closest to the size and voltage rating required. For example, with electrolytics, in order to guarantee the ESR over temperature or age, it might have been necessary to use a radial 1000-µF, 6.3-V Aluminum Electrolytic in a 10x16 mm case (1257 mm2) to get an ESR value below 100 mΩ. It would also be necessary to check the ESR with frequency at 500 kHz, as this data is seldom offered for electrolytics. By comparison, the Marcon TCCR70E1E106 10-µF, 25-Vdc is available in 7.5 x 6.3 x 2.75 (130 mm2) and has an ESR of less than 15 mΩ at 500 kHz. This will be ideal for low output ripple an noise. Recently introduced organic semiconductor electrolytics offer substantial improvements and could also be considered. In this example, it was decided to use 2 x 10-µF capacitors in order to obtain low output ripple.

Output Inductor Design

The output inductor limits the rate at which the current flows into the output capacitor when the voltage is applied from the primary through the transformer (Figure 21).

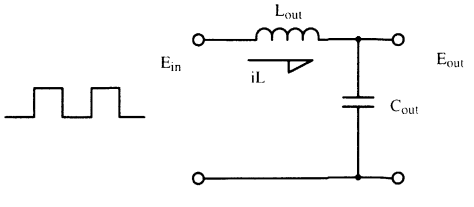


Figure 21

From simple circuit theory, the voltage applied across an inductor is:

$$V_L = L\frac{di}{dt} \qquad \text{where} \qquad V_L = E_{in}-E_{out}$$

$$\text{and } di = \Delta I_L \text{ then } L = \frac{(E_{in}-E_{out})x\Delta t}{\Delta I_L}$$

In forward converters, at maximum duty cycle, Ein = 2xEout, and:

$$t_{off} = \frac{1}{2 \times F_{sw}}$$

In this case, substituting gives:

$$t_{off} = 1\mu S \text{ and } L = \frac{E_{out} \times t_{off}}{\Delta I_L}$$

Therefore

$$L = \frac{5\ V \times 1\ \mu S}{0.3\ A} = 16.7\ \mu H$$

In practice, an inductor between 5 and 10 µH would be an acceptable choice, allowing for manufacturing tolerances and variations.

The core selected is the EF12.6, which is identical to the core selected for the transformer design. The EF12.6 is a cheap, low-profile design available from many suppliers in all parts of the world. A surface-mounted version of this bobbin was selected for a design that could be entirely machine wound and terminated. This implies that larger wire sizes are not possible, due to automated winding restrictions.

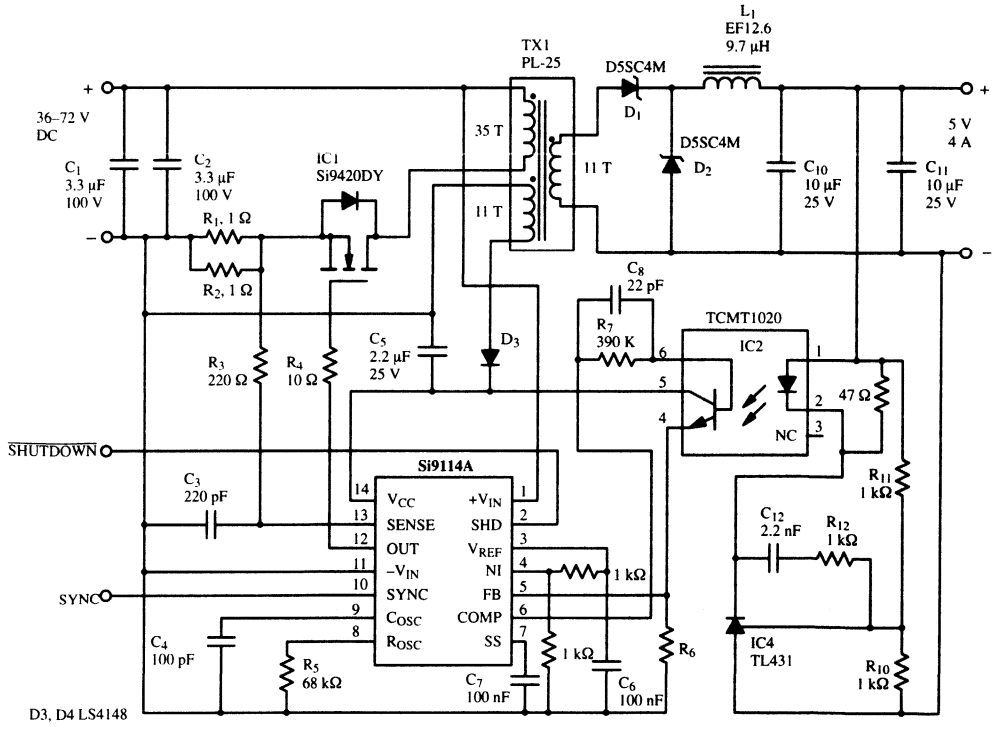


Figure 22 DC-to-DC Converter Block Diagram

Since this choke must carry the full output current, the minimum number of turns required on this core is given by:

$$N_{min} = \frac{L_{choke} \times I_{Choke}}{B_{max} \times A_{min}}$$

where B_{max} is the maximum flux density used, and A_{min} is the minimum core area. In this case B_{max} = 200 mT and A_{min} = 13 mm^2. Substituting in this equation yields:

$$N_{min} = \frac{8\ \mu H \times 3\ A}{200\ mT \times 13\ mm^2} = 9.2\ T$$

In this case it was decided to wind 3 layers of 12 turns of 0.315 mm in one layer each across the bobbin. This allowed the best fill factor of the bobbin, maximizing copper area.

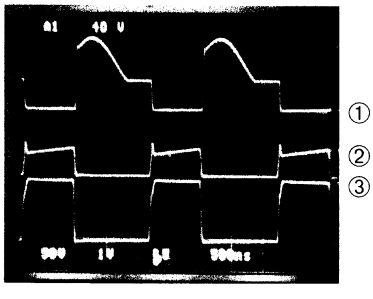
The result yields a choke having a dc resistance of 22 mΩ and therefore a dc copper loss of $P = I^2R_{DC} = 9 \times 0.022$ = 200 mW with 3 A dc. Using a core set with an A_L value of 45, a transformer of $L = N_{min}^2 \times A_L = 12^2 \times 45 \times 10^{-9}$ = 6.48μH was calculated. Measured value was 9.73 μH: slightly higher, but acceptable.

Transformer Design

See appendix A for a design using these specifications.

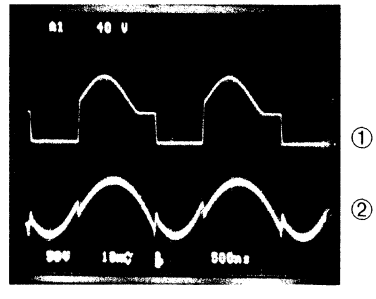
Performance Results

The switching waveforms in Figure 23 show that the resonant reset is limiting the peak voltage to 120 V, well below the maximum rating of 200 V. Note the leading edge spike caused mainly by the peak gate current.



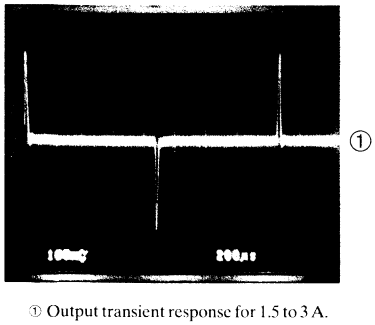
① V_{DS} of MOSFET 50 V/div
② Voltage across sense resistor 1 V/div
③ Voltage across gate 5 V/div

Figure 23 Time Base 500 ns/div.



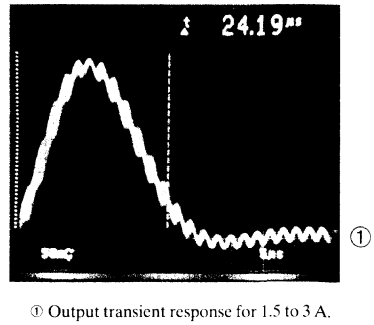
① V_{DS} of MOSFET 50 V/div
② Output ripple 10 mV/div

Figure 24 Time Base 500 ns/div.



① Output transient response for 1.5 to 3 A.

Figure 25 Time Base 200 μs/div.



① Output transient response for 1.5 to 3 A.

Figure 26 Time Base 5 μs/div.

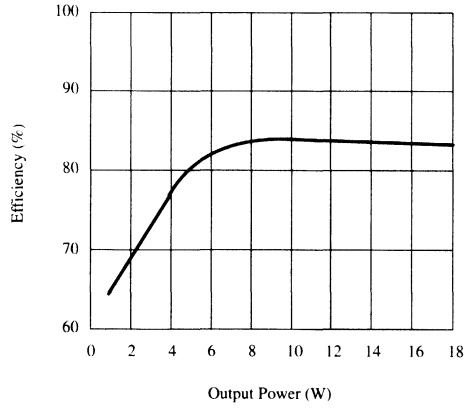


Figure 27 Si9114A 15-W, 500-kHz Converter Efficiency

In Figure 24, the low output ripple (<20 mV) is obtained with two 10-µF capacitors.[1] In Figure 26, note the excellent recovery time of <25 µs to within 1% of output for a 50% load step with total excursion of <300 mV. The efficiency of the converter is measured in Figure 27.

Benefits of Using Si9114A

Low power consumption:

at 500 kHz, the Si9114A consumes only 8 mA from the 12-V supply. This amounts to a total of 96 mW or 5.6% of the losses. It is important to remember that this figure represents both the power MOSFET losses as well as the control circuit. The control circuit was measured to consume only 3.2 mA or 2% of the total losses. In comparison, typical bipolar circuits would consume 35 mA, or 21% of the losses.

Short delay times:

with typical delay time approaching 65 ns, short circuit current can be lowered, and operation at higher frequencies is possible.

Integrated high-voltage start circuit:

the depletion transistor circuit allows fast turn-on and eliminates the need for extra components. At lower frequencies and power levels, it is possible to omit the bias winding completely, since circuit consumption is low, and the depletion circuit behaves as a linear regulator.

Synchronization in phase and frequency:

is a necessary benefit for distributed power systems where multiple converters are operated.

Conclusions

Operation at 500 kHz is possible using BiC/DMOS PWM control circuits. Significant power savings are possible, yielding high efficiencies and lower parts count due to the integrated high-voltage start circuitry. Operation at high frequencies allows the use of small, efficient, low-profile energy storage components, with higher reliability and calculated MTBFs. Surface mounted power MOSFETs are easily assembled using conventional assembly techniques.

References

1/ Murakami, Noaki and Yamasaki, Mikio. "Analysis of a Resonant Rest Condition for a Single Ended Forward Converter." *PESC88 Record* (April 1988) CH 2523-9/88/0000-1018 $1.00 ©1988 IEEE.

2/ Chryssis, George C. *High Frequency Switching Power Supplies: Theory and Design.* 2nd. ed. New York: McGraw Hill.

3/ Blanc, James. "Designing DC/DC converters with the Si9110 Switched Controller." AN-88-3. Siliconix Power Products Data Book, 1993.

4/ Blanc, James. "Efficient ISDN Power Converters Using the Si9100." AN87-2. Siliconix Power Products Data Book, 1993.

[1] The strange shape of the ripple needs to be further analyzed but could be explained as follows:

- The step voltage that appears at the same time as the voltage switching edges is caused entirely by the ESR, as it is the only possible cause for a rapid step voltage across a capacitor. In this case, the measured value is on the order of 8 mV, thus predicting an ESR value of 6/0.3 = 20 mΩ for both devices. This is slightly higher than predicted, but of the same order of magnitude.
- The sinusoidal waveform must be caused by the equivalent capacitance that appears across the inductor, causing a capacitive coupling directly into the output.

Appendix A

Forward Converter Transformer Design

The forward converter transformer is operated as a voltage transformer. An ac source applies voltage across the primary, which is then transformed (up or down) by the turns ratio. For correct operation, the transformer must be correctly sized (in order to avoid core saturation) and large enough to accept the number of turns required. Since these two requirements may often compete with one another, compromise may be necessary to complete a design.

In operation, the transformer is driven through the magnetic B/H loop. In a forward converter, the core is only driven in quadrant 1. Care must be taken not to saturate it, since only a "minor loop" is used. The core is driven in the +H direction, and when the MOSFET turns off, the core is allowed to "float back" to the H = 0 position. As there is no negative drive, the core cannot be driven into quadrant 3 (as in the case of a push-pull converter), and so the core always returns to the B_{REM} (remnant) position.

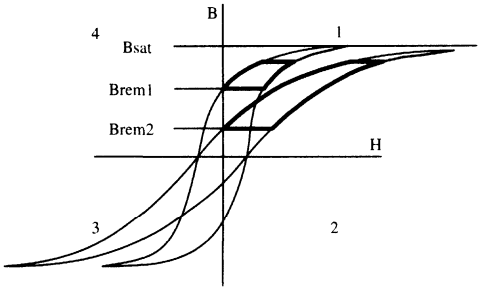


Figure 28

In some cases, a small air gap is placed in the core, which causes the B/H curve to be skewed out. The remnant position can thus be lowered from the Brem1 to the Brem2 position, allowing a larger area of operation. In all joined cores (such as RM or EE), this small gap actually exists in the form of the interface between the two cores and causes the BH curve to skew over. In high-frequency applications, this gap has a significant beneficial effect on the operation of the transformer. The number of turns is already low, and the gap prevents core saturation.

Other converters (such as half-bridge and push-pull) use all four quadrants and make better use of the whole core. These, however, require additional power switching devices and windings and are therefore not used. At high frequencies, the core losses of ferrite materials are high, so the used flux must be reduced. once this is done, the problem becomes insignificant, very small core excursions are used.

In selecting the core type and size, the transformer losses need to be divided more or less evenly between core and copper losses. Most manufacturers will now supply formulas extracted from core loss tables that allow precise core loss calculations to be made. It is important to remember that most ferrite manufacturers use peak-to-peak flux for their calculations, while for single quadrant converters, the core losses will be halved compared to the data published. Most ferrite manufacturers will likewise recommend levels no higher than 200 mT for the highest flux swing, to cover the complete temperature and operating conditions. Most ferrites have the lowest core losses at between 75 and 95°C. As the temperature in the transformer gradually rises, the efficiency of the transformer will increase.

To design a forward converter transformer, the following data is necessary:

F_{SW}	Operating Switching Frequency, usually 20 to 500 kHz
d_{max}	Maximum duty cycle, usually 50% in Siliconix products
h	Target efficiency, usually 0.75 to 0.85
V_{inmin}	Minimum input voltage used
P_{out}	Total output power
V_{out}	Output Voltage(s) required

In this case, a design for a 48-V (38- to 60-V), 5-V, 4-A (20-W) device operating at 50% duty cycle with 500-kHz switching frequency will be demonstrated. The period of conversion will be 2 µs, and the maximum on-time thus Tonmax = 1 µs.

The EF12.6, or the EPC13, which have similar characteristics, will be used as the core. The core operating flux has been selected to 85 mT as a first pass design. The loss in Philips 3F4 material is calculated from (source Philips Components):

$$P_v = 12x10^{-2} \cdot f^{1.75} \cdot B^{29} \cdot (0.95x10^{-4} \cdot T^2 - 1.1x10^{-2} \cdot T + 1.15)$$

Where:

P_V = power loss in W/m^3

B = operating flux density in Tesla

f = operating frequency in Hertz

T = core temperature in °C

With 500 kHz, 85 mT, and 50°C, the core loss can be calculated as:

$$P_v = 742.5 \times 10^3 \text{ W/m}^3 \text{ or } 0.742 \text{ W/cm}^3$$

The volume of the EF12.6 core is specified as 384 mm^3 or 0.384 cm^3.

Therefore the core loss will be:

$$P = 0.742 \times 0.384$$
$$P = 0.285 \text{ W} \approx 1/4 \text{ W}$$

which represents less than 2% of the total converter losses.

The converter transformer can be calculated by using the following adapted version of Faraday's equation:

$$N = \frac{V_{in\,min} \times t_{on\,max}}{B_{max} \times A_{eff}}$$

Where:

V_{inmax} = minimum input voltage (V)

N = number of turns (Integer)

B_{max} = maximum peak flux (Tesla)

A_{ef} = effective area of core (m^2)

In the case of the EF12.6, the minimum number of turns will be:

$$N = \frac{36 \text{ V} \times 1 \text{ µs}}{85 \text{ mT} \times 12.2 \text{ mm}^2}$$

N = 36.64 Turns [37 Turns

This is the calculated minimum number of turns that should be applied. To determine the turns for a given output voltage, first determine the output voltage (5 V). Then determine all the other losses that will exist in series with the output: including the choke, transformer dc losses, and rectifier forward drop. Assuming these add up to 0.5 V, with a duty cycle of 50%, the transformer will be required to supply a peak voltage of

Vsec = (Vout+Vloss)/Dmax

Vsec = (5 V + 0.5 V)/0.5 = 11 V

The transformer turns ratio is thus determined: for 36-V input, 11-V output is required. The turns ratio is therefore TR=36/11 = 3.27.

For the 5-V output, the number of turns required is:

NS=Np/TR = 11.01

Therefore, the number of turns selected is 11. The Si9114A will require a few miliamps of current to power itself and drive the power MOSFET. This power can be taken from a winding which peak charges a capacitor through a diode and does not require an inductor. In this case, 11 turns can also be taken (as this was calculated to be sufficient for 11 V).

Skin Depth

Conductors carrying high-frequency ac current are subject to a "skin effect" in which the current has a tendency to flow predominantly on the surface of the conductor instead through the whole cross section. The value at which the current falls to 1/e (37%) is called the "skin depth." Below this depth, very little usage of copper is made, and multiple

strands are required for applications where higher current is required. In some instances, it may be necessary to use larger wire than indicated, due to mechanical assembly constraints and ease of manufacture. The skin depth can be calculated from:

$$X_D = \frac{6.61}{\sqrt{f}} \text{ in. mm}$$

Operation at 500 kHz means that the skin depth will be 0.093 mm (or approximately 0.1 mm). Ideally, a conductor with a diameter just over twice the skin depth is recommended. In this case, therefore, 0.2 mm or thereabouts will suffice.

Leakage Inductance

In PWM converters, the coupling factor between windings should be optimized to minimize the leakage inductance. Leakage inductance is a parasitic element, storing energy that will need to be dissipated. This leakage is a measure of the quality of the coupling; the lower it is, the better the transformer and its performance. The leakage inductance can be measured by shorting out the 5-V winding and measuring the primary inductance. Ideally, this should be zero, but in reality values of less than 10% of the primary inductance are typical. This value can be minimized by splitting the primary winding in two halves, and by sandwiching all secondaries in between the two primary halves.

In this case, the transformer was wound as follows:

Winding Order	Winding Name	# Turns	Wire Size	Start Pin	End Pin
1	Half Primary	17	1x0.3 mm	1	10
2	Bias Winding	11	3x0.3 mm	3	9
3	Secondary	11	3x0.3 mm	4,5	7,6
4	Half Primary	18	1x0.3 mm	10	2

Copper wire of 0.3 mm was used to obtain single layer fill across the surface of the bobbin.

The wound transformer had the following characteristics:

Winding	Inductance	DC Resistance
Primary	883 µH	151 mΩ
Secondary	87 µH	25 mΩ

The leakage inductance was measured at 2.25 µH, which represents less than 1/4% of the primary inductance.

The configuration of the forward converter transformer is as follows (note the polarity/phasing of the windings):

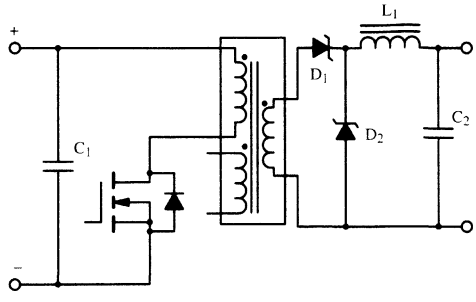


Figure 29

The above equations and calculations are supplied only as a guide for the designer. In practical terms other factors will must be considered, including the following:

- Effective required voltage adjustment range of output
- Losses in the primary side of the circuit, including the sense resistor and the MOSFET voltage drops
- Losses in the secondary side of the circuit, including dc losses in the output choke
- Forward voltage of the rectifier over load and temperature
- Interconnection losses, including remote sense drops
- OR-ing diode losses, if used in multiple converters.

Appendix B

Flyback Converter Transformer Design

The flyback magnetic component is often referred to as a transformer, but should in fact be viewed as an inductor with energy storage capability.

Two modes of operation are possible. In *discontinuous mode*, all the energy is transferred to the output(s). In *continuous mode*, some energy remains in the inductor. Discontinuous mode provides the advantages of a smaller inductor and the absence of unexpected or difficult transfer modes in the control mechanism. As energy transfer is complete, furthermore, rectifier currents always fall to zero before reverse voltages are applied. The result is lower rectifier switching losses.

For the sake of simplicity, it is recommended that only highly experienced designers use continuous mode, further information on which can be reviewed in some of the publications listed in the reference section of this application note. In this appendix, only the discontinuous mode is explained.

Due to the discontinuous nature of the energy transfer mechanism, flyback inductors are usually larger than the transformers encountered in forward and other Buck topologies, where only voltage transformation—and no energy storage—is performed.

To design a Flyback *Inductor*, the following information must be known:

F_{sw}	operating switching frequency (usually 20 to 500 kHz)
d_{max}	maximum duty cycle (usually 50% in Siliconix products)
n	target efficiency (usually 0.75 to 0.85)
V_{min}	minimum input voltage used
P_{out}	total output power
V_{out}	output voltage(s) required.

In this case, a design for a 24-V (16- to 30-V), 5-V, 2-A (10 W) inductor will be demonstrated.

The first step is to determine the minimum primary inductance from:

$$L_{pmin} = \frac{(V_{in\,min} \times t_{on\,max})^2 \times f_{sw} \times \eta}{2 \times P_{out}}$$

$$L_{pmin} = \frac{(18\ IV \times 2\ \mu s)^2 \times 250\ kHz \times 0.75}{2 \times 10\ W}$$

$$L_{pmin} = 12.2\ \mu H \approx 12\ \mu H$$

The next step is to determine the peak primary current. For a given inductor, the applied voltage will be:

$$V = L\frac{di}{dt}$$

Re-arranging yields:

$$i_{pk} = \frac{V_{in\,min} \times t_{on\,max}}{L_{pmax}}$$

$$i_{pk} = \frac{18\ V \times 2\ \mu s}{12\ \mu H} = 3\ A$$

The R.M.S. value for a triangular waveform can be used to calculate the power that will be dissipated in the MOSFET:

$$i_{ms} = i_{pk} \times \sqrt{\frac{\delta_{max}}{3}}$$

$$i_{ms} = 3\ A \times \sqrt{\frac{0.5}{3}} = 1.22\ A \approx 1.2\ A$$

To calculate the number of turns required for the 5-V output the following quotation can be used:

$$N_S = N_p \frac{(V_O + V_F)(1-D_{max})}{V_{inmin}\ D_{max}}$$

in this case, for $D_{max} = 0.5$ and $V_F = 0.6$ V for a 5 V output, the secondary turns will be:

$$N_S = N_p \frac{(5\ V + 0.6\ V)(1-0.5)}{16\ V \times 0.5}$$

Therefore

$$\therefore \frac{N_P}{N_S} = \frac{1}{0.35} = 2.86$$

The primary turns can be derived from the same equation used for the forward converter output indicator:

$$N_{min} = \frac{L_P \times I_{pK}}{B_{max} \times A_{min}} = \frac{12\ \mu H \times 3\ A}{200\ mT \times 13\ mm^2} = 13.85\ \text{Turns.}$$

$$\therefore N_{min} = 14\ \text{Turns.}$$

For 5 V, the number of turns will then be:

$$N_S = N_p \times 0.35 = 14 \times 0.35 = 4.9\ T \simeq 5\ T$$

In the flyback converter, all windings appear in parallel with each other, and will track the voltage of the controlled output. Small variations will be present due to the differences between Schottky and bipolar rectifiers. It must also be remembered that this will also cause the bias winding to collapse under short circuit conditions with possible overpower dissipation.

Si9117

High-Frequency Controller for Telecom Applications

Features

- On-board high-voltage, 1-Ω Switching FET
- Switching Frequencies of Up to 1 MHz
- Synchronization Capability
- Easily Compensated Current-Mode Operation
- Operates with Input Voltages Up to 200 V
- 1.8-MHz Error Amplifier
- Soft-Start
- Latched $\overline{\text{SHUTDOWN}}$

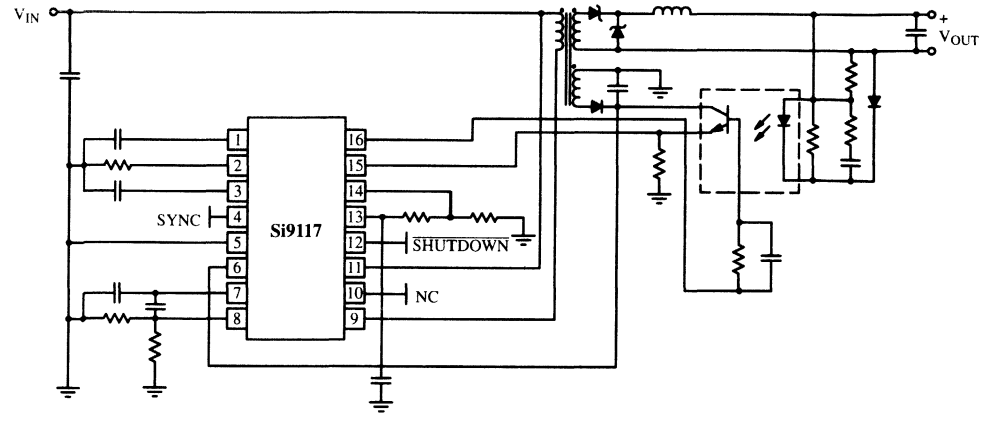
Description

The Si9117 high-efficiency controller for telecom systems running off 48 V is ideal for emerging applications such as interactive video (IV) set-top boxes and microcell base stations, such as those used for Personal Communications Systems (PCS). IV set-top boxes and microcell base stations typically require less than 15 W of power and have access to the analog telephone line power. Both IV set-top boxes and microcell base stations process extremely low-level, modulated analog signals (on the order of μVs), making the frequency and energy content of radiated and conducted noise a major issue. These application circuits are also constrained in terms of available board space and place a premium on minimal footprint.

The combination of an on-board, high-voltage, 1-Ω switch and a PWM IC with operational input voltage of 200 V allows operation off of the analog telephone line, even with the worst case battery voltage and ringing voltage. Once the controller has started up, a simple bootstrap circuit can provide power to the IC by raising the source voltage of the n-channel, depletion mode, start-up FET above its gate voltage of 9.2 V. This technique lowers system costs, reduces the area required for circuit implementation, and minimizes circuit power consumption.

Description Continued on Page 2.

Application Circuit



Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70027.

Description (Cont'd)

Processing high-frequency, modulated analog signals for video or RF requires receivers with sensitivities in the range of 0.5 to 25 µV. At these levels, noise generated by switchmode power conversion can impair the signal recovery process. Controlling radiated noise is a matter of proper layout and shielding. Controlling conducted noise is a matter of limiting its energy and isolating the conducted energy's fundamental and harmonic frequencies to bands which will not affect the frequencies of interest. The high-frequency, synchronized switching of the Si9117 enables this design requirement. First, for a given output current, high-frequency switching attenuates output ripple, minimizing conducted energy. Second, synchronizing the high switching frequency to an external frequency allows the fundamental and its harmonics to be moved out of range of the frequency bands of interest. An additional benefit of high-frequency switching is reduced size and cost of the inductor and the output filter capacitance.

In addition to these mandatory design considerations, the Si9117 is easy to design with and compensate, and takes a minimum of board area to implement: an important benefit in high-volume/small-package applications such as set-top boxes and microcell base stations.

Absolute Maximum Ratings

Voltages Referenced to $-V_{IN}$
V_{CC} ..... 18 V
$+V_{IN}$ (Note: $V_{CC} < +V_{IN} + 0.3$ V) ..... 200 V
Logic Input ($\overline{SHUTDOWN}$, SYNC) ..... –0.3 V to V_{CC} + 0.3 V
Linear Inputs (FEEDBACK, SENSE, SOFT-START) ..... –0.3 V to V_{CC} + 0.3 V
HV Pre-Regulator Input Current (continuous) ..... 5 mA
Storage Temperature ..... –65 to 150°C
Operating Temperature ..... –40 to 85°C
Junction Temperature (T_J) ..... 150°C
Drain-Source Voltage (T_A = 25°) (V_{DS})[a] ..... 200 V
Continuous Drain Current (T_A = 25°) (I_D)[a] ..... 1.0 A
Power Dissipation (Package)[a]
16-Pin SOIC (Y Suffix)[b] ..... 900 mW
Thermal Impedance (Θ_{JA})
16-Pin SOIC ..... 140°C/W

Notes
a. Device mounted with all leads soldered or welded to PC board, t ≤ 2 sec.
b. Derate 7.2 mW/°C above 25°C.

Recommended Operating Range

Voltages Referenced to $-V_{IN}$
V_{CC} ..... 9.5 V to 16.5 V
$+V_{IN}$ ..... 15 V to 200 V
f_{OSC} ..... 20 kHz to 2 MHz
R_{OSC} ..... 56 kΩ to 1 MΩ
C_{OSC} ..... 47 pF to 200 pF
Linear Inputs ..... 0 to V_{CC} – 4 V
Digital Inputs ..... 0 to V_{CC}

Specifications

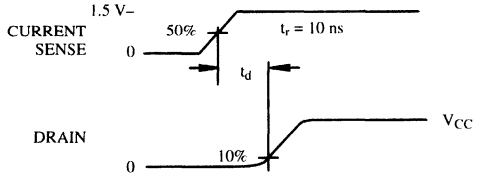
Parameter	Symbol	Test Conditions Unless Otherwise Specified Oscillator Disabled $-V_{IN}$ = 0 V, V_{CC} = 10 V		Limits D Suffix –40 to 85°C Min[a]	Typ[b]	Max[a]	Unit
Reference							
Output Voltage	V_R	OSC Disabled, T_A = 25°C		3.94	4.0	4.06	V
		OSC Disabled Over Voltage and Temperature Ranges[c]		3.88	4.0	4.12	
Short Circuit Current	I_{SREF}	$V_{REF} = -V_{IN}$			–30	–5	mA
Load Regulation	$\Delta V_R/\Delta I_R$	I_{REF} = 0 to –1 mA			10	40	mV
Oscillator							
Initial Accuracy	f_{OSC}[d]	R_{OSC} = 374 kΩ, C_{OSC} = 200 pF		90	100	110	kHz
		R_{OSC} = 70 kΩ, C_{OSC} = 200 pF		450	500	550	
Voltage Stability[c]	Δf/f	R_{OSC} = 70 kΩ, C_{OSC} = 200 pF Δf/f = |f(16.5 V) – f(9.5 V)| / f(9.5 V)			1	2	%
Temperature Coefficient[c]	OSC TC	–40 ≤ T_A ≤ 85°C, f_{OSC} = 100 kHz			200	500	ppm/°C
Sync Output Current (Master Mode)	$I_{SYNC(M)}$	V_{ROSC} ≤ 5 V		± 1.0	± 3.0		mA
Sync Output Current (Slave Mode)	$I_{SYNC(S)}$	$V_{ROSC} = V_{CC}$			± 1	± 500	nA
Error Amplifier ($C_{OSC} = -V_{IN}$ OSC Disabled)							
Input BIAS Current	I_{FB}	V_{FB} = 5 V, NI = V_{REF}			<1.0	± 200	nA
Input OFFSET Voltage	V_{OS2}				± 5	± 25	mV
Open Loop Voltage Gain[c]	A_{VOL}			65	80		dB
Unity Gain Bandwidth[c]	BW			1.8	2.7		MHz
Output Current	I_{OUT}	Source (V_{FB} = 3.5 V, NI = V_{REF})			–2.7	–1.0	mA
		Sink (V_{FB} = 4.5 V, NI = V_{REF})		1.0	2.4		
Power Supply Rejection	PSRR	9.5 V ≤ V_{CC} ≤ 16.5 V		50	80		dB
Pre-Regulator/Start-Up							
Input Leakage Current	$+I_{IN}$	$+V_{IN}$ = 200 V, V_{CC} ≥ 10 V			< 1	10	µA
Pre-Regulator Start-Up Current	I_{START}	$+V_{IN}$ = 48 V, t_{PW} ≤ 300 µs, $V_{CC} = V_{UVLO}$		8	20		mA
V_{CC} Pre-Regulator Voltage	V_{PR}	$+V_{IN}$ = 48 V		8.8	9.1	9.4	V
$V_{PR} - V_{UVLO}$ (Turn-On)	V_{DELTA}			0.1	0.25	0.7	
Undervoltage Lockout Hysteresis	V_{HYST}			0.18	0.28	0.4	
Supply							
Supply Current	I_{CC}	C_{LOAD} ≤ 50 pF	f_{OSC} = 100 kHz		1.8	2.5	mA
			f_{OSC} = 500 kHz		3.7	4.5	
Protection							
Current Limit Threshold Voltage	V_{SENSE}	V_{FB} = 0 V, NI = V_{REF}		1.035	1.16	1.30	V
Current Limit Delay to Output[c]	t_d	V_{SENSE} = 1.5 V, See Figure 1			105	130	ns
$\overline{\text{SHUTDOWN}}$ Logic Threshold	V_{SD}				2.8	0.5	V

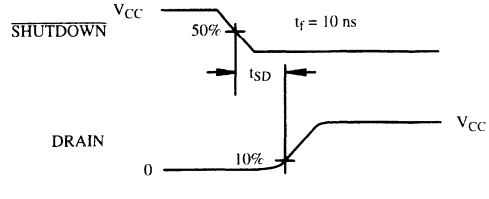
Specifications

Parameter	Symbol	Test Conditions Unless Otherwise Specified Oscillator Disabled $-V_{IN}$ = 0 V, V_{CC} = 10 V	Limits D Suffix –40 to 85°C Min[a]	Typ[b]	Max[a]	Unit
Protection (Cont'd)						
$\overline{\text{SHUTDOWN}}$ Delay to Latched Output[c]	t_{SD}	See Figure 2		0.21	1.0	µs
$\overline{\text{SHUTDOWN}}$ Pull-Up Current	I_{SD}	V_{SD} = 0 V	12	22	30	µA
Soft-Start Current	I_{SS}		12	22	30	
Output Inhibit Voltage	$V_{SS(off)}$	Soft-Start Voltage to Disable Driver Output		1.6	0.5	V
Switch						
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS} = 200 V, V_{GS} = 0 V, T_A = 25°C		0.7	5	µA
Drain-Source On-State Resistance[e]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 1.0 A, T_A = 25°C		0.8	1	Ω

Notes
a. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum.
b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
c. Guaranteed by design, not subject to production test.
d. $C_{STRAY} \leq 5$ pF on C_{OSC}.
e. Pulse Test; Pulse Width ≤ 300 µs, Duty Cycle ≤ 2%.

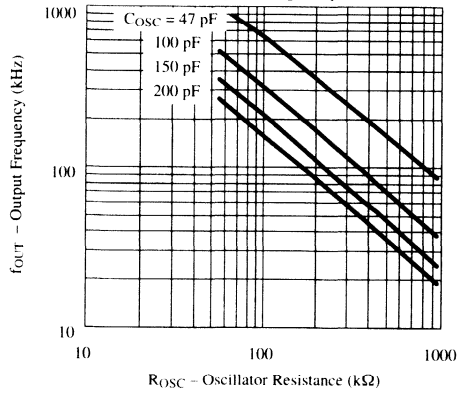
Timing Waveforms



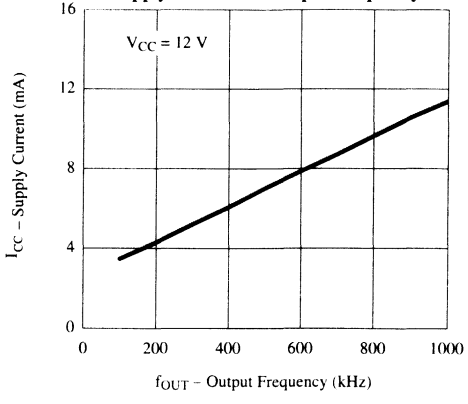


Typical Characteristics (25°C Unless Noted)

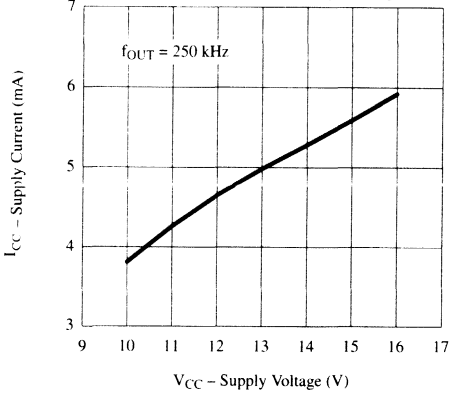
Output Frequency



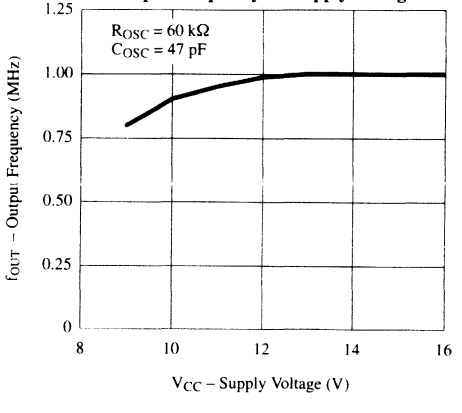
Supply Current vs. Output Frequency



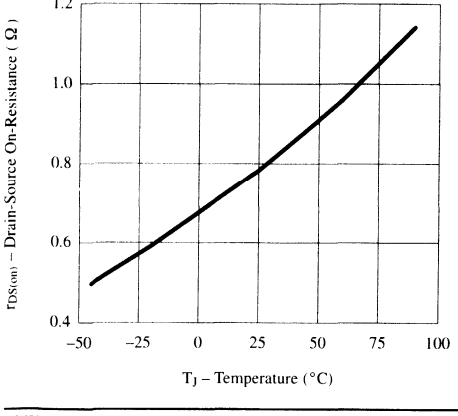
Supply Current vs. Supply Voltage



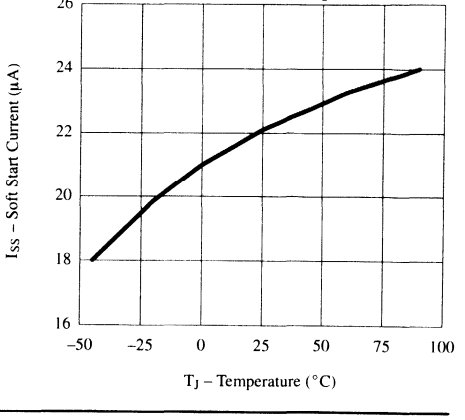
Output Frequency vs. Supply Voltage



Drain-Source On Resistance vs. Temperature



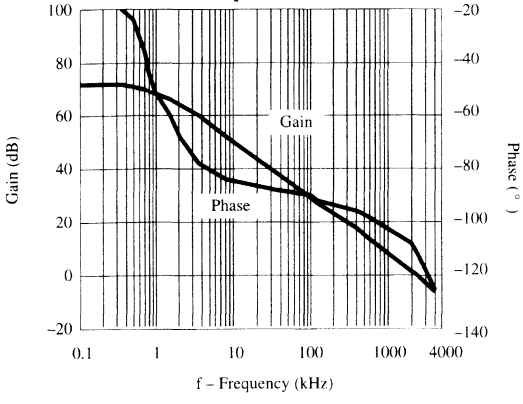
I_{SS} (Soft-Start) vs. Temperature



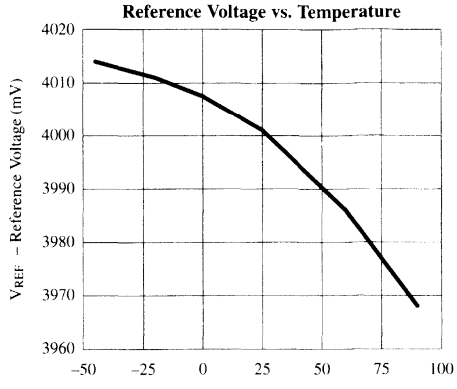
1 Power Conversion

Typical Characteristics (25°C Unless Noted)

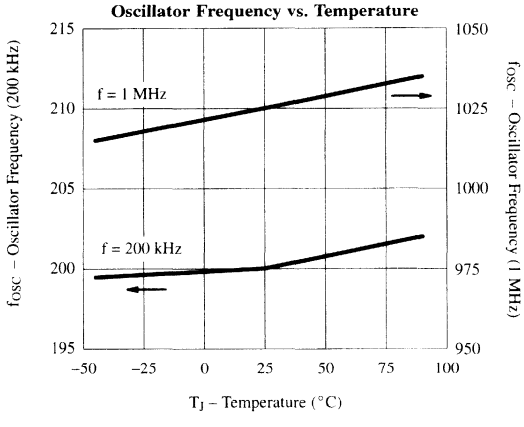
Error Amp Gain and Phase



Reference Voltage vs. Temperature

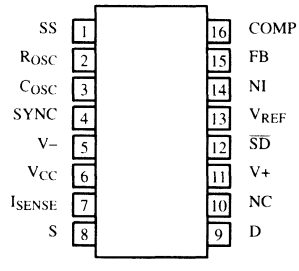


Oscillator Frequency vs. Temperature



Pin Configurations

16-Pin SOIC



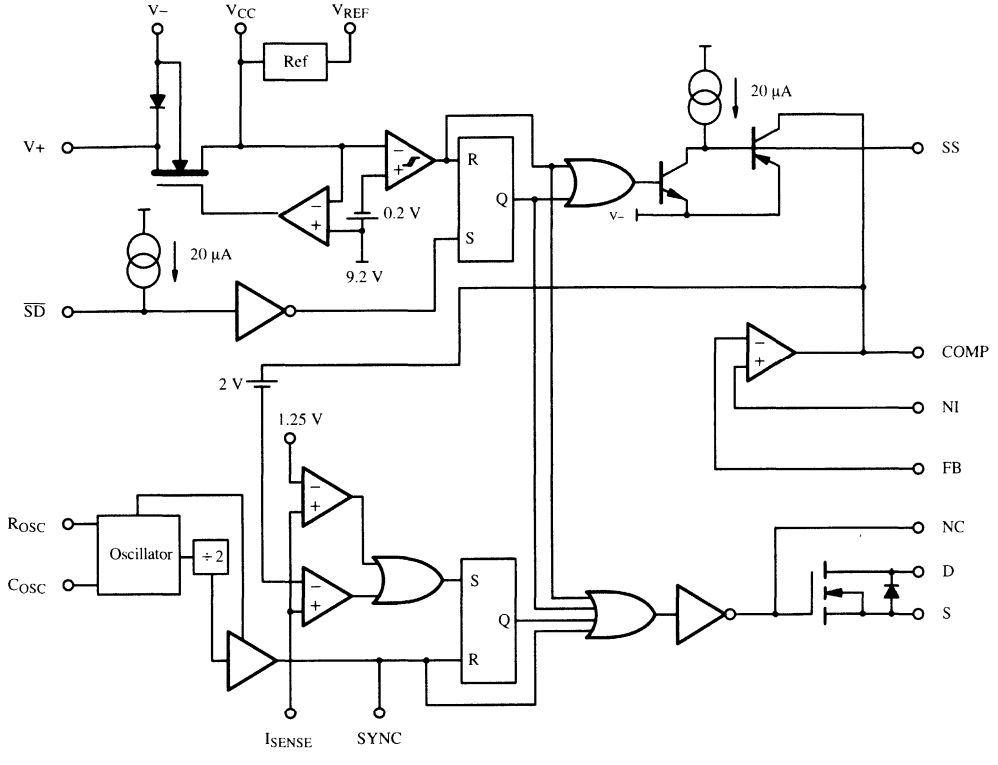
Top View

Order Number: Si9117DY

Pin Description

Pin Number	Symbol	Description
1	SS	Generates a 20-µA current source. IC turns or when capacitor is charged to 4.6 V.
2	R_{OSC}	Sets the oscillator charging current. Use the "oscillator frequency vs. R_{OSC}" curve in The Typical Characteristics section.
3	C_{OSC}	Sets oscillator frequency. Use the "Oscillator frequency vs. R_{OSC}" curve in the Typical Characteristics section along with equations 1 and 2 in the Oscillator section of the Description of Operations.
4	SYNC	Synchronization input overrides the oscillator. Slave mode operations is possible, as is operation of the controller at duty cycles >50%. See Oscillator section of the Description of Operations.
5	V–	Ground or negative mode of input power supply.
6	Vcc	Bootstrap power supply pin
7	I_{SENSE}	Current-mode sense input
8	S	Switch FET source.
9	D	Switch FET drain.
10	NC	No connect: for test purposes only. (Normally left open)
11	V+	High voltage (up to 200 V) power supply input.
12	$\overline{SD}$	$\overline{Shutdown}$. Logic low shuts down the controller.
13	V_{REF}	Output of the 4-V reference sources 5 mA.
14	NI	Non-inverting input of the error amplifier. A resistor divider from the reference can be used to set this voltage.
15	FB	Inverting input to the error amplifier; used to maintain output regulation.
16	Comp	Output of the error amplifier. Used to provide compensation for the controller's feedback control loop.

Block Diagram



Applications

Description of Operation

The Si9117 is a current mode PWM IC combined with an integrated 1-Ω 200-V MOSFET. Current mode operation offers the following advantages:

- Cycle-by-cycle current limit protection
- Simple loop compensation, eliminating the effect of output inductor
- Excellent fast transient response due to inner control loop
- Automatic input voltage feed-forward compensation

In addition, the Si9117 is duty-cycle limited to avoid core saturation.

High Voltage Pre-Regulator

All switchmode power supplies face a start-up problem caused by the large difference between dc bus voltage and the V_{CC} power rail for supplying the control circuit. The traditional technique has been to keep the control circuit in "sleep mode," while a small amount of energy is used to "top up" a large enough electrolytic capacitor to get the circuit started. When the circuit starts operating, a winding on the transformer is then used to power the control circuit. Disadvantages with this type of circuit include delayed start-up and large required capacitances for guaranteed operation over the full voltage range. The Si9117 overcomes these problems by using low power consumption, BiC/DMOS circuitry, and a unique high-voltage depletion mode MOSFET (see Figure 1).

When power is first applied, the depletion transistor is on, and current flows from the input capacitor C_{IN} into the V_{CC} capacitor C_{VCC} until V_{CC} reaches 9.2 V. The converter transformer will then supply the V_{CC} through a bias winding, which will raise V_{CC} to a level higher than 9.2 V. Ideally this will be between 11 and 13 V, thus turning off the high-voltage depletion mode MOSFET. The 9.2-V threshold has a hysteresis of 300 mV to prevent oscillations when the transition voltage is not clearly defined or when high-line supply impedance is encountered.

For applications where the input dc voltage is not high, and the chip power consumption is not excessive, the feedback winding can be eliminated. In such cases, the pre-regulator circuit will behave just like a linear regulator with 9.2-V output and 10-kΩ series resistance. In this case, the parameters to be considered are the dropout voltage at lowest line condition and the power dissipation at highest voltage. The high-voltage depletion mode MOSFET contains an internal body diode, and in situations where the V_{CC} is being powered from a laboratory supply, care must be taken to avoid loading the $+V_{IN}$ rail beyond the current rating of this device. Typically, the reverse characteristics of the device will generate a voltage of 3.4 V on Pin 11 with 10 kΩ load when powering V_{CC} from a lab supply.

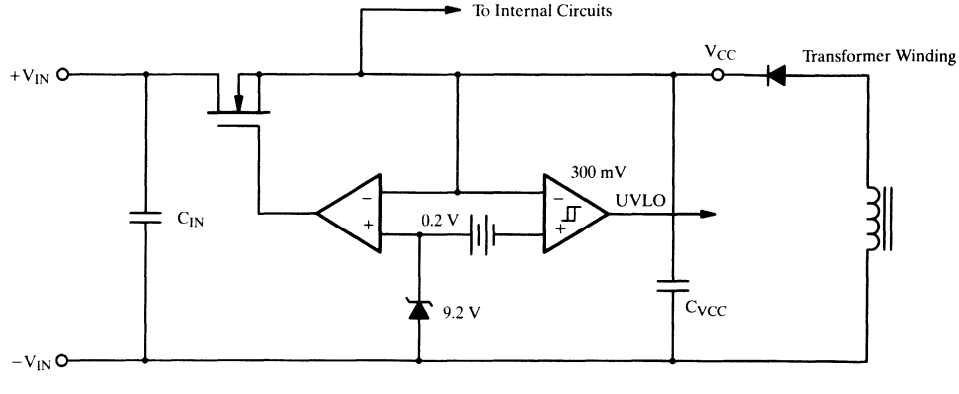


Figure 1. Start Circuit

In some applications it is necessary to inhibit the start of a converter until a high enough voltage is present on the supply bus. This is the case for the following reasons:

- Circuitry fed from a high line impedance such as a telephone line will have difficulty starting, since the converter will behave like a negative impedance. As the dc voltage decreases, the input current increases because constant power is drawn. This causes severe oscillations, and can in some instances have a destructive effect on the converter.
- During start-up, the Si9117 will begin operation as soon as the UVLO threshold is reached. Since the converter is designed to operate over a much higher range—for example, from 36 to 72 V—then between 10 and 36 V input the output voltage will be out of regulation and undefined. In some cases, digital circuitry will not accept this mode of operation, and system faults will be encountered without a RESET watchdog circuit.

To overcome these problems, a Zener diode of suitable value V_Z can be placed in series with the +Vin pin, preventing start-up until $V_Z + 9.2$ V is reached.

Shutdown

The shutdown pin is configured to allow fast latched termination of the output pulse. The delay from shutdown to output is typically 300 ns. This delay is short enough to allow this pin to be used for over-voltage applications where fast orderly shutdown is desirable: for example, when control of the feedback loop is lost.

Using an opto-coupler and a TL431, interface is easy (see Figure 2). Once latched, the shutdown can only be reset from the UVLO circuit by re-cycling the power. In the event of an over-voltage, the latch can be reset by momentarily pulling the V_{CC} to a value lower than the UVLO threshold. This approach will generally be acceptable, since the feedback winding will not be supplying power, and the only power maintaining the latch will be supplied by the depletion start transistor. Note, however, that this action will still be subject to the power dissipation limits of the Si9117 package and should ideally be applied as a short fast pulse.

Reference

The reference voltage is a fully buffered band gap type which can source 5 mA over the specified voltage tolerance range. The reference should be well de-coupled to prevent instability and jitter. A ceramic 100-nF or small tantalum is recommended, depending on the de-coupling present on the supply pins.

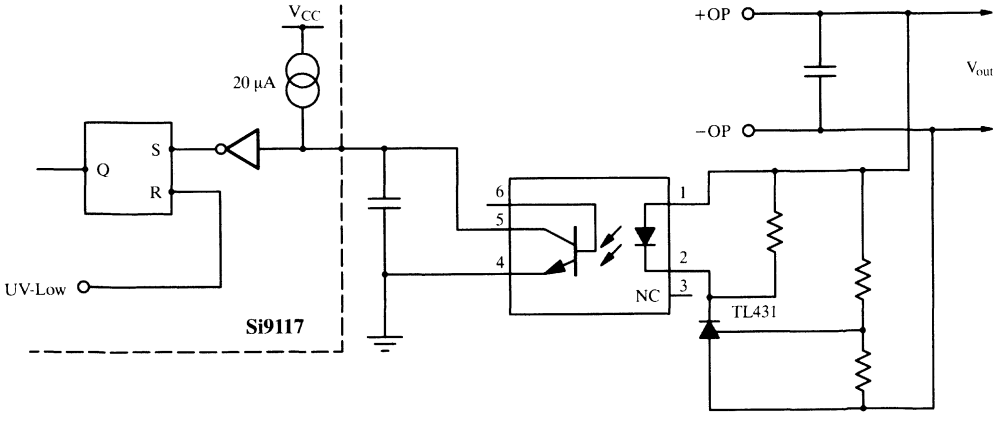


Figure 2. Shutdown

Error Amplifier

The error amplifier consists of a PMOS input folded cascade gain stage followed by a class AB unity gain amplifier. Typical open loop voltage gain is 77 dB, and unity gain bandwidth is typically 2.7 MHz. The soft-start circuit (see Pin 1 description) forces the output to within 0.7 V above ground, and additional clamp diodes limit the positive output excursion to within $2xV_{BE}$ above V_{REF}. Operation at high frequency allows high closed loop bandwidths and permits excellent transient response to both input and output changes. Under normal operation, a small 100-pF bypass capacitor is recommended from N_{INV} to Comp to increase high-frequency noise rejection. This should be calculated, however, in conjunction with the loop dynamics.

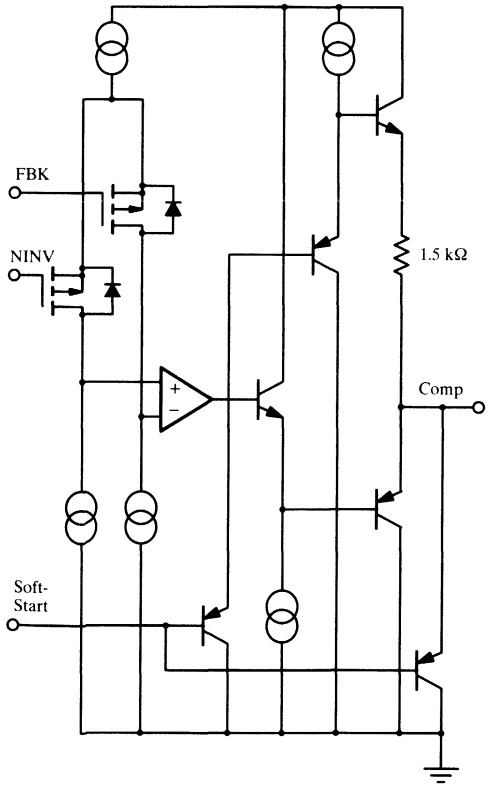


Figure 3. Operational Amplifier

Soft-Start

The soft-start circuit is designed to help dc-to-dc converters start in an orderly manner and reduce component stress. The output of the error amplifier is clamped by a PNP transistor.

The external capacitor C_{SS} is supplied by a 20-µA current source and will charge linearly to 4.6 V. In the event of an under-voltage lockout (or during start-up), this capacitor is held low. Soft-start is a very important feature and has many beneficial effects, especially in applications connecting to telecom lines where source impedances are high. In such cases, there is an initial start-up current caused by the input capacitor, followed by a secondary peak caused by the converter running at maximum duty cycle while trying to reach regulation. Where large output capacitances and peak loads are encountered, oscillations may occur. These can be prevented with the use of long soft-start times. The soft-start pin can also be used as a non-latching shutdown pin by connecting it to $-V_{IN}$. This approach allows a shutdown with soft re-start.

Oscillator

The oscillator circuit uses external timing components R_T and C_T. An internal divide-by-two prevents pulses with greater than 50% duty cycle, so that core saturation can be avoided. When the R_T terminal is connected to V_{CC}, comparator C_2 disconnects the oscillator output from the SYNC terminal using SW_1, and allows an external oscillator circuit to take control of the current mode comparator circuit.

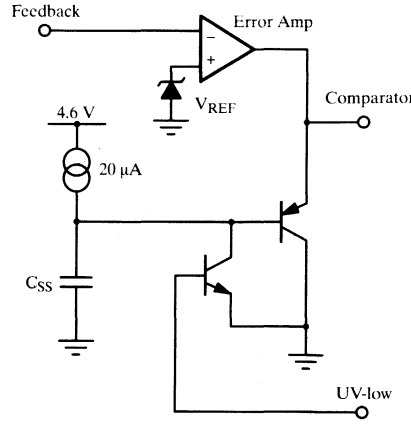


Figure 4. Soft-Start

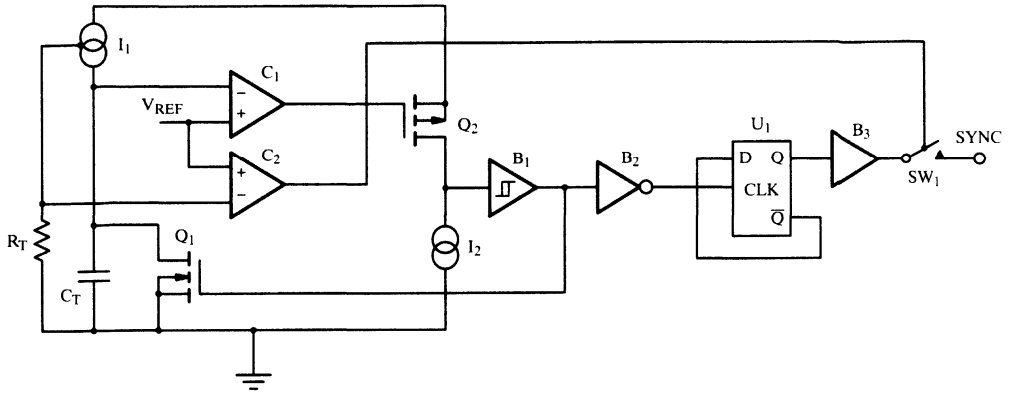


Figure 5. Oscillator

The current programmed by R_T defines the charging current of C_T and the on and off times with the following design equations:

$$T_{ON} = \frac{1.025 \times R_T \times C_T}{8} \quad (1)$$

$$T_{OFF} = 5 \times R_{ql} \times C_T \quad \text{where } R_{ql} = 25\ \Omega \quad (2)$$

$$F_{OSC} = \frac{1}{2} \times \frac{1}{(T_{ON} + T_{OFF})} \quad (3)$$

Actual values taken from a prototype board have been plotted (Figure 6), and are a close match (except for 47 pF, where stray parasitics have a more significant effect).

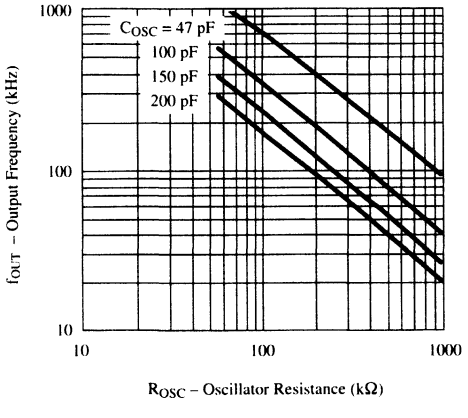


Figure 6. Oscillator Frequency Selection

In certain circumstances, such as current limiting, it may be desirable to change the frequency of the converter for a period of time to overcome current tails (see Figure 14 for further explanation). With the Si9117, this is easily done by adding or subtracting some current into the R_T terminal:

- The charging current in C_T is set by 8 × R_T.
- The voltage at the R_T terminal is 4 V, as supplied by an internal emitter follower from the reference.

The frequency can be changed easily by supplying some of the current into R_T from the V_{CC} rail, thus "starving" the internal current source, and slowing the frequency down.

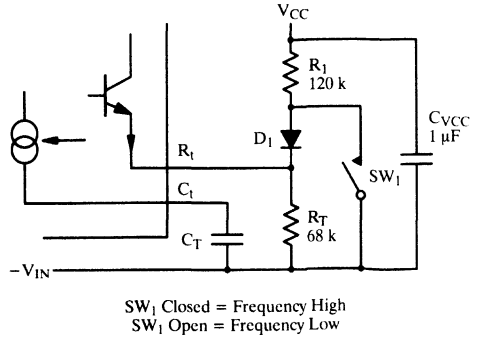


Figure 7. Frequency Shifting Using R_t Current Change

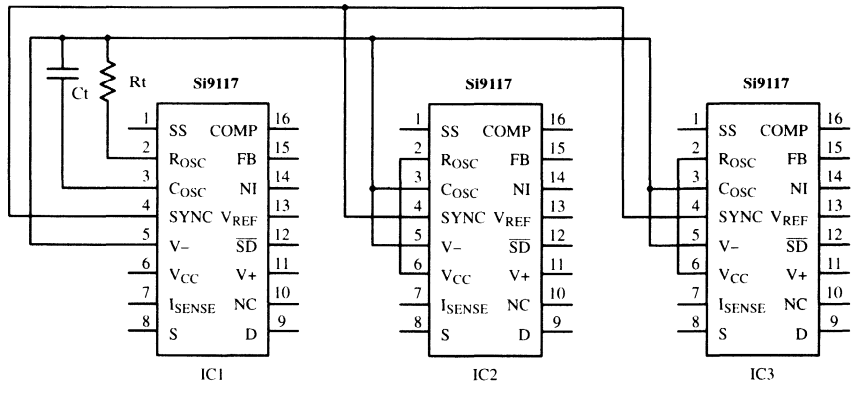


Figure 8. Oscillator Synchronization

The current in R_T is set by V = IR where V = 4 V and R = R_T. Using a diode, and some type of switch, the frequency can be easily changed: when SW_1 is closed, D_1 is reverse biased, and has no effect on R_T. When SW_1 is open, current flows through R_1 and D_1 into R_T and removes some of the current supplied by the internal emitter follower.

Synchronization

The *SYNC* input allows operation from a master clock as the connection is made after the divide-by-two. As a result, synchronization in both frequency and phase is possible. This unique feature is important to systems designers who use multiple converters, where noise caused by an unsynchronized "beating" effect is present and causes difficult EMI/EMC problems. If an external clock is used, duty cycles of > 50% are possible due to the position of the *SYNC* pin , after the divide-by-two. Where > 50% conduction is used, core reset must be allowed, in order to prevent core saturation. Synchronization is in master/slave mode, with one device (the "master") setting the switching frequency and others (the "slaves") with disabled oscillators locked to it. Alternatively, all devices can be clocked using a master oscillator.

During slave mode, the unused C_T pin should be connected to ground, and the R_T to V_{CC}.

V_{IN} and V_{DD}

These pins are used for powering the Si9117 and should consequently be well de-coupled. In selecting the right de-coupling, the MOSFET gate drive requirements should be considered, as the de-coupling capacitor will also have to supply the required peak current. Generally speaking, the best combination would be a 1- to 10-µF electrolytic for bulk energy and a 100-nF ceramic for high-frequency bypass. The V_{CC} rail should be carefully observed at the switch on and off occurrences using ac de-coupling, and the peak voltage spikes should be measured. These should be less than 200 mV. Excessive noise on the V_{CC} will appear on other pins and may cause instability or jitter on the control waveforms.

Switch

The switch FET is designed specifically for converters in the 5- to 10-W power range. It has a 200-V V_{DS} rating with 1-Ω $r_{DS(on)}$. Using the Gate charge curve, for a gate drive of 12 V from the Si9117, the total gate charge for 100-V V_{DS} will be 10 nC. From Q = i x t, it is easy to deduce that with a 400 mA internal gate drive, a time of 50 ns will be obtained (see Figure 9).

Current Sense

The current sense comparator performs the current mode control function by comparing the output of the error amplifier (V_C) with the current in the output inductor. It is impractical to measure the output inductor current, but the rising slope of the current can supply all the necessary information if sampled in the MOSFET as a scaled equivalent. Certain precautions are necessary, however, due to data distortion, noise, and the rarity of ideal operating conditions.

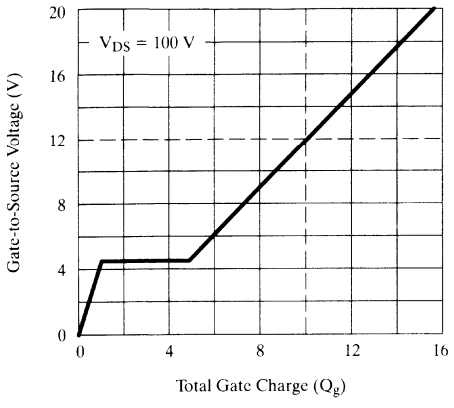


Figure 9. Si9117 Internal MOSFET Gate Charge

Sensed current waveforms often have leading-edge spikes or noise caused by reverse recovery of rectifiers, equivalent capacitive loading on the secondary, and inductive circuit effects. Inductive sense resistors must not be used, as they cause large damaging spikes and distort the sensed waveforms. These spikes can confuse the PWM comparator into believing that an overload condition is present. In addition, the Si9117 uses a single pin (–Vin) for all the return current requirements, including the output driver. As a result, the current pulse from the gate charge transfer into the MOSFET will appear on the sense pin and be filtered out.

Waveform A (Figure 11) has an ideal textbook appearance, but is in fact rarely encountered. Waveforms B and C are typical yet close to the threshold limit, and thus could lead to instability. The addition of a simple RC network on the sensed waveform suppresses this leading-edge spike. The low pass filter should be selected so that only the leading-edge spike is suppressed and the overall waveform is not distorted. The waveform must contain a clean rising slope for the error amplifier to intersect. If the RC time constant is too long, then the waveform will be distorted and lead to falling-edge jitter on the turn-off edge.

Slope compensation can also be used to eliminate noise or jitter. A sample of the oscillator voltage is superimposed on the error amplifier to produce a clean crossing of the thresholds and to avoid any hunting.

The Si9117 has built-in leading-edge blanking/ suppression to eliminate some of the effects of these spikes.

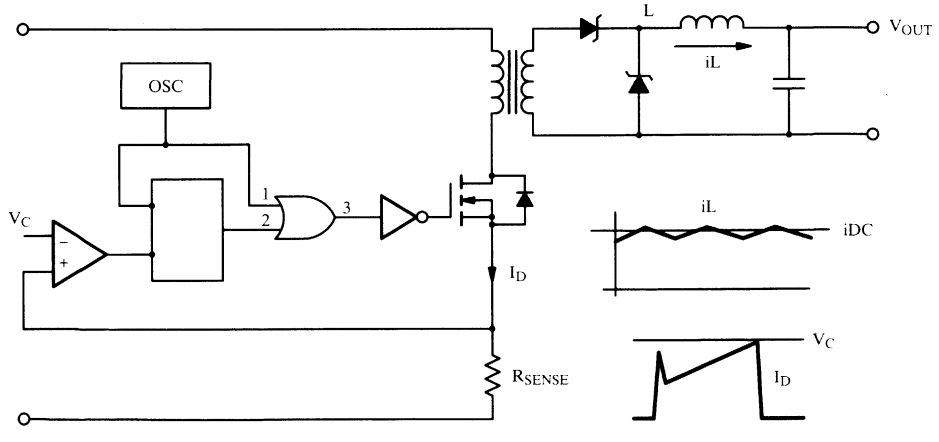


Figure 10. Constant Frequency Current Mode Control

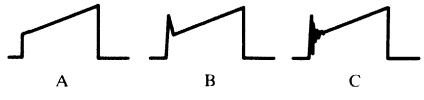


Figure 11. Current Waveforms

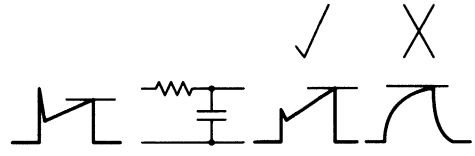


Figure 12. Current Sense Filtering Network

The two comparators used to operate the circuit have different delay times as follows:

- The current mode comparator needs more noise immunity, and therefore has a deliberately slower delay time to block out noise and spikes which are present on the leading edge. Typical delay times should be around 100 ns.
- The peak current limiting comparator has the fastest response time, since it is used only to protect the circuit in the event of an overload. The delay times for this comparator should be around 70 ns.

High-Frequency Design Requirements

When designing converters for high switching frequency, a certain discipline is required to determine the right choice of components. This process should be an iterative choice and the board layout should be properly planned before CAD layout is undertaken.

Layout Considerations

The main current loop flows from the input capacitor—through the transformer, MOSFET, and sense resistor—and returns to the capacitor. This current will have high rates of change and associated fast voltage and current edges. It is essential to avoid the injection of noise into the other circuitry.

To prevent this result, a "fishbone" type arrangement is recommended (Figure 13). Designers are encouraged to separate different grounds with "imaginary" dummy resistors. These can be removed at a later stage. Main current loops must be designed to be as short as possible: from C_{IN} to the transformer, through the MOSFET and Sense resistor, and back into C_{IN}. It is obvious that signals switching 50 V or 1 A in 25 ns should not be mixed with signals that are controlling a closed-loop, high-gain feedback system which is capable of regulating the output voltage to less than 1 mV.

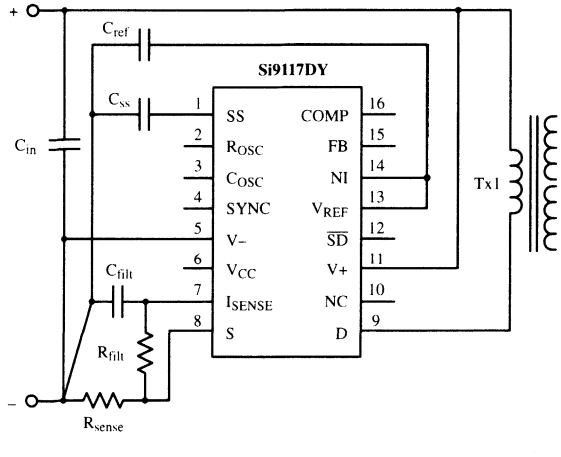


Figure 13.

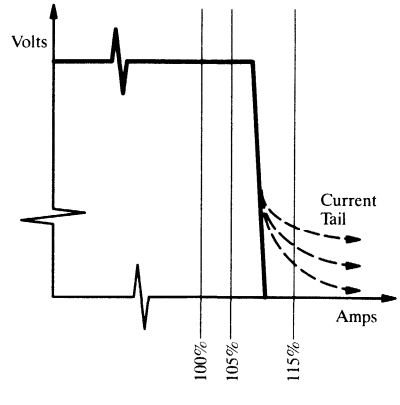


Figure 14.

Choosing the Switching Frequency

When selecting the switching frequency, it is usually best to choose the lowest possible frequency that the design solution will accept. In PWM control topologies, the maximum switching frequency will be strongly governed by short circuit behavior. When a short circuit is applied to the output, the control circuit is required to reduce the duty cycle to the smallest possible value to maintain constant current operation (Figure 14).

Ideally, the converter should deliver 105% of the output current within regulation and no more than 115% under short circuit. At 500 kHz, the period of conversion is 2 µs and the maximum on time is 1 µs. High minimum duty ratios will result in current tails and require rectifier oversizing to avoid destructive currents under overload conditions.

The Si9117 has a sync-to-output delay of less than 70 ns, so the minimum duty cycle for operation at 500 kHz would be 70 ns/1 µs = 7%. This minimum should be considered when the short circuit current is determined. Designers should note that a shunt placed across the output of the converter is probably not a realistic load in the event of a failure, and the real circuit impedance will probably be substantially lower. In such circumstances, it may be necessary to shift the frequency of the converter to a lower value during overload. Frequency shifting can be accomplished by altering the steady state values of the oscillator programming components (see oscillator section, Figure 7).

Short Circuit Behavior

Short circuit behavior is different for both common topologies, and must be paid special attention.

- In flyback converters, all windings appear in "parallel" with each other. When one winding is shorted, all other flyback windings are also shorted through it. In multiple output converters, therefore, any single winding without a separate secondary current-limiting protection will "drag down" all the other windings. As a result, if a bias winding is used to power the control circuit, it will stop delivering power. When this occurs, the Si9117 depletion device will turn on and regulate the supply rail to 9.2 V, as in its normal starting mode. In this event, designers should calculate the worst-case power dissipation caused by the voltage drop across the depletion transistor at the highest applied voltage across it and with the current flowing through it.

- In forward converters, traditionally the bias winding is also taken in forward conduction mode, but without any series inductance. In the event of a short circuit, the pulse width is reduced to minimum, but it is sufficient to supply enough power to the control circuit. This is an advantage, and avoids the problems encountered with flyback converters. Power may also be taken in flyback mode, however, when the duty cycle is low. There will be very little flyback voltage present, since the applied volt/microseconds is low and the core need not, therefore, fly back very far to reset.

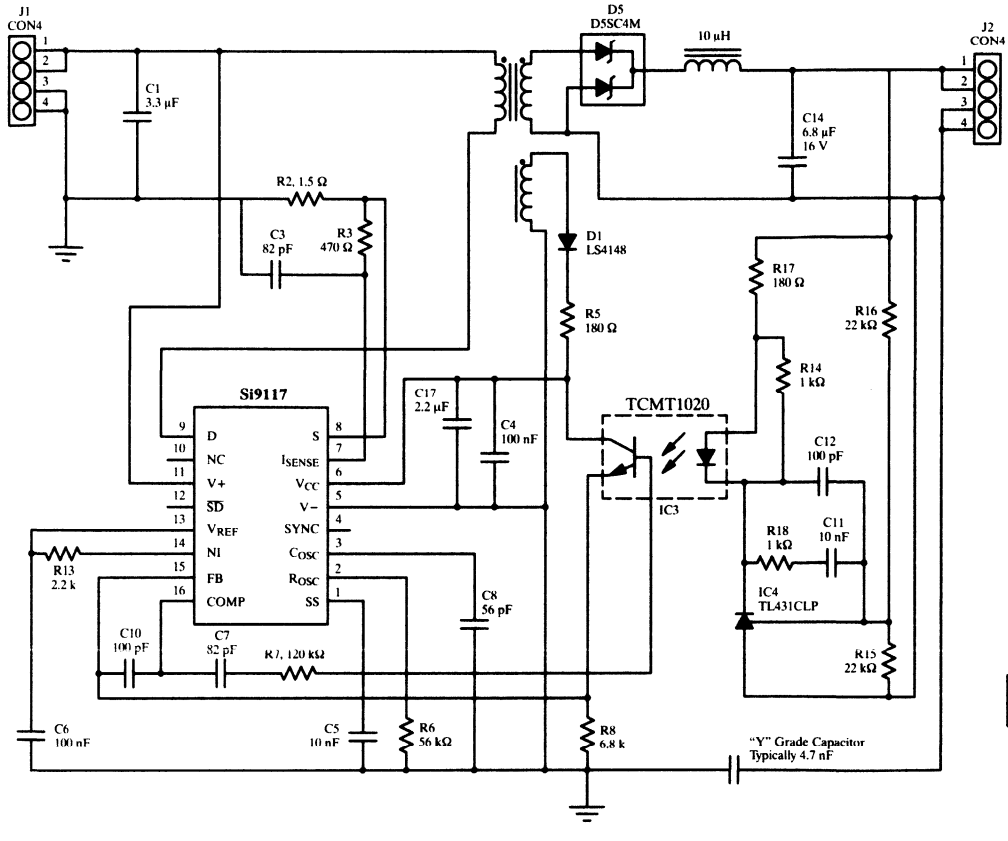


Figure 15. Complete Schematic Diagram

SMP Controller for High Performance Processor Power Supplies

Features

- Runs on 3.3- or 5-V Supplies
- Adjustable, High Precision Output Voltage
- High Frequency Operation (>1 MHz)
- High Efficiency Synchronous Switching
- Full Set of Protection Circuitry

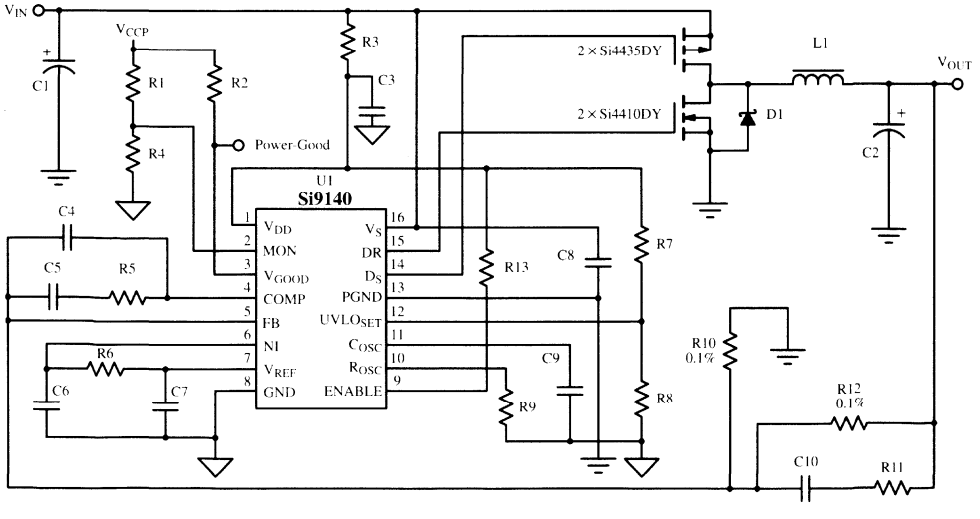
Description

Siliconix' Si9140 Buck converter IC is a high-performance, surface-mount switchmode controller made to power the new generation of low-voltage, high-performance microprocessors. The Si9140 has an input voltage range of 3 to 6.5 V to simplify power supply designs in desktop PCs. Its high-frequency switching capability and wide bandwidth feedback loop provide tight, absolute static and transient load regulation. Circuits using the Si9140 can be implemented with low-profile, inexpensive inductors, and will dramatically minimize power supply output and processor decoupling capacitance. The Si9140 is designed to meet the stringent regulation requirements of new and future high-frequency microprocessors, while improving the overall efficiency in new "green" systems.

Today's state-of-the-art microprocessors run at frequencies over 100 MHz. Processor clock speeds are going up and so are current requirements, but operating voltages are going down. These simultaneous changes have made dedicated, high-frequency, point-of-use buck converters an essential part of any system design. These point-of-use converters must operate at higher frequencies and provide wider feedback bandwidths than existing converters, which typically operate at less than 250 kHz and have feedback bandwidths of less than 50 kHz. The Si9140's 100-kHz feedback loop bandwidth ensures a minimum improvement of one-half the required output/decoupling capacitance, resulting in a tremendous reduction in board size and cost of implementation.

With the microprocessing power of any PC representing an investment of hundreds of dollars, designers need to ensure that the reliable operation of the processor will not be affected by the power supply. The Si9140 provides this assurance. A demo board, the Si9140DB, is available.

Application Circuit



Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70026.

Absolute Maximum Ratings

Voltages Referenced to GND.

V_{DD}, V_S ..... 8 V
P_{GND} ..... ±0.3 V
V_{DD} to V_S ..... –0.3 V
Linear Inputs ..... –0.3 V to V_{DD} to +0.3 V
Logic Inputs ..... –0.3 V to V_{DD} to +0.3 V
Peak Output Drive Current ..... 350 mA
Storage Temperature ..... –65 to 125°C
Operating Junction Temperature ..... 150°C
Power Dissipation (Package)[a]
16-Pin SOIC (Y Suffix)[b] ..... 900 mW
Thermal Impedance (Θ_{JA})
16-Pin SOIC ..... 140°C/W

Notes
a. Device mounted with all leads soldered or welded to PC board.
b. Derate 7.2 mW/°C above 25°C.

* *Exposure to Absolute Maximum rating conditions for extended periods may affect device reliability. Stresses above Absolute Maximum rating may cause permanent damage. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum rating should be applied at any one time*

Recommended Operating Range

Voltages Referenced to GND.

V_{DD} ..... 3 V to 6.5 V
V_S .....
f_{OSC} ..... 2 kHz to 2 MHz
R_{OSC} ..... 5 kΩ to 250 kΩ
C_{OSC} ..... 47 pF to 200 pF
Linear Inputs ..... 0 to V_{DD}
Digital Inputs ..... 0 to V_{DD}
V_{REF} Load Resistance ..... >150 kΩ

Specifications

Parameter	Symbol	Test Conditions Unless Otherwise Specified[a] 3 V ≤ V_{DD} ≤ 6.5 V, V_{DD} = V_S GND = P_{GND}	Limits C Suffix 0 to 70°C Min[b]	Typ	Max[b]	Unit
Reference						
Output Voltage	V_{REF}	I_{REF} = –10 µA	1.455		1.545	V
		T_A = 25°C	1.477	1.50	1.523	
Oscillator						
Maximum Frequency[c]	f_{MAX}	V_{CC} = 5 V, C_{OSC} = 47 pF, R_{OSC} = 5.0 kΩ	2.0			MHz
Accuracy	f_{OSC}	V_{CC} = 5 V C_{OSC} = 100 pF, R_{OSC} = 7.50 kΩ, T_A = 25°C	0.85	1.0	1.15	
R_{OSC} Voltage	V_{ROSC}			1.0		V
Voltage Stability[c]	Δf/f	4 V ≤ V_{DD} ≤ 6 V, Ref to 5 V, T_A = 25°C	–8		8	%
Temperature Stability[c]		Referenced to 25°C	–5		5	
Error Amplifier (C_{OSC} = GND, OSC DISABLED)						
Input Bias Current	I_{FB}	V_{NI} = V_{REF}, V_{FB} = 1.0 V	–1.0		1.0	µA
Open Loop Voltage Gain	A_{VOL}			55		dB
Offset Voltage	V_{OS}	V_{NI} = V_{REF}	–15	0	15	mV
Unity Gain Bandwidth[c]	BW			10		MHz
Output Current	I_{EA}	Source (V_{FB} = 1 V, NI = V_{REF})		–2.0	–1.0	mA
		Sink (V_{FB} = 2 V, NI = V_{REF})	0.4	0.8		
Power Supply Rejection[c]	P_{SRR}	3 V < V_{DD} < 6.5 V		60		dB

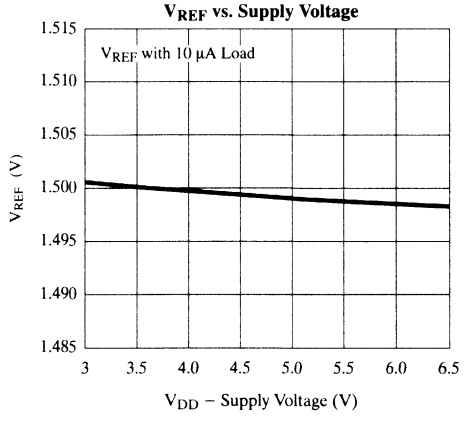
Specifications

Parameter	Symbol	Test Conditions Unless Otherwise Specified[a] 3 V ≤ V_{DD} ≤ 6.5 V, V_{DD} = V_S GND = P_{GND}	Limits C Suffix 0 to 70°C Min[b]	Typ	Max[b]	Unit
$UVLO_{SET}$ Voltage Monitor						
Under Voltage Lockout	V_{UVLOHL}	$UVLO_{SET}$ High to Low	0.85	1.0	1.15	V
	V_{UVLOLH}	$UVLO_{SET}$ Low to High		1.2		
Hysteresis	V_{HYS}	V_{UVLOLH} – V_{UVLOHL}		165		mV
UVLO Input Current	$I_{UVLO(SET)}$	V_{UVLO} = 0 to V_{DD}	–100		100	nA
Output Drive (D_R and D_S)						
Output High Voltage	V_{OH}	V_{DD} = 5 V, I_{OUT} = –10 mA	4.7	4.8		V
Output Low Voltage	V_{OL}	V_{DD} = 5 V, I_{OUT} = 10 mA		0.2	0.3	
Peak Output Current	I_{SOURCE}	V_{DD} = 5 V, V_{OUT} = 0 V		–380	–260	mA
Peak Output Current	I_{SINK}	V_{DD} = 5 V, V_{OUT} = 5 V	180	300		
Break-Before-Make	t_{BBM}			30		nS
Logic						
ENABLE Turn-On Delay	$\Delta\emptyset_{EN}$	ENABLE Rising		1.5		Cycles
ENABLE Logic Low	V_{ENL}				0.2 V_{DD}	V
ENABLE Logic High	V_{ENH}		0.8 V_{DD}			
ENABLE Input Current	I_{EN}	ENABLE = 0 to V_{DD}	–1.0		1.0	µA
V_{GOOD} Comparator (Voltage-Good Comparator)						
Input Offset Voltage	V_{OS}	V_{IN} Common Mode Voltage = V_{REF}, V_{DD} = 5 V	–45	0	45	mV
Input Hysteresis	V_{INHYS}			10		
Input Bias Current	I_{BMON}	V_{IN} = V_{REF}, V_{DD} = 5 V	–1	0	1	µA
Output Sink I	I_{SINK}	V_{OUT} = 5 V, V_{DD} = 5 V	6	9		mA
Output Low Voltage	V_{OL}	I_{OUT} = 2 mA, V_{DD} = 5 V		350	500	mV
Supply						
Supply Current—Normal Mode	I_{DD}	f_{OSC} = 1 MHz, R_{OSC} = 7.50 kΩ		1.6	2.3	mA
Supply Current—Standby Mode		ENABLE < 0.4 V		250	330	µA

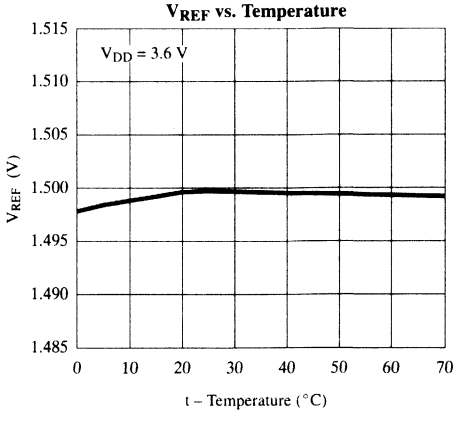
Notes
a. 100 pF includes C_{STRAY} on C_{OSC}.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
c. Guaranteed by design, not subject to production testing.

Typical Characteristics (25°C Unless Otherwise Noted)

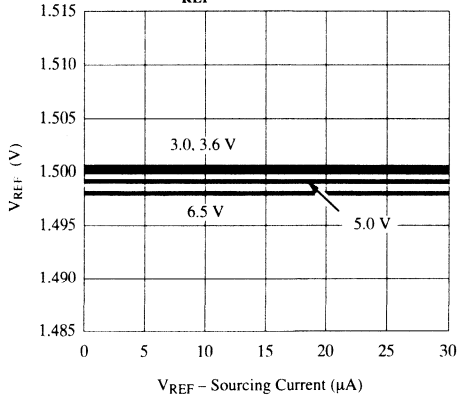
V_{REF} vs. Supply Voltage



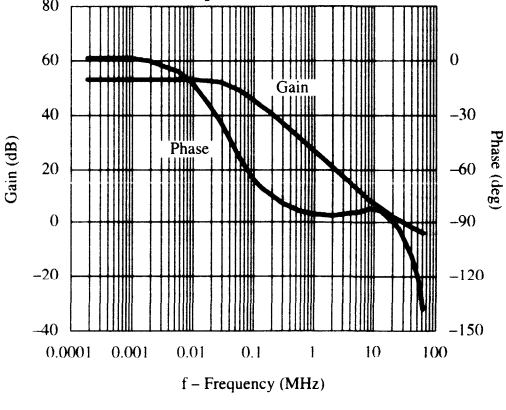
V_{REF} vs. Temperature



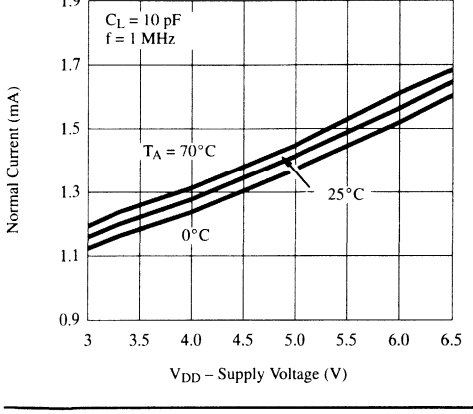
V_{REF} vs. Load Current



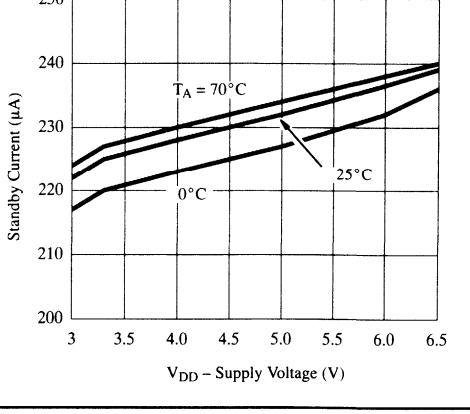
Error Amplifier Gain and Phase



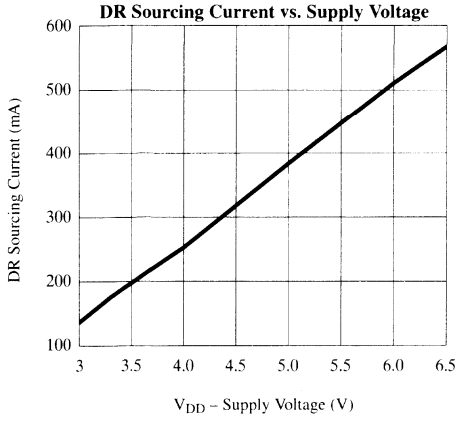
Supply Current vs. Supply Voltage and Temperature

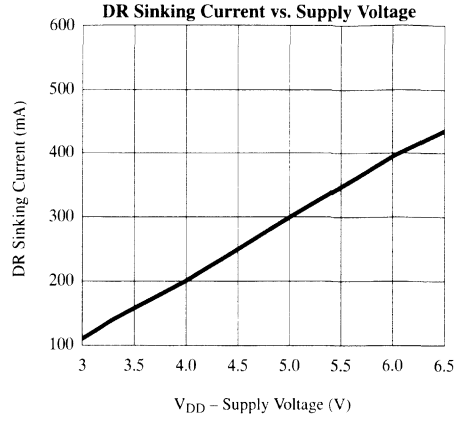


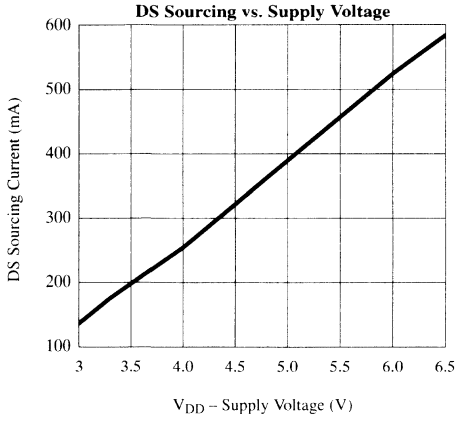
Standby Current vs. Supply Voltage and Temperature

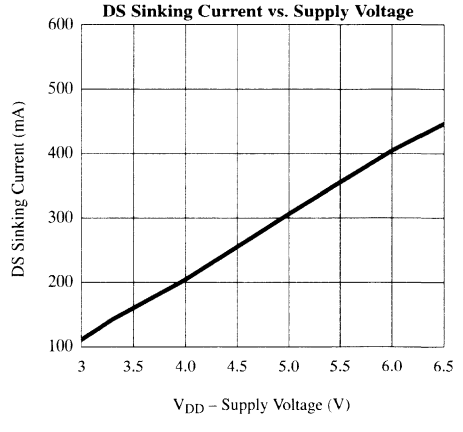


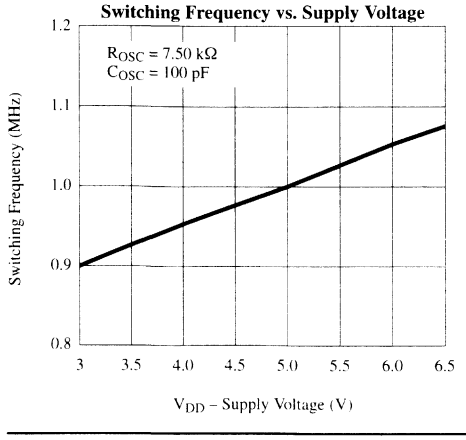
Typical Characteristics (25°C Unless Otherwise Noted)

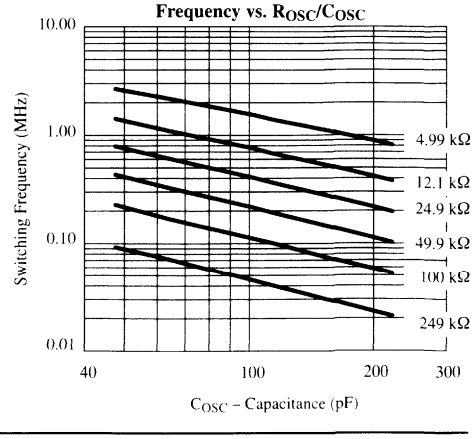






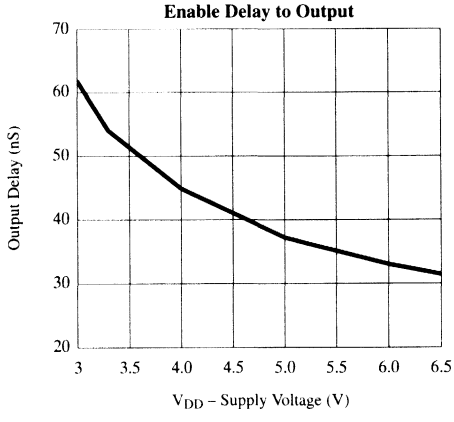




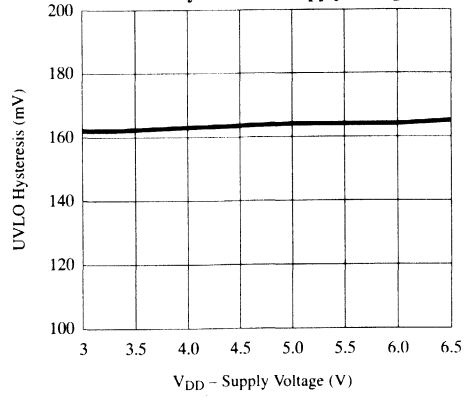


Typical Characteristics (25°C Unless Otherwise Noted)

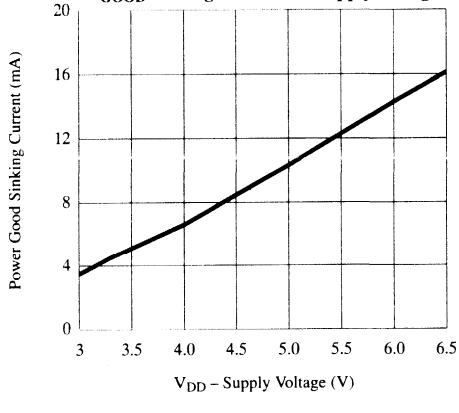
Enable Delay to Output



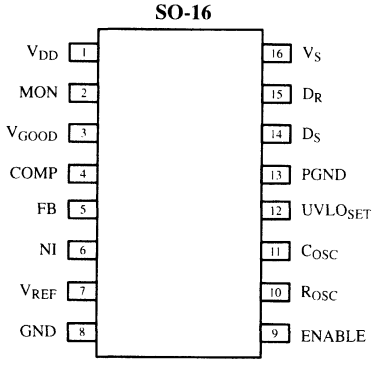
UVLO Hysteresis vs. Supply Voltage



V_{GOOD} Sinking Current vs. Supply Voltage



Pin Configurations



Order Number: Si9140CY

Pin Description

Pin 1: V_{DD}

The positive power supply for all functional blocks except output driver. A bypass capacitor of 0.1 µF (minimum) is recommended.

Pin 2: MON

Non-inverting input of a comparator. Inverting input is tied internally to reference voltage. This comparator is typically used to monitor the output voltage and to flag the processor when the output voltage falls out of regulation.

Pin 3: V_{GOOD}

This is an open drain output. It will be held at ground when the voltage at MON (Pin 2) is less than the internal reference. An external pull-up resistor will pull this pin high if the MON pin (Pin 2) is higher than the V_{REF}. (Refer to Pin 2 description.)

Pin 4: COMP

This pin is the output of the error amplifier. A compensation network is connected from this pin to the FB pin to stabilize the system. This pin drives one input of the internal pulse width modulation comparator.

Pin 5: FB

The inverting input of the error amplifier. An external resistor divider is connected to this pin to set the regulated output voltage. The compensation network is also connected to this pin.

Pin 6: NI

The non-inverting input of the error amplifier. In normal operation it is externally connected to V_{REF} or an external reference.

Pin 7: V_{REF}

This pin supplies a 1.5-V reference.

Pin 8: GND (Ground)

Pin 9: ENABLE

A logic high on this pin allows normal operation. A logic low places the chip in the standby mode. In standby mode normal operation is disabled, supply current is reduced, the oscillator stops and D_S goes high while D_R goes low.

Pin 10: R_{OSC}

A resistor connected from this pin to ground sets the oscillator's capacitor C_{OSC}, charge and discharge current. See the oscillator section of the description of operation.

Pin Description (Cont'd)

Pin 11: C_{OSC}

An external capacitor is connected to this pin to set the oscillator frequency.

$$f_{OSC} \simeq \frac{0.75}{R_{OSC} \times C_{OSC}} \quad (\text{at } V_{DD} = 5.0\ V)$$

Pin 12: $UVLO_{SET}$

This pin will place the chip in the standby mode if the $UVLO_{SET}$ voltage drops below 1.2 V. Once the $UVLO_{SET}$ voltage exceeds 1.2 V, the chip operates normally. There is a built-in hysteresis of 165 mV.

Pin 13: P_{GND}

The negative return for the V_S supply.

Pin 14: D_S

This CMOS push-pull output pin drives the external p-channel MOSFET. This pin will be high in the standby mode. A break-before-make function between D_S and D_R is built-in.

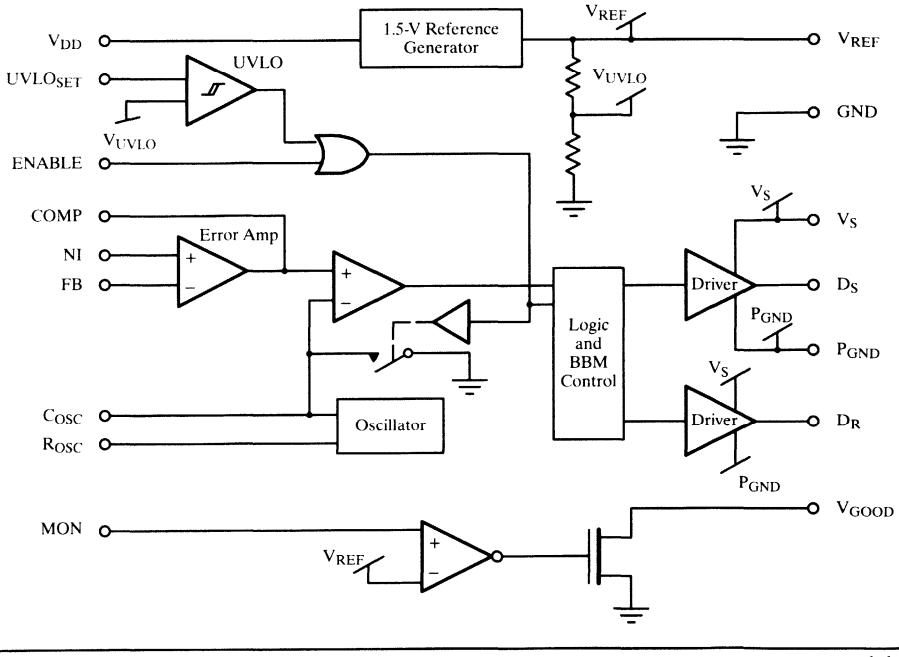
Pin 15: D_R

This CMOS push-pull output pin drives the external n-channel MOSFET. This pin will be low in the standby mode. A break-before-make function between the D_S and D_R is built-in.

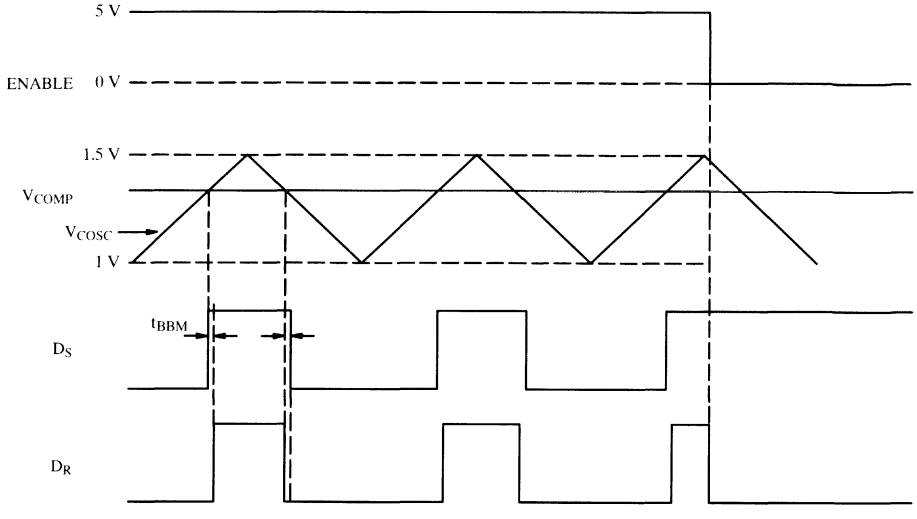
Pin 16: V_S

The positive terminal of the power supply which powers the CMOS output drivers. A bypass capacitor is required.

Functional Block Diagram



Timing Waveforms



Description of Operation

Schematics of the Si9140 dc-to-dc conversion solutions for high-performance PC microprocessors are shown in Figure 1 and 2 respectively. These solutions are geared to meet the extremely demanding transient regulation and power requirements of these new microprocessors at minimal cost and with a minimal parts count. The two solutions are nearly identical, except for slight variations in output voltage, load transient amplitude, and specified power. Figure 3 is a schematic diagram for a 3.3-V logic converter.

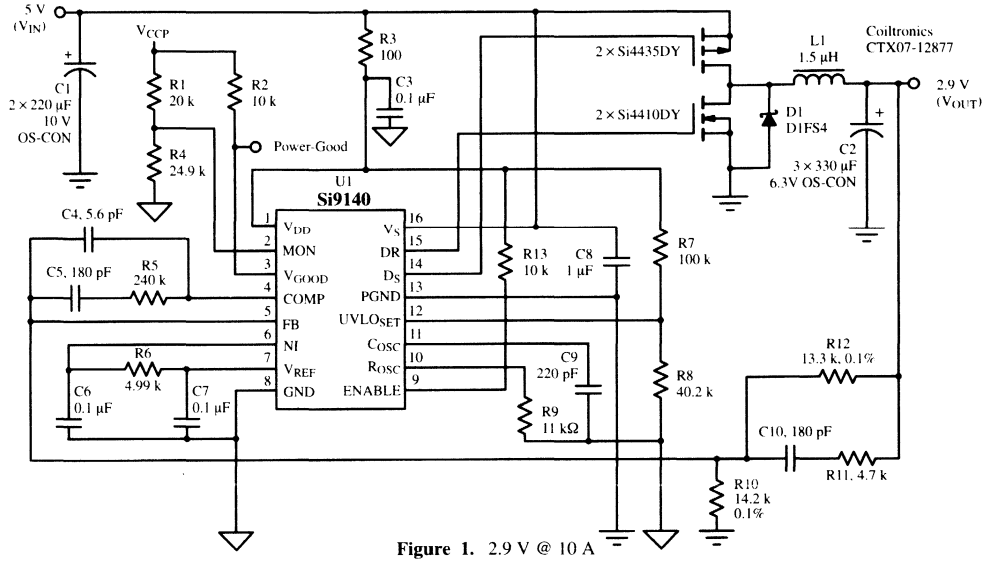


Figure 1. 2.9 V @ 10 A

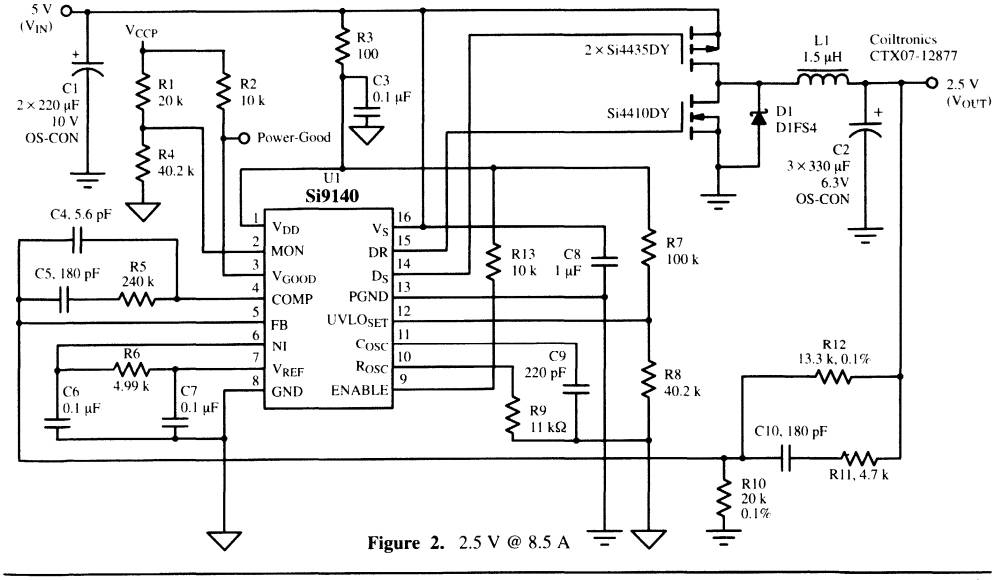


Figure 2. 2.5 V @ 8.5 A

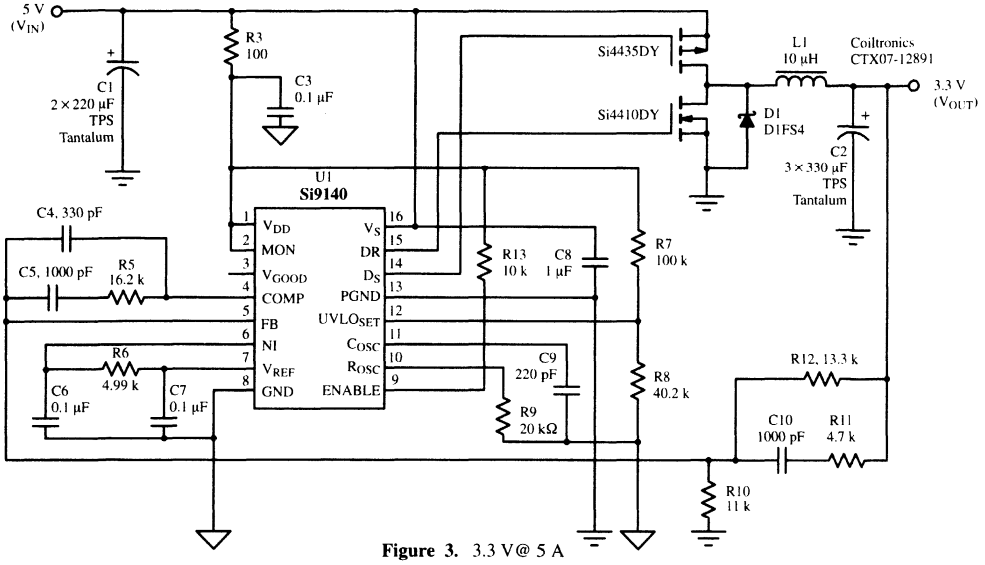


Figure 3. 3.3 V@ 5 A

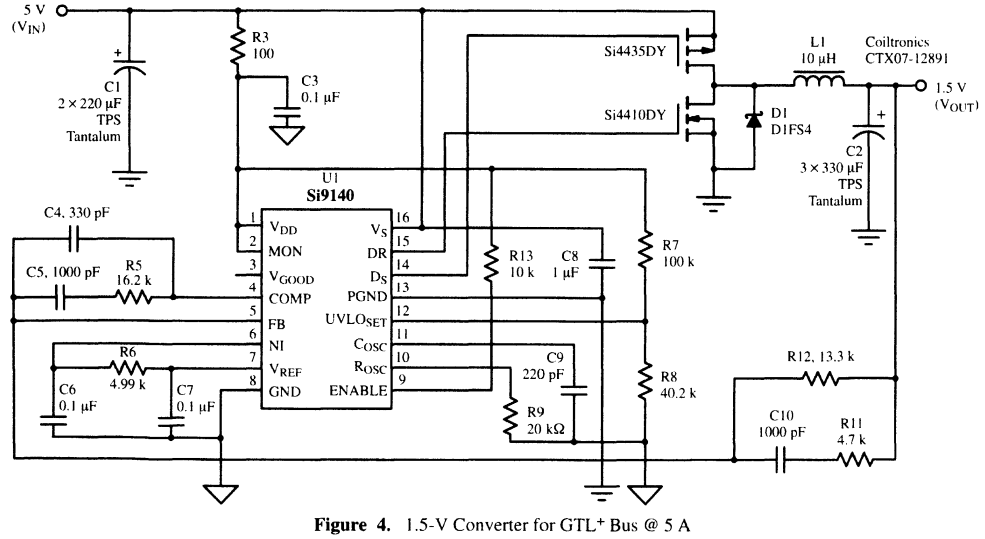


Figure 4. 1.5-V Converter for GTL+ Bus @ 5 A

Figure 4 is a schematic diagram of a converter which produces 1.5 V for a GTL bus.

Each of these dc-to-dc converters has four major sections:

- PWM Controller—regulates the output voltage
- Switch and Synchronous Rectification MOSFETs—delivers the power to the load
- Inductor—filters and stores the energy
- Input/Output Capacitor—filters the ripple

The functions of each circuit are explained in detail below. Design equations are provided to optimize each application circuit.

PWM Controller

There are generally two types of controllers, voltage mode or current mode. In voltage mode control, an error voltage is generated by comparing the output voltage to the reference voltage. The error voltage is then compared to an artificial ramp, and the result is the duty cycle necessary to regulate the output voltage. In current mode, an actual inductor current is used, in place of the artificial ramp, to sense the voltage across the current sense resistor.

The logic and timing sequence for voltage mode control is shown in Figure 5. The Si9140 offers voltage mode control, which is better suited for applications requiring both fast transient response and high output current.

Current mode control requires a current sense resistor to monitor the inductor current. A 10-mΩ sense resistor in a 10-A design will dissipate 1 W, decreasing efficiency by 3.5%. Such a design would require a 2-W resistor to satisfy derating criteria, besides requiring additional board space. Voltage mode control is a second-order LC system and has a faster natural transient response compared to current mode control (first-order RC system). Current mode has the advantage of providing an inherently good line regulation. But the situations where line voltage is fixed, as in the point-of-use conversion for microprocessors, this feature is wasted. Current mode control also provides automatic pulse-to-pulse current limiting. This feature requires a current sense resistor as stated above. These characteristics make voltage mode control ideal for high-end microprocessor power supplies.

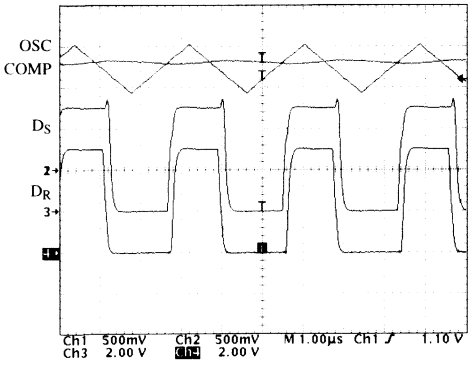


Figure 5. Voltage Mode Logic and Timing Diagram

The error amplifier of the PWM controller plays a major role in determining the output voltage, stability, and the transient response of the power supply. In the Si9140, the non-inverting input of the error amplifier is available for use with an external precision reference for tighter tolerance regulation. With a two-pair lead-lag compensation network, it is easy to create a stable 100-kHz closed loop converter with the Si9140 error amplifier.

The Si9140 achieves the 5-µS transient response by generating a 100-kHz closed-loop bandwidth. This is possible only by switching above 400 kHz and utilizing an error amplifier with at least a 10-MHz bandwidth. The Si9140 controller has a 25-MHz unity gain bandwidth error amplifier. The switching frequency must be at least four times greater than the desired closed-loop bandwidth to prevent oscillation. To respond to the stimuli, the error amplifier bandwidth needs to be at least 10 times larger than the desired bandwidth.

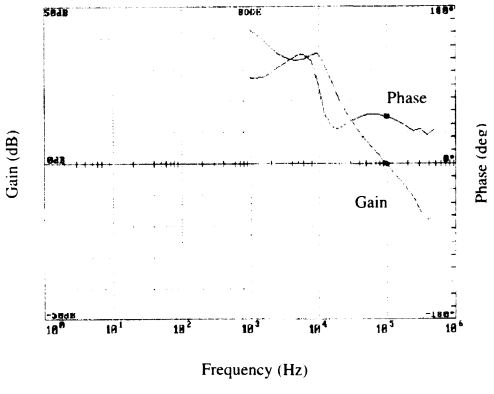


Figure 6. 100-kHz BW Synchronous Buck Converter

The Si9140 solution requires only three 330-µF OS-CON capacitors on the output of power supply to meet the 10-A transient requirement. Other converter solutions on the market with 20- to 50-kHz closed loop bandwidths typically require two to five times the output capacitance specified above to match the Si9140's performance.

The theoretical issues and analytical steps involved in compensating a feedback network are beyond the scope of this application note. However, to ease the converter design for today's high-performance microprocessors, typical component values for the feedback network are provided in Table 1 for various combinations of output capacitance. Figure 6 shows the Bode plot (frequency domain) of the 2.9-V converter shown schematically in Figure 1.

Table 1. Feedback Network Component Values

Total Output and Decoupling Capacitance	C8	C9	R4
3 x 330 µF[a] ..... Os-con 6 x 100 µF[b] ..... Tantalum 25 x 1 µF[b] ..... Ceramic	5.6 pF	180 pF	240 k
2 x 330 µF[a] ..... Os-con 4 x 100 µF[b] ..... Tantalum 25 x 1 µF[b] ..... Ceramic	10 pF	220 pF	200 k
3 x 330 µF[a] ..... Tantalum 4 x 100 µF[b] ..... Tantalum 25 x 1 µF[b] ..... Ceramic	10 pF	100 pF	100 k

a. Power supply output capacitance.
b. µprocessor decoupling capacitance.

Figure 7 is the measured transient response (time domain) for the 10-A step response. The measured transient response shows the processor voltage regulating to 70 mV, well within the 0.145-V regulation.

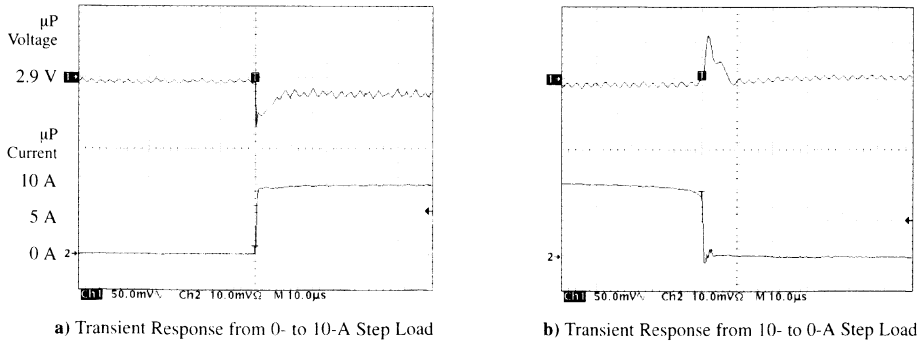
The Si9140's switching frequency is determined by the external R_{OSC} and C_{OSC} values, allowing designers to set the switching frequency of their choice. For applications where space is the main constraint, the switching frequency can be set as high as 2 MHz to minimize inductor and output capacitor size. In applications where efficiency is the main concern, the switching frequency can be set low to maximize battery life. The switching frequency for high-performance processors applications circuits are set for 400 kHz. The equation for switching frequency is:

$$f_{OSC} \approx \frac{0.75}{R_{OSC} \times C_{OSC}} \qquad (\text{at } V_{DD} = 5.0 \text{ V})$$

The precision reference is set at 1.5 V ± 1.5%. The reference is capable of sourcing up to 1 mA. The combination of 1.5% reference and 3.5% transient load regulation safely complies with the ±5% regulation requirement. If additional margin is desired, an external precision reference can be used in place of the internal 1.5-V reference.

Switching and Synchronous Rectification MOSFETs

The synchronous gate drive outputs of Si9140 PWM controller drive the high-side p-channel switch MOSFET and the low-side n-channel synchronous rectifier MOSFET. The physical difference between the non-synchronous to synchronous rectification requires an additional MOSFET across the free-wheeling diode (D1). The inductor current will reach 0 A if the peak-to-peak inductor current equals twice the output current. In synchronous rectification mode, current is allowed to flow backwards from the inductor (L1) through the synchronous MOSFET (Q3) and to the output capacitors (C3–C5) once the current reaches 0 A. Refer to schematic on Figure 1. In non-synchronous rectification, the diode (D1) prevents the current from flowing in the reverse direction. This minor difference has a drastic affect on the performance of a power supply. By allowing the current to flow in the reverse direction, it preserves the continuous inductor current mode, maintaining the wide converter bandwidth and improving efficiency. Also, maintaining the continuous current mode during light load to full load guarantees consistent transient response throughout a wide range of load conditions.



a) Transient Response from 0- to 10-A Step Load

b) Transient Response from 10- to 0-A Step Load

Figure 7.

The transition from stop clock and auto halt to active mode is a perfect example. The microprocessor current can vary from 0.5 A to 10 A or greater during these transitions. If the converter were to operate in discontinuous current mode during the stop clock and auto halt modes, the transfer function of the converter would be different compared to operation in the active mode. In discontinuous current mode, the converter bandwidth can be 10 to 15 times lower than the continuous current mode (Figure 8). Therefore, the response time will also be 10 to 15 times slower, violating the microprocessor's regulator requirements. This could result in unreliable operation of the microprocessor.

For these reasons, synchronous rectification is a must in today's microprocessors power supply design. Pulse-skipping modes are undesirable in high-performance microprocessor power supplies, especially when the minimum load current is as high as 500 mA. This pulse-skipping mode disables the synchronous rectification during light load and generates a random noise spectrum which may produce EMI problems.

Siliconix' TrenchFET™ technology has resulted in 20-mΩ n-channel (Si4410DY) and 35-mΩ p-channel (Si4435DY) MOSFETs in the SO-8 surface-mount package. These LITTLE FOOT® products totally eliminate the need for an external heatsink.

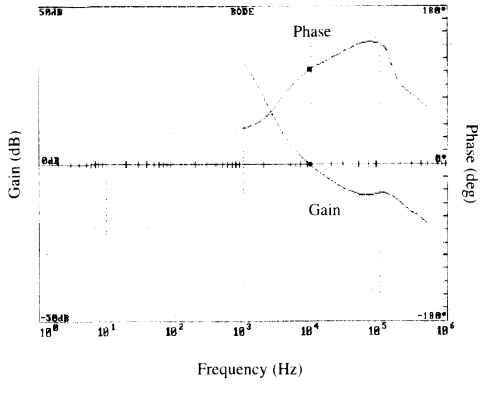


Figure 8. Non-Synchronous Converter BW

Worst case current of 10 A can be handled with two paralleled Si4435DY and two paralleled Si4410DY MOSFETs, which results in the efficiency levels shown in Figure 9.

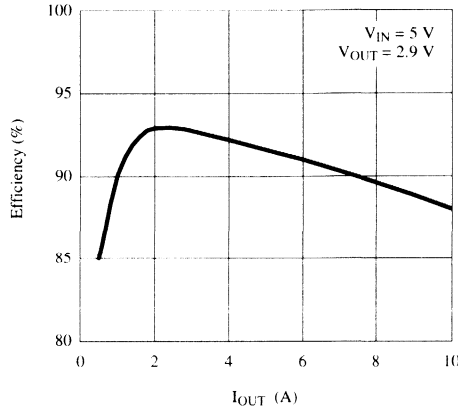


Figure 9. Efficiency

Good electrical designs must provide an adequate margin for the specification, but they should not be grossly overdesigned to lower costs. LITTLE FOOT power MOSFETs allow designers to balance cost and performance considerations without sacrificing either. If the design requires only an 8.5-A continuous current, for example, one Si4410DY can be eliminated. Table 2 shows the number of MOSFETs required to handle the various output current levels of today's high-performance microprocessors. For other output power levels, the equations below should be used to calculate the power handling capability of the MOSFET.

Table 2. Converter Requirements (Figures 1, 2, and 3)

I_O (A) Maximum	Quantity High-Side P-Channel Si4435DY	Quantity Low-Side N-Channel Si4410DY	Quantity Input (C1-C3) Capacitor Os-con 220 µF
5 A	1	1	1
8.5 A	2	1	2
10 A	2	2	2
14.5 A	3	2	3

$$P_{Dissipation\ in\ switch} = I_{RMS\ SW}^2 \times R_{SW} + \frac{Q_{SW} \times V_{IN} \times f_{OSC}}{2} + \frac{I_{PP} \times V_O \times \tau_C \times f_{OSC}}{2}$$

$$I_{RMS\ SW} = \sqrt{(I_{PEAK}^2 + I_{PP}^2 + I_{PEAK} \times I_{PP}) \times \frac{V_O}{3 \times V_{IN}}}$$

$$P_{Dissipation\ in\ synchronous\ rectification} = I_{RMS\ RECT}^2 \times R_{RECT} + \frac{Q_{RECT} \times V_{IN} \times f_{OSC}}{2}$$

$$I_{RMS\ RECT} = \sqrt{(I_{PEAK}^2 + I_{PP}^2 + I_{PEAK} \times I_{PP}) \times \frac{(V_{IN} - V_O)}{3 \times V_{IN}}}$$

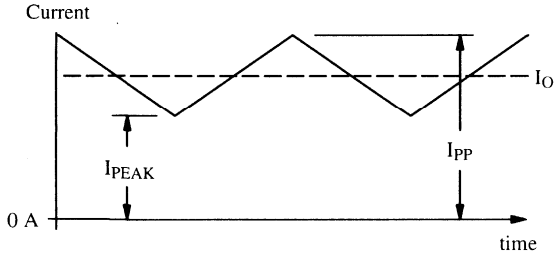
$$I_{PP} = I_{PEAK} + \Delta I$$

$$\Delta I = \frac{V_O^2}{L \times f_{OSC} \times V_{IN}}$$

$$I_{PEAK} = \frac{P_{IN} - (0.5 \times V_O \times \Delta I)}{V_O}$$

$$P_{IN} = \frac{V_O \times I_O}{\eta}$$

I_{RMSSW}	=	Switch rms current
R_{SW}	=	Switch on resistance
$I_{RMSRECT}$	=	Synchronous rectifier rms current
R_{RECT}	=	Synchronous rectifier on resistance
Q_{SW}	=	Total gate charge of switch
Q_{RECT}	=	Total gate charge of synchronous rectifier
V_{IN}	=	Input voltage
V_O	=	Output voltage
I_O	=	Output current
f_{OSC}	=	Switching frequency
η	=	efficiency
τ_C	=	Crossover time



Inductor

The size and value of the inductor are critical in meeting overall circuit dimensional requirements and in assuring proper transient voltage regulation. The size of the core is determined by the output power, the material of the core, and the operating frequency. To handle higher output power, the core must be larger. Luckily, a higher switching frequency will lower the inductance value, decreasing the core size. However, a higher switching frequency can also mean greater core loss.

In applications where the dc flux density is high and the ac flux density swing is only 100 to 200 gauss, the core loss will be negligible compared to the wire loss. Kool Mu is the best material to use at 500 kHz to deliver 30 W in the minimum volume. Ferrite has a lower core cost and loss at this frequency, but the core size is fairly large. If the power supply is designed on the motherboard and space is not a critical issue, ferrite is a better choice.

The higher switching frequency reduces the core size by decreasing the amount of energy that must be stored between switching periods. It also accelerates the transient response to the load by decreasing the inductance value. The inductance is calculated with following equation:

$$L = \frac{V_O^2}{V_{IN} \times \Delta I \times f_{OSC}}$$

ΔI = desired output current ripple. Typically ΔI = 25% of maximum output current.

Finally, the time required to ramp up the current in the inductor can be reduced with smaller inductance. A quick response from the power supply relaxes the decoupling capacitance required at the microprocessor, reducing the overall solution cost and size.

Input Capacitor

The input capacitor's function is to filter the raw power and serve as the local power source to eliminate power-up and transient surge failures. The type and characteristics of input capacitors are determined by the input power and inductance of the step-down converter. The ripple current handling requirement usually dominates the selection criteria. The capacitance required to maintain regulation will automatically be achieved once it meets the ripple current requirement. The following equation calculates the ripple current of the input capacitor:

$$I_{RIPPLE} = \sqrt{I_{RMSSW}^2 - I_{IN}^2}$$

An aluminum-electrolytic capacitor from Sanyo (OS-CON), AVX (TPS Tantalum), or Nichicon (PL series) should be used in high-power (30-W) applications to handle the ripple current. The Sanyo capacitor is smaller and handles higher ripple current than Nichicon, but at higher cost than the Nichicon product. The AVX Tantalum capacitor has the best capacitance and current handling capability per volume ratio, but it takes extra surface area compared to OS-CON or PL series. The TPS capacitors, lead time and cost have increased drastically in the recent past due to high demand, causing designers to shy away from the TPS Tantalum capacitors. Nichicon capacitors can be used to provide an economical solution if space is available or a large bulk capacitance is already present on the input line. The number of Sanyo (OS-CON) input capacitors required to handle various output currents are specified in Table 2.

Output Capacitor

To regulate the microprocessor's input voltage within 145 mV during 10-A load transients, a large output capacitance with low ESR is required. The output capacitor of the power supply and decoupling capacitors at the microprocessor must hold up the processor voltage until the power supply responds to the change. Even with fastest known switching solution, it still takes three 330-µF OS-CON capacitors to handle the load transient. If it weren't for the 10-A load transient, the output capacitor would not need a low ESR value. The fundamental output ripple current in a continuous step-down converter is much lower than the input ripple current. Maintaining voltage regulation during transients requires an ESR in the range of 30 mΩ. For microprocessors with lower transient requirements, the number of output and decoupling capacitors can be reduced. The lower transient requirements also allows greater consideration for Tantalum or Nichicon PL series capacitors.

Conclusion

The Si9140 synchronous Buck controller's ability to switch up to 1 MHz combined with a 25-MHz error amplifier provides the best solution in powering high-performance microprocessors. The high switching frequency reduces inductor size without compromising output ripple voltage. The wide converter bandwidth generated with the help of a 25-MHz error amplifier reduces the amount of decoupling capacitors required to handle the extreme transient requirement. The Si9140's synchronous fixed-frequency operation eliminates the pulse skipping mode that generates random unpredictable EMI/EMC problems in desktop and notebook computers. The synchronous rectification also allows the converter to operate in continuous current mode, independent of output load current. This preserves the wide closed-loop converter bandwidth required to meet the transient demand of the microprocessor as it transitions from stop clock and auto halt to active mode. The synchronous rectification improves the efficiency of the converter by substituting the much smaller I^2R MOSFET loss for the VI diode loss. The need for heatsinking is eliminated by using low $r_{DS(on)}$ TrenchFETs (Si4410DY and Si4435DY).

Synchronous Buck Controller for High Performance Processors

Features

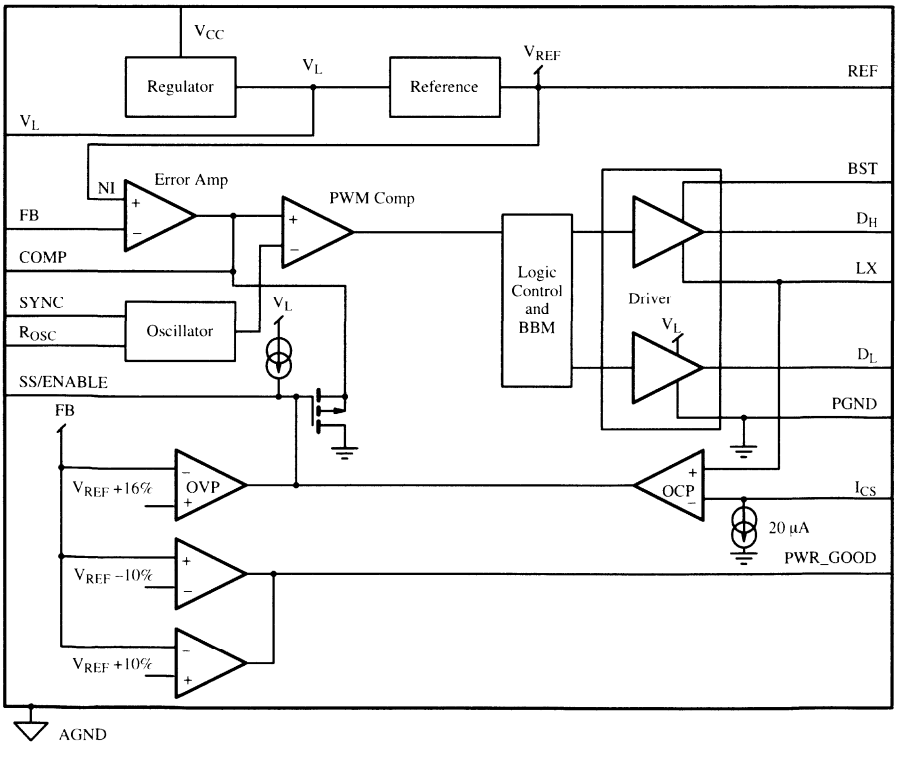
- Voltage Mode Control
- Precision 1.3-V, ± 1.6% Reference
- Drives N-Channel Switch and Rectifier
- 750-µA Quiescent Current (f_s = 200 kHz)
- 125-µA Standby Current
- Programmable Over-Current Protection
- Over-Voltage Protection
- Integrated "Power Good" Output
- Synchronization
- Under-Voltage Lockout

Description

The voltage mode, synchronous Buck controller is designed for point-of-use dc/dc conversion in high performance server and desktop computers. High efficiency is accomplished at full load by driving high- and low-side n-channel MOSFETs. The input voltage range has been designed for 4.75 V to 13.2 V to allow use of either 5 V or 12 V. The 1-MHz switching frequency combined with the 10-MHz error amplifier provides ultra-fast transient response necessary in a high performance microprocessor power supply.

Si9141 is available in a narrow-body 16-pin SOIC package and specified to operate over the commercial (0° to 70°C) temperature range.

Functional Block Diagram



This product is currently in development. Inquiries regarding the status of this product should be directed to Siliconix Marketing.

Si9142

Synchronous Buck Controller for High Performance Processors

Features

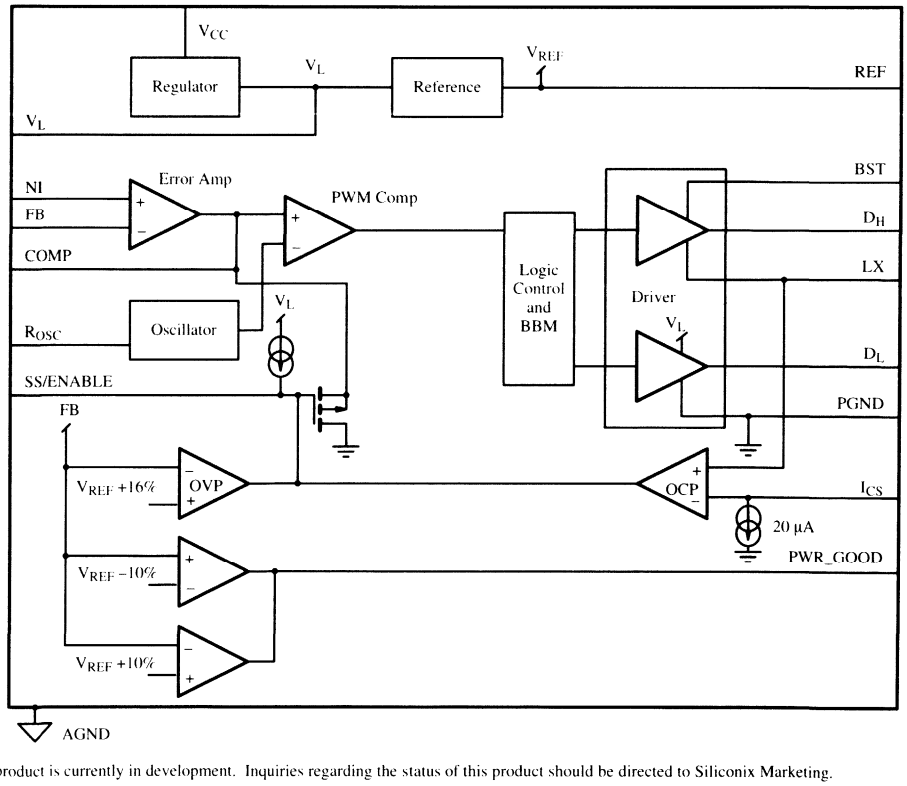
- Voltage Mode Control
- Precision 1.3-V, ± 1.6% Reference
- Drives N-Channel Switch and Rectifier
- Non-Inventing Error Amp Pin
- 750-µA Quiescent Current (f_s = 200 kHz)
- 125-µA Standby Current
- Programmable Over-Current Protection
- Over-Voltage Protection
- Integrated "Power Good" Output
- Under-Voltage Lockout

Description

The voltage mode, synchronous Buck controller is designed for point-of-use dc/dc conversion in high performance server and desktop computers. High efficiency is accomplished at full load by driving high- and low-side n channel MOSFETs. The input voltage range has been designed for 4.75 V to 13.2 V to allow use of either 5 V or 12 V. The 1-MHz switching frequency combined with the 10-MHz error amplifier provides ultra-fast transient response necessary in a high performance microprocessor power supply.

S9142 is available in a narrow-body 16-pin SOIC package and specified to operate over the commercial (0° to 70°C) temperature range.

Functional Block Diagram



This product is currently in development. Inquiries regarding the status of this product should be directed to Siliconix Marketing.

Pre-Release Information

Current Sharing Controller for High Performance Processors

Features

- Voltage Mode Control
- Precision 1.3-V, ± 1.6% Reference
- Drives N-Channel Switch and Rectifier
- 1-mA Quiescent Current (f_s = 200 kHz)
- 150-µA Standby Current
- Programmable Over-Current Protection
- Over-Voltage Protection
- Integrated "Power Good" Output
- Synchronization
- Under-Voltage Lockout
- Automatic True Current Sharing with Parallel Converters
- External High Side Gate Drive for FAULT Protection

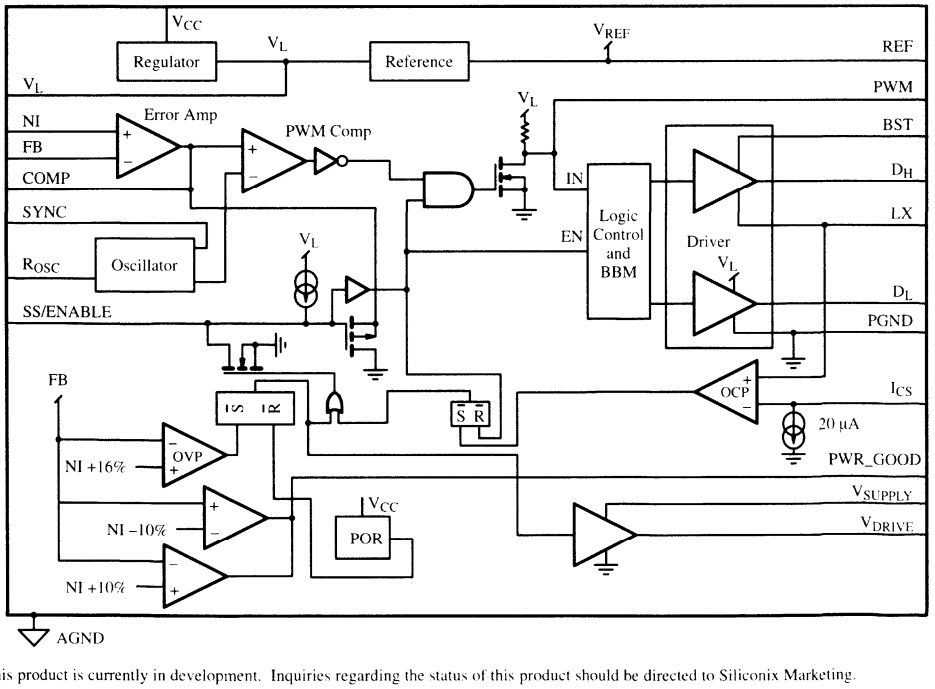
Description

The voltage mode, synchronous Buck controller is designed for point-of-use dc/dc conversion in high performance server and desktop computers. High efficiency is accomplished at full load by driving high- and low-side n-channel MOSFETs. The input voltage range has been designed for 4.75 V to 13.2 V to allow use of either 5 V or 12 V. The 1-MHz switching frequency combined with the 10-MHz error amplifier provides ultra-fast transient response necessary in a high performance microprocessor power supply.

Si9143 is designed to provide automatic true current sharing with parallel power supply. True current sharing reduces stress burdened by single supply and increases system reliability. The system reliability is further increased by short circuit protection and external gate drive signal to disconnect the power supply during fault conditions.

Si9143 is available in a wide-body 20-pin SOIC package and specified to operate over the commercial (0° to 70°C) temperature range.

Functional Block Diagram



This product is currently in development. Inquiries regarding the status of this product should be directed to Siliconix Marketing.

Low-Voltage Switchmode Controller

Features

- 2.7-V to 7-V Input Operating Range
- Voltage-Mode PWM Control
- High-Speed, Source-Sink Output Drive (200 mA)
- Internal Oscillator (up to 2 MHz)
- Standby Mode
- 0–100% Controllable Maximum Duty-Cycle

Description

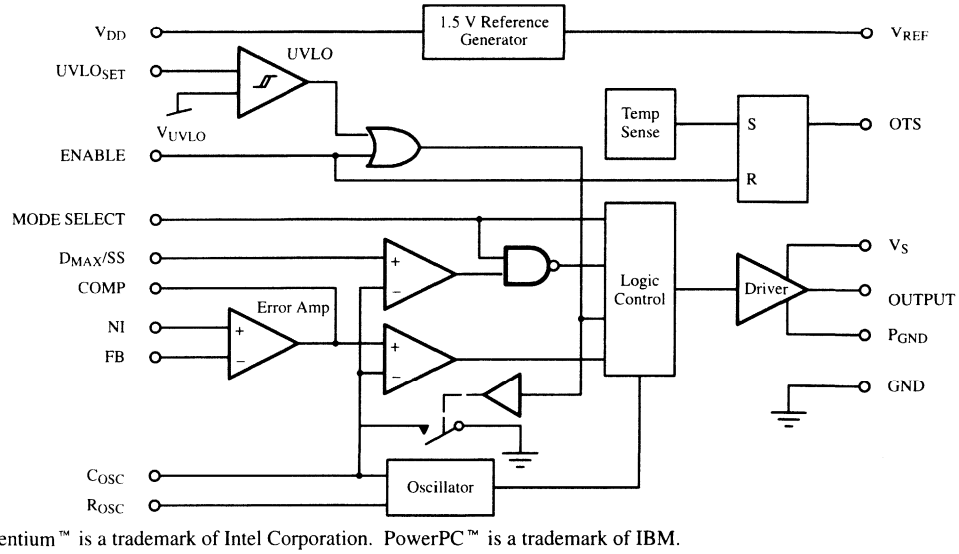
The Si9145 switchmode controller IC is ideally suited for high efficiency dc/dc converters in low input voltage systems. Operation is guaranteed down to 2.7 V, with a minimum start-up voltage of 3.0 V making the Si9145 ideal for use with NiCd, NMH, and lithium ion battery packs. A mode select pin allows the output driver polarity to be programmed allowing the device to function as a step-up or step-down converter.

Features include a precision bandgap reference, a wide bandwidth error amplifier, a 2-MHz oscillator, an input voltage monitor with standby mode and a 200-mA output driver. Supply current in normal operation is typically 1.1 mA and 250 µA in standby mode.

The Si9145 implements conventional voltage mode control. The maximum duty cycle in boost mode can be limited by voltage on D_{MAX}/SS pin. Frequency can be externally programmed by selection of R_{OSC} and C_{OSC}.

The Si9145 is available in 16-pin SOIC and TSSOP packages and is specified over the industrial temperature range (–25°C to 85°C).

Functional Block Diagram



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Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70021.

Absolute Maximum Ratings

Voltages Referenced to GND.

V_{DD}, V_S ..... 8 V
P_{GND} ..... ±0.3 V
V_{DD} to V_S ..... –0.3 V
Linear Inputs ..... –0.3 V to V_{DD} to +0.3 V
Logic Inputs ..... –0.3 V to V_{DD} to +0.3 V
Continuous Output Current ..... 100 mA
Storage Temperature ..... –65 to 125°C
Operating Junction Temperature ..... 150°C

Power Dissipation (Package)[a]
16-Pin SOIC (Y Suffix)[b] ..... 900 mW
16-Pin TSSOP (Q Suffix)[c] ..... 925 mW

Thermal Impedance (Θ_{JA})
16-Pin SOIC ..... 140°C/W
16-Pin TSSOP ..... 135°C/W

Notes
a. Device mounted with all leads soldered or welded to PC board.
b. Derate 7.2 mW/°C above 25°C.
c. Derate 7.4 mW/°C above 25°C.

Recommended Operating Range

Voltages Referenced to GND.

V_{DD} ..... 2.7 V to 7 V
V_S ..... 2.7 V to 7 V
f_{OSC} ..... 2 kHz to 2 MHz
R_{OSC} ..... 5 kΩ to 250 kΩ
C_{OSC} ..... 47 pF to 200 pF
Linear Inputs ..... 0 to V_{DD}
Digital Inputs ..... 0 to V_{DD}
V_{REF} Load Resistance ..... >150 kΩ

Specifications

Parameter	Symbol	Test Conditions Unless Otherwise Specified[a] 2.7 V ≤ V_{DD} ≤ 7 V, V_{DD} = V_S GND = P_{GND}		Limits B Suffix – 25 to 85°C Min[b]	Typ	Max[b]	Unit
Reference							
Output Voltage	V_{REF}	I_{REF} = –10 µA		1.455		1.545	V
			T_A = 25°C	1.477	1.50	1.523	
Oscillator							
Maximum Frequency[c]	f_{MAX}	V_{CC} = 3.0 V, C_{OSC} = 47 pF, R_{OSC} = 5.0 kΩ		2.0			MHz
Accuracy	f_{OSC}	V_{CC} = 3.0 V, C_{OSC} = 100 pF, R_{OSC} = 6.98 kΩ	T_A = 25°C	0.85	1.0	1.15	
R_{OSC} Voltage	V_{ROSC}				1.0		V
Minimum Start-Up Voltage	V_{DDOSC}			3.0			
50% D_{MAX}/SS	V_{DMAX} 50%	MODE SELECT = V_{DD}			1.25		
100% D_{MAX}/SS	V_{DMAX} 100%				1.54		
D_{MAX}/SS Input Current	I_{DMAX}	D_{MAX} = 0 to V_{DD}		100		100	nA
Voltage Stability[c]	Δf/f	2.7 V ≤ V_{DD} ≤ 7 V, Ref to 4.8 V	T_A = 25°C	–16		16	%
		2.7 V ≤ V_{DD} ≤ 4.2 V, Ref to 3.5 V		–8		8	
		3.8 V ≤ V_{DD} ≤ 5.6 V, Ref to 4.7 V		–7		7	
Temperature Stability[c]		Referenced to 25°C			±5		

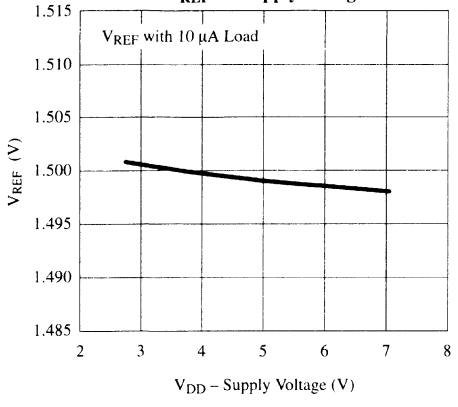
Specifications

Parameter	Symbol	Test Conditions Unless Otherwise Specified[a] 2.7 V ≤ V_{DD} ≤ 7 V, V_{DD} = V_S, GND = P_{GND}	Limits B Suffix – 25 to 85°C Min[b]	Typ	Max[b]	Unit
Error Amplifier (C_{OSC} = GND, OSC DISABLED)						
Input Bias Current	I_{FB}	V_{NI} = V_{REF}, V_{FB} = 1.0 V	–1.0		1.0	µA
Open Loop Voltage Gain	A_{VOL}		47	55		dB
Offset Voltage	V_{OS}	V_{NI} = V_{REF}	–15	0	15	mV
Unity Gain Bandwidth[c]	BW			10		MHz
Output Current	I_{EA}	Source (V_{FB} = 1 V, NI = V_{REF})		–2.0	–1.0	mA
		Sink (V_{FB} = 2 V, NI = V_{REF})	0.4	0.8		
Power Supply Rejection[c]	P_{SRR}	2.7 V < V_{DD} < 7.0 V		60		dB
$UVLO_{SET}$ Voltage Monitor						
Under Voltage Lockout	V_{UVLOHL}	$UVLO_{SET}$ High to Low	0.85	1.0	1.15	V
	V_{UVLOLH}	$UVLO_{SET}$ Low to High		1.2		
Hysterisis	V_{HYS}	V_{UVLOLH} – V_{UVLOHL}		200		mV
UVLO Input Current	I_{UVLO}	V_{UVLO} = 0 to V_{DD}	–100		100	nA
Output						
Output High Voltage	V_{OH}	V_{DD} = 2.7 V, I_{OUT} = –10 mA	2.55	2.60		V
Output Low Voltage	V_{OL}	V_{DD} = 2.7 V, I_{OUT} = 10 mA		0.06	0.15	
Peak Output Current	I_{SOURCE}	V_{DD} = 2.7 V, V_{OUT} = 0 V		–180	–130	mA
Peak Output Current	I_{SINK}	V_{DD} = 2.7 V, V_{OUT} = 2.7 V	150	200		
Logic						
ENABLE Delay to Output	td_{EN}	ENABLE Rising to OUTPUT		35		ns
ENABLE Logic Low	V_{ENL}				0.2 V_{DD}	V
ENABLE Logic High	V_{ENH}		0.8 V_{DD}			
ENABLE Input Current	I_{EN}	ENABLE = 0 to V_{DD}	–1.0		1.0	µA
MODE SELECT Logic Low	V_{MODEL}				0.2 V_{DD}	V
MODE SELECT Logic High	V_{MODEH}		0.8 V_{DD}			
MODE SELECT Input Current	I_{MODE}	MODE SELECT = 0 to V_{DD}	–1.0		1.0	µA
Over Temperature Sense						
Trip Point	T_{TRIP}			150		°C
Output Low Voltage	V_{OTSL}	V_{DD} = 2.7 V, I_{OUT} = 1 µA		0.06	0.15	V
Output High Voltage	V_{OTSH}	V_{DD} = 2.7 V, I_{OUT} = –1 µA	2.55	2.6		
Supply						
Supply Current – Normal Mode	I_{DD}	V_{DD} = 2.7 V, f_{OSC} = 1 MHz, R_{OSC} = 6.98 kΩ		1.1	1.5	mA
		V_{DD} = 7 V, f_{OSC} = 1 MHz, R_{OSC} = 6.98 kΩ		1.6	2.3	
Supply Current – Standby Mode		ENABLE = Low		250	330	µA

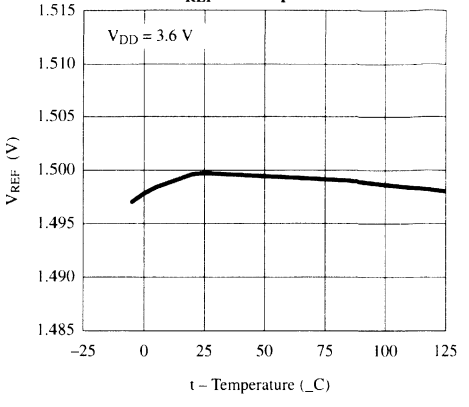
Notes
a. C_{STRAY} < 5 pF on C_{OSC}. After Start-Up, V_{DD} of ≥ 3 V.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
c. Guaranteed by design, not subject to production testing.

Typical Characteristics (25°C Unless Otherwise Noted)

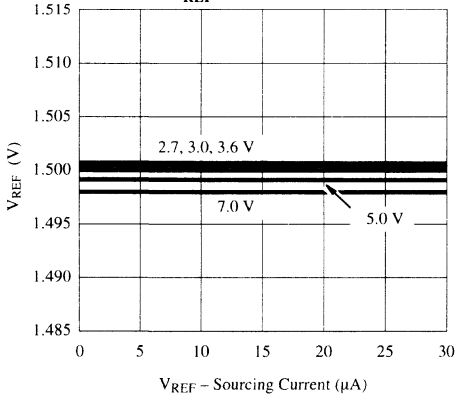
V_{REF} vs. Supply Voltage



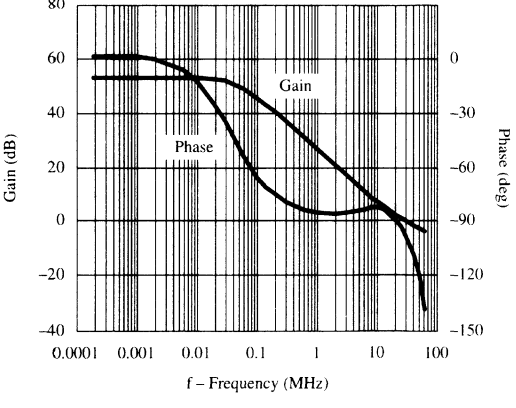
V_{REF} vs. Temperature



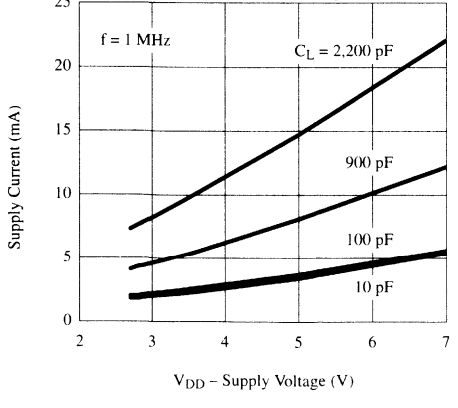
V_{REF} vs. Load Current



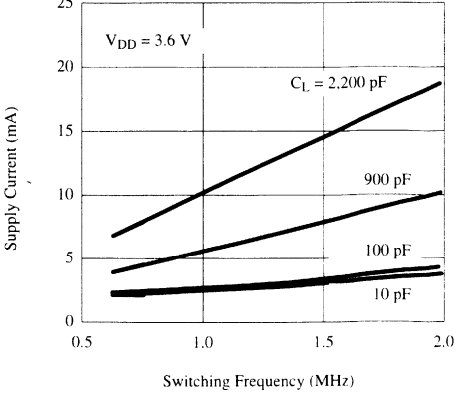
Error Amplifier Gain and Phase



Supply Current vs.Supply Voltage and Output Load

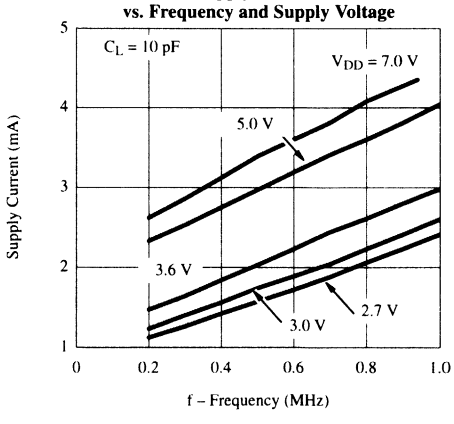


Supply Current vs. Switching Frequency and Output Load

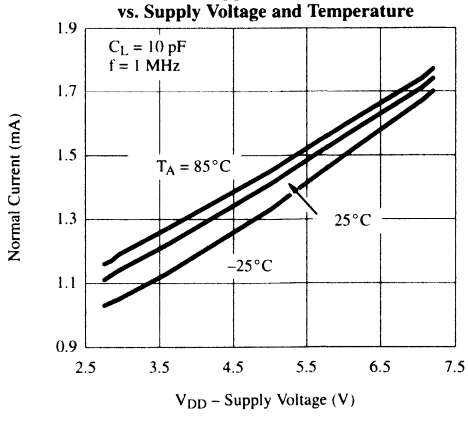


Typical Characteristics (25°C Unless Otherwise Noted)

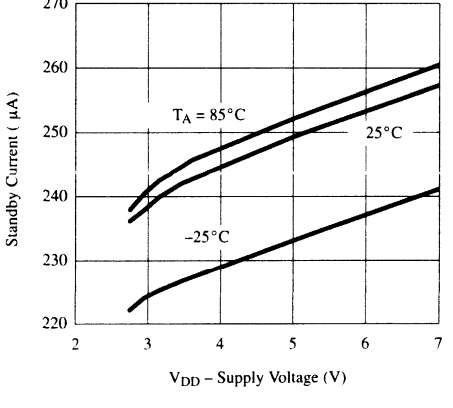
Supply Current vs. Frequency and Supply Voltage



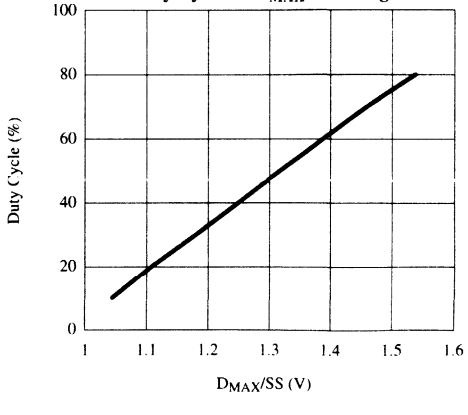
Supply Current vs. Supply Voltage and Temperature



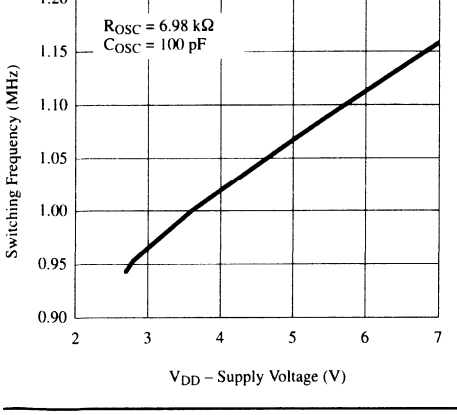
Standby Current vs. Supply Voltage and Temperature



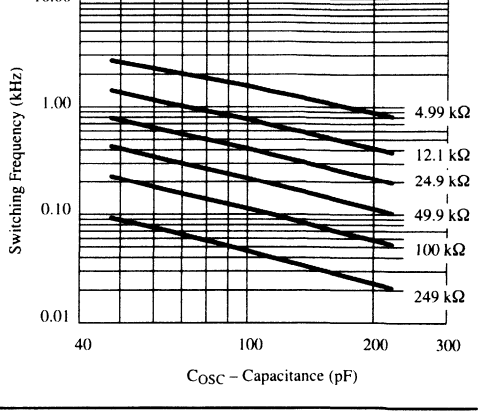
Duty Cycle vs. D_{MAX}/SS Voltage



Switching Frequency vs. Supply Voltage



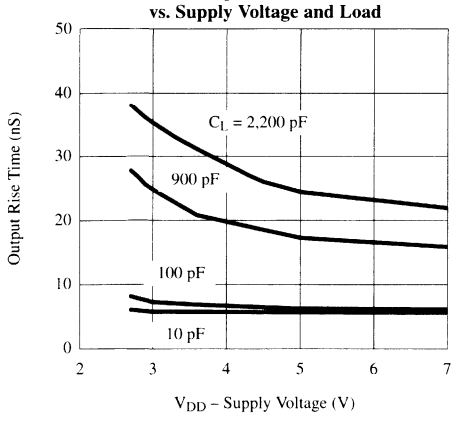
Frequency vs. R_{OSC}/C_{OSC}



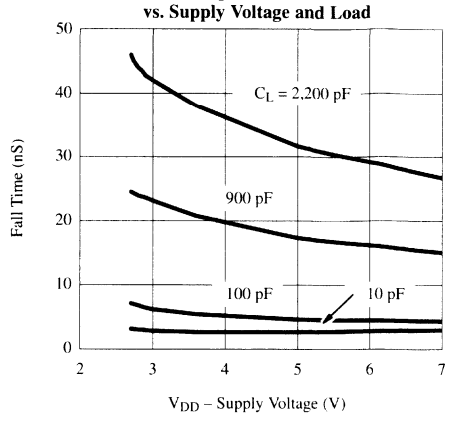
1 Power Conversion

Typical Characteristics (25°C Unless Otherwise Noted)

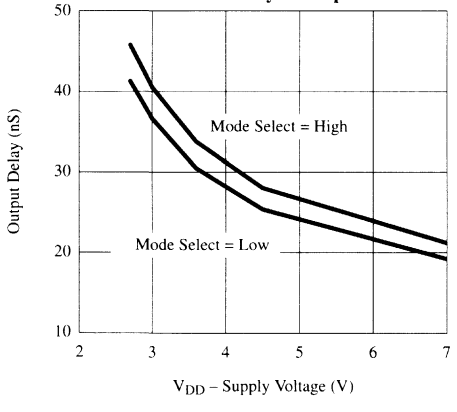
Output Rise Time vs. Supply Voltage and Load



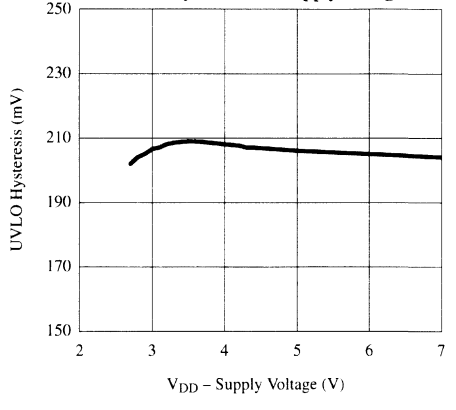
Output Fall Time vs. Supply Voltage and Load



Enable Delay to Output



UVLO Hysteresis vs. Supply Voltage



Timing Waveforms

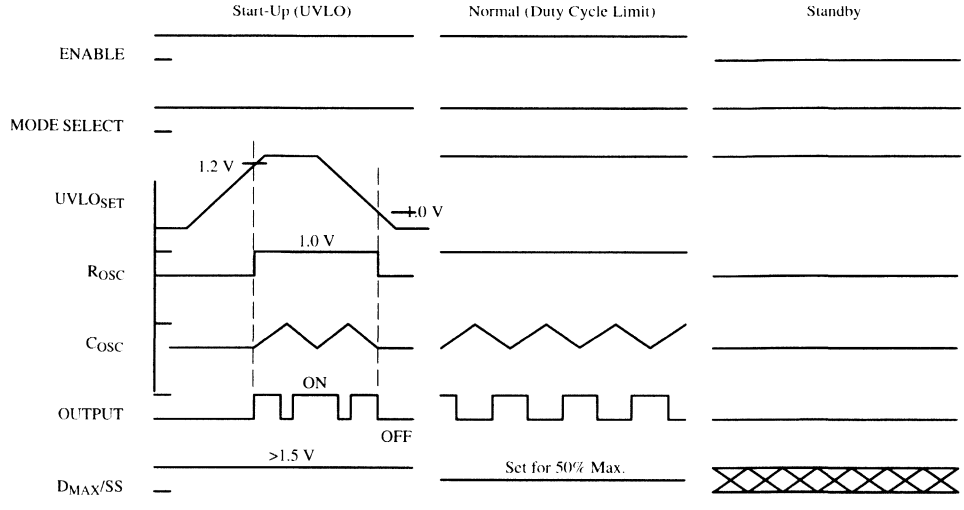


Figure 1. Si9145 Timing Diagram (MODE SELECT = High)

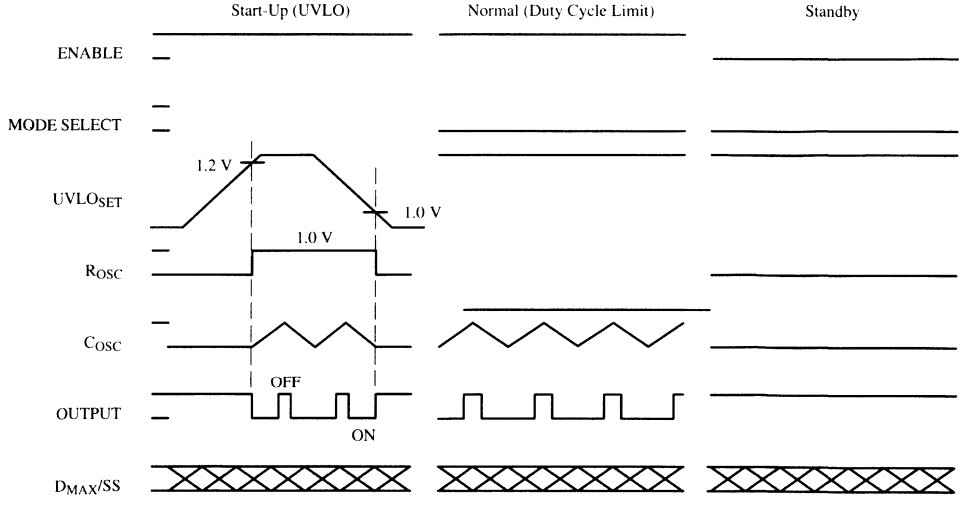
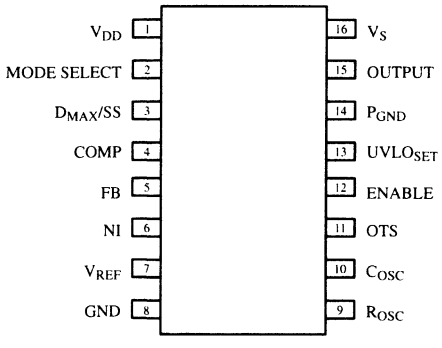


Figure 2. Si9145 Timing Diagram (MODE SELECT = Low)

Pin Configurations

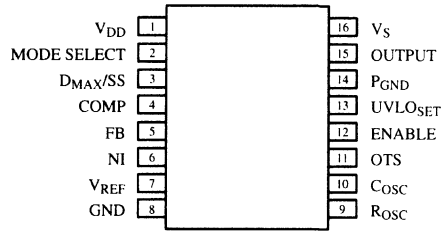
SO-16



Top View

Order Number: Si9145BY

SO-16 (TSSOP)



Top View

Order Number: Si9145BQ

Pin Description

Pin 1: V_{DD}

The positive power supply for all functional blocks except output driver. A bypass capacitor of 0.1 µF (minimum) is recommended.

Pin 2: MODE SELECT

This pin is used to enable maximum duty cycle limit and set output polarity of controller. When connected to V_{DD}, the maximum duty cycle function is controlled by the D_{MAX}/SS pin. The maximum duty cycle limit is usually used for forward, flyback, and boost converters. The output polarity is high when the PWM circuitry requires the external device to be turned on.

When connected to GND, the maximum duty cycle is not limited (usually for buck converters driving a p-channel MOS). The output polarity is low when the PWM circuitry requires the external PMOS to be turned on.

Pin 3: D_{MAX}/SS

D_{MAX}/SS pin controls the maximum duty cycle achievable by the PWM circuitry when the MODE SELECT = V_{DD}.

When D_{MAX}/SS is at less than 1.0 V (typical) the OUTPUT is held low (0% duty cycle). When D_{MAX}/SS is at more than 1.5 V (typical), the PWM circuitry can achieve 100% duty cycle. With voltage at D_{MAX}/SS between 1.0 V and 1.5 V, the maximum duty cycle is proportionally limited to this voltage.

The addition of external components can implement a soft start function.

Pin 4: COMP

This pin is the output of the error amplifier. A compensation network is connected from this pin to the FB pin to stabilize the system. This pin drives one input of the internal pulse width modulation comparator.

Pin Description (Cont'd)

Pin 5: FB

The inverting input of the error amplifier. External resistors are connected to this pin to set the regulated output voltage. The compensation network is also connected to this pin.

Pin 6: NI

The non-inverting input of the error amplifier. In normal operation it is externally connected to the V_{REF} pin.

Pin 7: V_{REF}

This pin supplies 1.5 V trimmed to ±1.5%. The reference voltage is generated by a band-gap reference.

Pin 8: GND

Negative return for V_{DD}.

Pin 9: R_{OSC}

This pin is the equivalent of a 1.0-V voltage source derived from the on-chip V_{REF}. When a low T.C. resistor is externally connected from this pin to GND, a temperature independent current is generated internally. This current is used as the charging current source connected to the C_{OSC} pin. The current is internally multiplied by 2 and is used as the discharging current source connected to the C_{OSC} pin. Therefore, the external resistor is one of the factors that determine the oscillator frequency.

Pin 10: C_{OSC}

An external capacitor is connected to this pin to set the oscillator frequency. Internal current sources alternately charge and discharge the external capacitor. The oscillator waveform is a symmetrical triangular type with a typical voltage swing between 1.0 V and 1.5 V.

$$f_{osc} \simeq \frac{0.9}{R_{OSC} * C_{OSC}}$$

Pin 11: $\overline{OTS}$

This pin indicates an over-temperature condition on the device when the output is low. The output is latched low and is reset with the ENABLE pin going low then high, or by turning power off and on.

Pin 12: ENABLE

A logic high on this pin allows normal operation. A logic low places the chip in the standby mode. In standby mode normal operation is disabled, supply current is reduced, the oscillator stops and the output is held high for MODE SELECT = low, and low for MODE SELECT = high.

Pin 13: $UVLO_{SET}$

This pin will place the chip in the standby mode if the $UVLO_{SET}$ voltage drops below 1.2 V. Once the $UVLO_{SET}$ voltage exceeds 1.2 V, the chip operates normally. There is a built-in hysteresis of 200 mV.

Pin 14: P_{GND}

The negative return for the V_S supply.

Pin 15: OUTPUT

This CMOS push-pull output pin drives the external MOSFET and is capable of sinking 150 mA or sourcing 130 mA with V_S equal to 2.7 V.

Pin 16: V_S

The positive terminal of the power supply which powers the CMOS output driver. A bypass capacitor is required.

Applications

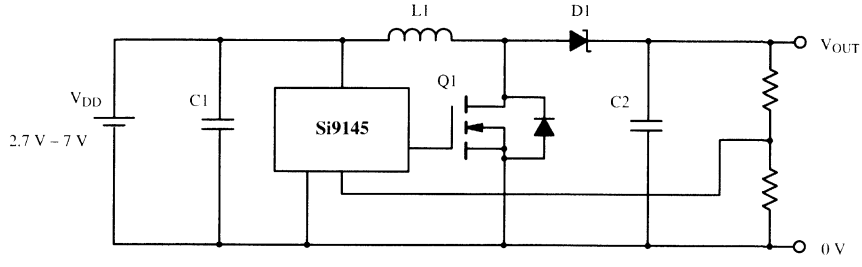


Figure 3. Non-Isolated Step Up Boost Converter for $V_{OUT} > V_{IN}$

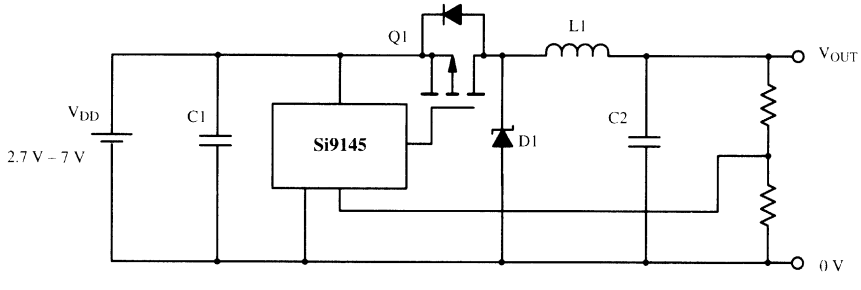


Figure 4. Non-Isolated Step Down Buck Converter for $V_{OUT} < V_{IN}$

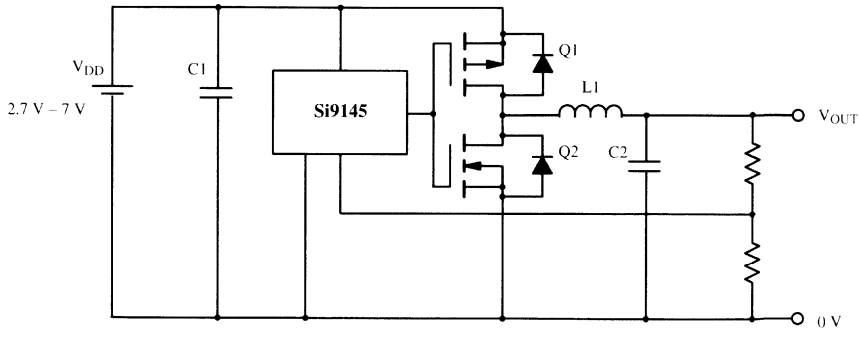


Figure 5. Non-Isolated Synchronous Buck Converter for $V_{OUT} < V_{IN}$

Designing Low-Voltage DC/DC Converters with the Si9145

Bijan E Mohandes and Chae Lee

Introduction

The Siliconix Si9145 switchmode controller IC is designed to make dc-to-dc conversion smaller and more efficient in low-voltage, low-power applications such as portable cellular phones and other battery-operated equipment. Compared with conventional bipolar and BiCMOS devices, the Si9145 offers extremely low power consumption and propagation delay times, as well as operation down to very low voltages. Built on Siliconix' proprietary BiC/DMOS technology, the Si9145 features an operating voltage range from 2.7 V to 7 V, enabling the use of single-cell lithium ion (Li+) batteries, as well as 3- to 4-cell NiCd and NiMH batteries.

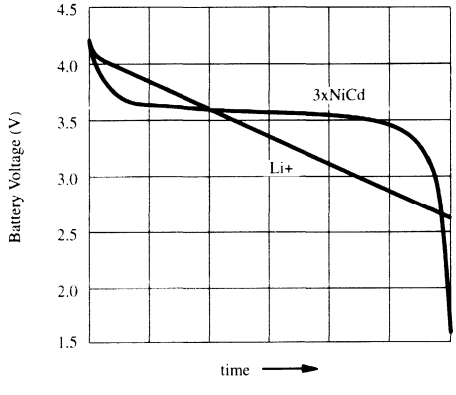


Figure 1. Discharge Comparison NiCd vs. Li+ (*)

An Overview of Lithium Ion Technology

Lithium ion batteries are becoming more readily available, and their introduction into consumer products such as camcorders and minidisk players will likely make lithium ion the technology of choice for the foreseeable future. Lithium ion batteries have several advantages over their nickel-based counterparts, including higher volumetric capacity, the absence of a memory effect, and built-in protection features supplied by the manufacturer. A single cell will produce an almost linear voltage discharge curve starting at 4 V and ending at around 2.9 V (Figure 1). The final discharge value varies by manufacturer. Compared with three NiCd batteries, however, there is a substantial voltage change over the operational platform of the battery. Presently most NiCd battery designs use a linear regulator, but with the new Li+ batteries, this would yield a substantial drop in the efficiency of the system. The Li+ battery will require a high-efficiency switchmode regulator solution to maintain all of its benefits.

Commonly Used DC/DC Topologies

There are numerous types of dc-to-dc converters, but most practical designs are variations of the Buck or boost topologies. The Si9145 has been configured so that the most popular conventional topologies, including Buck, synchronous Buck, and boost can be easily implemented.

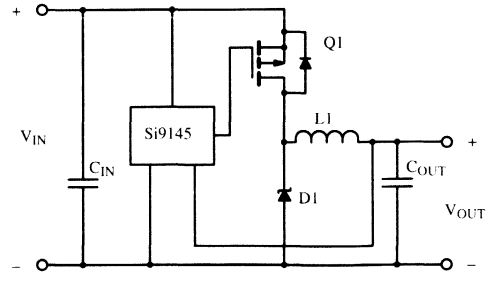


Figure 2. Buck Converter

The Buck converter (Figure 2) produces output voltages lower than the input, using a high-side switch (Q1). During the conduction time, current flows through Q1 and L1, and during the OFF time, current flows through D1 and L1, thus maintaining a continuous current.

The synchronous Buck converter (Figure 3) is identical to the Buck converter, except that a MOSFET is used to replace the rectifier. This substitution allows higher efficiencies, as well as a continuous current, even down to virtually no load.

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The Boost Converter (Figure 4) is used when a higher voltage than the input is required at the output. This result is obtained by allowing energy to be stored in L1 during the ON time of Q1 and by allowing the voltage polarity of L1 to reverse during the OFF time, thus raising the voltage above V_{IN}.

Functional Description of the Si9145

Where extremely low voltages are used and high efficiencies are required, it is not practical to measure extremely low voltages across sense resistors. Therefore, the Si9145 uses voltage mode control. The Si9145 (Figure 5) is configured for operation at high frequencies, typically between 200 kHz and 1MHz, where small energy storage components (magnetic and capacitive) are required. Operation at 1 MHz allows the use of small-outline surface-mount capacitors and inductors, which keep size and volume to a minimum.

The Si9145's pin configuration allows separation of its noisy load switching sections from its low-noise analog parts.

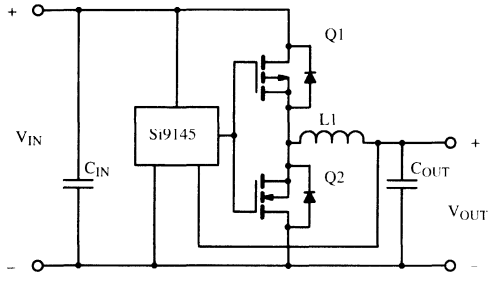


Figure 3. Synchronous Buck Regulator

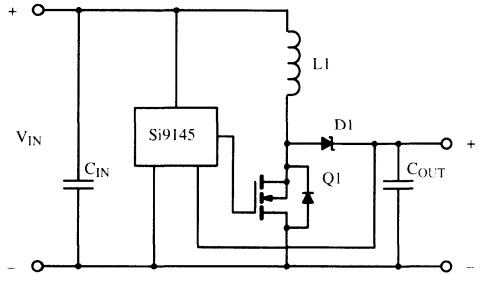


Figure 4. Boost Converter

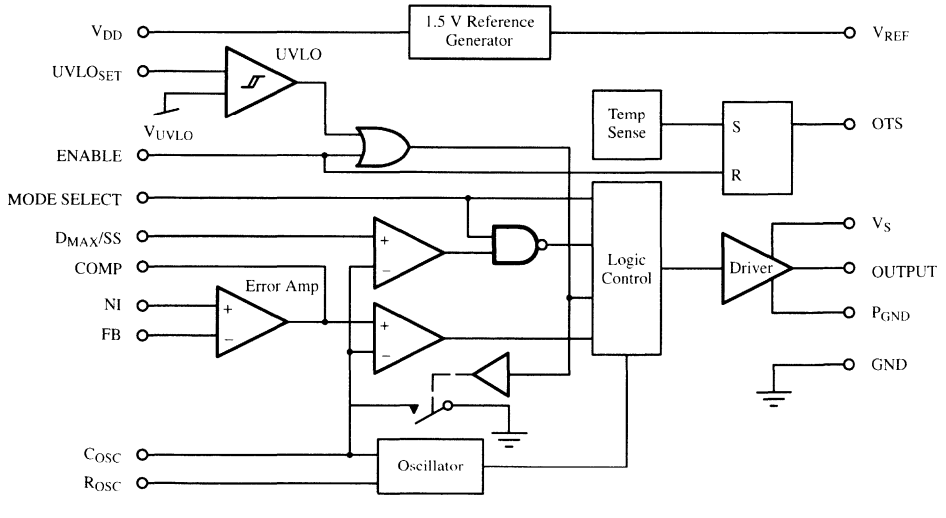


Figure 5. Si9145 Block Diagram

Pin 1: V_{DD}

This is the supply pin for the low-noise analog section. It should be well decoupled and separated from the V_S power pin. Good decoupling close to GND (pin 8) is recommended.

Pin 2: MODE Select

This pin allows the polarity of the output driver to be changed, to accommodate both n- and p-channel drives, as well as enabling the operation of the D_{MAX} pin (pin 3). When connected to GND, the D_{MAX} pin is disabled, allowing 100% duty cycle, and inverted output drive, suitable for p-channel MOSFETs, as would be the case in a Buck regulator.

When connected to V_{DD}, the duty cycle can be programmed by pin 3, and the output driver is configured for low-side drive of n-channel MOSFETs. This mode is suitable for boost regulators, and flyback/forward transformer isolated types, where duty cycle limitation prevents loop instability and core saturation.

Pin 3: D_{MAX}/SS

This pin allows the maximum duty cycle to be set between 0 and 100%. Below 1 V, the duty cycle is 0%, and above 1.5 V it is 100%. Users can program the exact value using a divider on this pin. In addition, soft start can be achieved by placing a capacitor in parallel with the lower divider in circuits where D_{MAX} is not connected to GND. This adds a time constant to the duty cycle during start-up.

Pins 4, 5, and 6: Comp, FB, and NI

These pins are the three connections to the error amplifier. The error amplifier uses a PNP bipolar input differential stage and has a complementary NPN/PNP output driver stage.

The high frequency capability of the error amp is exceptional due to the characteristics of the BCD process used. The unity gain bandwidth (Figure 6) of the error amplifier is around 20 MHz, from 3 V to 5 V.

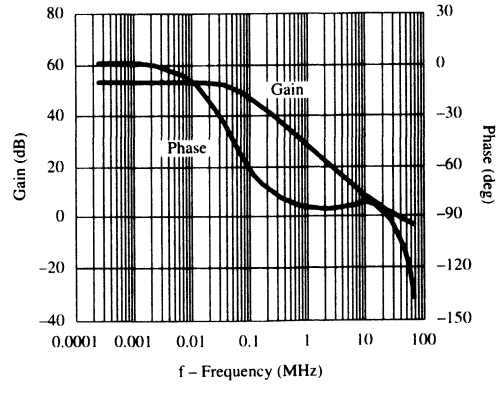


Figure 6. Si9145 Unity Gain Bandwidth and Phase

Pin 7: V_{REF}

The internal 1.5-V band gap reference is trimmed to ± 1.5% internally. A minimum 100-nF capacitor is recommended for de-coupling.

Pin 8: GND

This pin is the analog ground pin for all the noise sensitive functions (pins 1 through 7), and should be well decoupled with V_{DD}.

Pins 9 and 10: R_{OSC}, C_{OSC}

These pins are used to select the oscillator frequency of operation. The frequency of the oscillator is set by the value of the R_T resistor which sets the value of the current mirror that charges the timing capacitor C_T. It is recommended that capacitor values below 47 pF not be used, as stray capacitance and packaging manufacturing tolerance will affect the value selected. The frequency of operation can be calculated from the following equation:

$$F_{sw} = \frac{0.9}{R_t \times C_t} \quad (1)$$

This type of oscillator is difficult to synchronize. To obtain a true free running mode that can lock onto an available signal, a spike needs to be superimposed on top of the triangle ramp to pre-trigger the circuit. (Figures 7 and 8.)

Buffers 1, 2, and 3 generate a very short spike (dependent on propagation delay on the logic used) which drives Q1 on to superimpose a spike onto C_t. The spike duration should be kept to minimum, to avoid dissipating power in R1.

The oscillator frequency can be shifted to a lower value to minimize power consumption in light mode by changing the current in the timing resistor R_T with an external MOSFET (Figure 9). In normal operation Q1 is on and therefore reverse biases D1, preventing current from R1 flowing through R_T. When Q1 is open, D1 allows the mirrow current set by R_T to be altered, thus changing the frequency.

From this data (Table 1), it can be clearly seen that the improvement in efficiency at light load, for example in a sleep mode, would be significant. The current taken from $+V_{IN}$ has not changed significantly. But V_S, which drives the MOSFET and the output stage, has a significant reduction. This means that for a converter running in normal mode, the efficiency at light load may increase dramatically: from less than 50% to more than 75%, depending on other frequency losses in the circuit. The output ripple will change, as the parameters that define it have changed, but in this case the increase is acceptable.

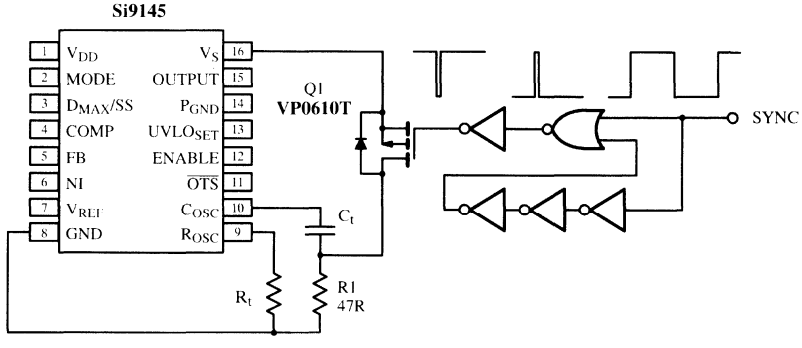


Figure 7. Synchronization to an External Source

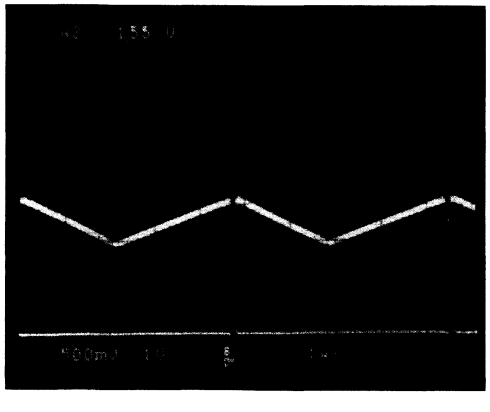


Figure 8. Oscillator Synchronization

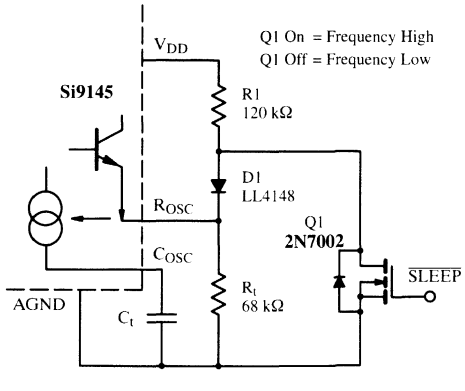


Figure 9. Frequency Shifting the Oscillator

Table 1

	F_{OSC} = 1 MHz	F_{OSC} = 150 kHz
$+V_{IN}$ Current (mA)	1.28	0.94
V_S Current (mA)	34.2	3.94
Total Current (mA)	35.48	4.88
Total Power from 5 V Input (mW)	177	24.4
Percentage of Output Power*	118	16.3
Output Ripple (mV)	35.5	43

*Taken with output power in sleep mode (35 mW).

Pin 11: $\overline{OTS}$

This pin is used to indicate an internal overtemperature shutdown. The internal integrated sensor detects excessive die temperature and latches this pin low in the event of overtemperature. Normally this pin is connected to the enable pin to allow shutdown in the event of overtemperature. Overtemperature will most likely be encountered in the event of a short circuit failure of one or both of the devices being driven from the output driver.

Pin 12: Enable

The enable pin should be pulled high in normal operation. Pulling this pin down stops operation of the chip and allows reduce consumption mode. This pin is normally configured with the $\overline{OTS}$ pin (see pin 11).

Pin 13: $UVLO_{set}$

The UVLO pin is used to determine the circuit's cut-off point of operation in the event of a low-voltage input. This function prevents excessive discharging or damage to batteries. The internal 1.2-V reference is compared with this pin, and a built in 200-mV hysteresis prevents oscillations close to the threshold of operation. This might be encountered with high-impedance sources, such as a battery at its end-of-charge.

Pins 14, 15, 16: PGND, Output, V_S

These pins are the three connections to the output driver stage, supplying the output buffer. The output buffer is a complementary MOS type, with very fast transition times and extremely low output impedance. It is also capable of generating noise in the area close to the chip. Access to pins 14, 15, and 16 allows proper decoupling and can minimize supply and return current paths to the load being driven. The output driver transition time is fast enough to drive a pair of complementary MOSFETs directly with common gate connections, while maintaining very low shoot- through current. Significant improvements in efficiency can be achieved by using an external break-before-make circuit, (see Figure 10). Using this circuit, efficiencies of better than 90% can be obtained with proper MOSFETs. It is important not to oversize the MOSFET(s) being driven for the application required. Using a larger, lower on-resistance MOSFET will not necessarily produce a better result.

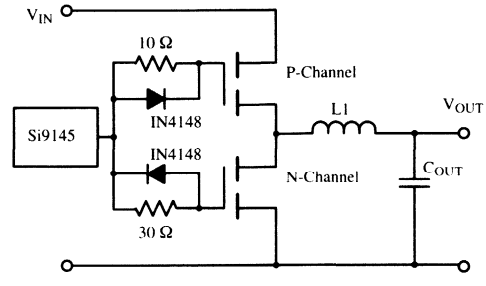


Figure 10.

The output driver of the Si9145 has been optimized for driving low on-resistance MOSFETs in the Siliconix LITTLE FOOT® series. The recently introduced LITTLE FOOT TSSOP-8 and TSOP-6 devices offer similar or better performance to the classic LITTLE FOOT SO-8 while using a smaller outline. Changes introduced in the lead connections in these packages have allowed the creation of low-voltage, low-gate threshold devices that can be used in low-profile, small-surface area power converters.

To design a highly efficient dc-to-dc converter, several parameters need to be considered:

- Required minimum efficiency. Usually 80 to 95% is achievable, with the higher efficiency occurring with the lowest switching frequency, and the lowest input to output voltage differential.
- Conduction losses caused by the current switching through the on-resistance of the MOSFETs.
- Gate drive losses caused by the turn ON and turn OFF gate charge (Qg) of both devices by the Si9145.
- Output capacitance losses caused by each MOSFET conducting and shorting out its own output capacitance.
- The input and output voltage ripple that appears on the input and output capacitors will be determined by the quality of the capacitor used. In experimental

tests, large variations were encountered from manufacturer to manufacturer and from different series. Good, low-ESR and -ESL (Equivalent Series Resistance and Inductance) devices should be selected. In boost converters, due to the discontinuous nature of energy transfer, even higher peak currents will be encountered, which will in turn generate higher ripple without lower ESR resistances.

- Board layout is critical to performance. Design methodology should include the minimization of all switching current paths as well as separated signal and power grounds, with single point connections.

The following design examples illustrate the types of converter that can be easily designed with the Si9145.

Design Example 1

5-V to 3-V @ 300 mA Buck Converter

Assume the following design specification:

V_{IN} (V) = 3 to 5 V dc

V_{OUT} (V) = 3 V dc

F_{SW} (MHz) = 1 MHz

I_{OUT} (A) = 0.3 A

P_{OUT} (W) = 0.9 W

ΔI (mA) = 30

First, select the correct inductor value: (see Appendix A and C)

L_{OUT} = 40 mH

For highest efficiency, select the synchronous Buck topology, using n- and p- channel MOSFETs. In choosing the MOSFETs, remember that the device will be driven only from rail to rail. The device selected needs to have gate thresholds specified over the input operating voltage and be suitably sized to avoid excessive power loss due to gate drive and switching losses. A small Schottky diode D1 is used to prevent current flow through the body diode of the n-channel MOSFET and to avoid recovery time through this device. D1 only conducts current during the crossover time. It therefore dissipates virtually no power, as the n-channel device shunts D1 when it is fully enhanced.

For the synchronous Buck regulator, the conduction duty cycles of the n- and p-channel devices are:

$$\delta_{Pchannel} = \frac{V_{OUT}}{V_{IN}} \quad (2)$$

and

$$\delta_{Nchannel} = \frac{V_{IN} - V_{OUT}}{V_{IN}} \quad (3)$$

For conduction losses in the worst possible case, the temperature coefficient of a MOSFET operating at 100°C will be approximately 1.4. The required on-resistance, based on power dissipated for each device will approximately be:

$$r_{DS(on)P} = \frac{V_{IN} \times P_{LOSS}}{V_{OUT} \times I_{MAX}^2 \times 1.4} \quad (4)$$

and for the n-channel device,

$$r_{DS(on)N} = \frac{V_{IN} \times P_{LOSS}}{(V_{IN} - V_{OUT}) \times I_{MAX}^2 \times 1.4} \quad (5)$$

Assuming that the conduction power losses of each MOSFET will be equal to 25% of the total losses at full load, then the losses of each device for an 85% efficient converter will be:

$$P_O = V_{OUT} \times I_{OUT} = (3\ V)(0.3\ A) = 0.9\ W$$

$$P_{IN} = \frac{P_O}{\eta} = \frac{0.9\ W}{0.85} = 1.06\ W$$

$$P_D = P_{IN} - P_O = 1.06\ W - 0.9 = 0.16\ W$$

$$P_{LOSS} = (0.25)(0.16\ W) = 0.04\ W$$

Then the on-resistance of each of the MOSFETs will need to be:

$$r_{DS(on)P} = \frac{V_{IN} \times P_{LOSS}}{V_{OUT} \times I_{MAX}^2 \times 1.4} \quad (6)$$

$$= \frac{5\ V \times 40\ mW}{3\ V \times (0.3\ A)^2 \times 1.4}$$

$$= 0.529\ \Omega$$

and for the n-channel device

$$r_{DS(on)P} = \frac{V_{IN} \times P_{LOSS}}{(V_{IN} - V_{OUT}) \times I_{MAX}^2 \times 1.4} \quad (7)$$

$$= \frac{5\ V \times 40\ mW}{(5\ V - 3\ V) \times (0.3\ A)^2 \times 1.4}$$

$$= 0.794\ \Omega$$

The total gate charge losses of the MOSFET need also to be considered. If the gate charge losses of both devices were equal to half of the full load conduction losses, then these would be approximately 20 mW. The required gate charges would be determined from:

$$P_{QGTOT} = V_{IN} \times I_{QGTOT} \quad (8)$$

$$= V_{IN} \times F_{OSC}(Qg_P + Qg_N)$$

then

$$(Qg_P + Qg_N) = \frac{P_{QGTOT}}{V_{IN} \times F_{OSC}} = \frac{20\ mW}{5\ V \times 1\ MHz} = 4\ nC$$

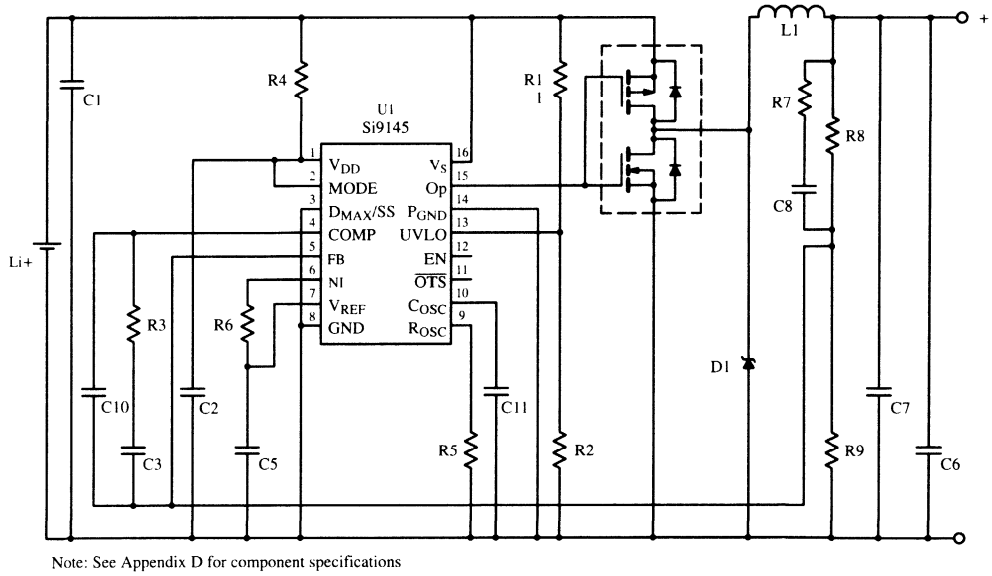
Ideally, n- and p-channel devices with 2 nC each should be selected.

A complete schematic of a 5-V to 3-V converter is shown in Figure 11. In this circuit example, the Si9145's power consumption was measured at 974 µA.

Loop Stability

To optimize the stability of the loop, the POWER456[2] software was utilized.

The data parameters for the Buck converter stage were entered and the resulting loop compensation components were extracted. For a manual detailed analysis of voltage mode loop stability should review Siliconix application note AN710[3].



Note: See Appendix D for component specifications

Figure 11. Complete Buck Regulator Schematic

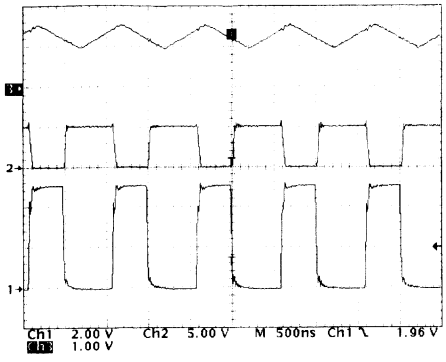


Figure 12. Synchronous Buck Switching Waveforms

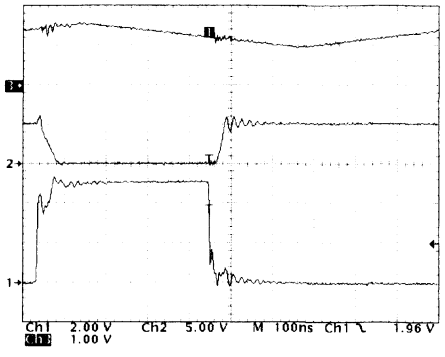


Figure 13. Synchronous Buck Switching Waveforms (Expanded)

Figure 12 shows the converter switching waveforms. The middle trace shows the input voltage node to the choke, which is also the common drain of both MOSFETs. The bottom trace shows the common gate connection of both MOSFET.

Figure 13 shows the same waveforms but greatly expanded, showing the rise and fall times of the output driver. The effect of noise is clearly apparent on the timing capacitor waveform.

Design Example 2

3-V to 6-V @ 500 mA Continuous Boost Converter

Assume the following Design specification:

V_{IN} (V) = 3 to 5 V dc

V_{OUT} (V) = 6 V dc

F_{SW} (MHz) = 1 MHz

I_{OUT} (A) = 0.1 to 0.5 A

P_{OUT} (W) = 0.6 to 3.0 W

Target Efficiency (η%) = 88%

First , select the correct inductor value (see Appendix B and C):

Ipeak = 1.296 A equivalent to Irms = 0.842 A

L = 4.7 µH

Assume that the MOSFET conduction losses will represent 40% of the total losses and that the V_{D1} of the Schottky diode is 0.3 V.

Total losses:

$$P_T = \frac{P_{OUT(MAX)}}{\eta} - P_{OUT(MAX)}$$

$$= \frac{3.0\ W}{0.88} - 3.0\ W = 0.409\ W$$

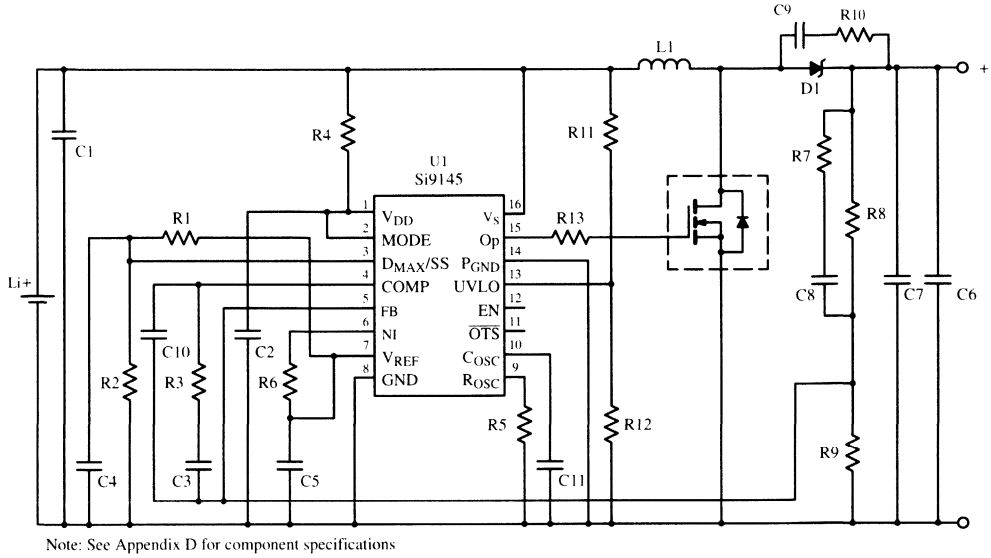
The power dissipated by the MOSFET will be:

$$P_{LOSS} = I^2_{RMS} \times r_{DS(on)} \qquad (9)$$

Therefore, the MOSFET will need to have an on-resistance of:

$$r_{DS(on)} = \frac{P_{LOSS}}{I^2_{RMS}} = \frac{0.164\ W}{(0.842\ A)^2} = 0.231\ \Omega \qquad (10)$$

Allowing for worst case heating effect, a factor of 1.4 must be added to obtain a data sheet specification of 231/1.4 = 165 mΩ. It is important to remember that this value needs to be specified for operation with the input voltage to the Si9145, as this is the only source for the gate drive. In this case, it would be advisable to select a device with this on-resistance rated at 2.7 V V_{GS} to allow for other losses in series (such as output stage and tracking losses).



Note: See Appendix D for component specifications

Figure 14. Complete Boost Regulator Schematic

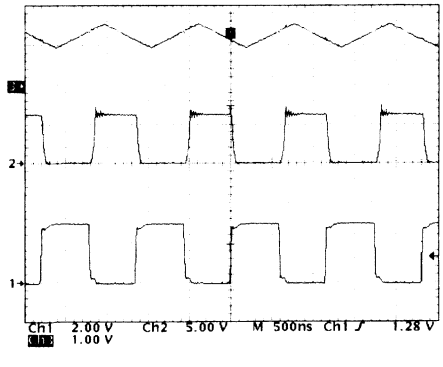


Figure 15. Boost Switching Waveforms

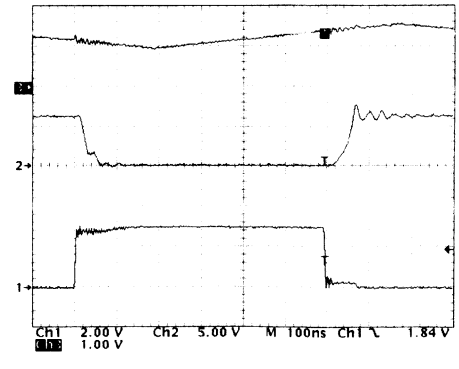


Figure 16. Boost Switching Waveforms (Expanded)

The gate charge losses should also be considered. In the case of the boost converter, the drain of the MOSFET is switched to the same voltage as the output (ignoring diode voltage drop). If the gate charge losses of the MOSFET were equal to half of the full load conduction losses, then these would be approximately 82 mW.

The required gate charge would be determined from:

$$Q_{gN} = \frac{P_{QG}}{V_{IN} \times F_{OSC}} = \frac{82\ mW}{(5\ V) \times 1\ MHz} = 16\ nC \qquad (11)$$

Ideally, an n-channel device with less than 16 nC gate charge should be selected. A complete schematic of a 3-V to 6-V converter is shown in Figure 14. The waveforms in Figure 15 and Figure 16 show typical results obtained.

References

1. Mohandes, Bijan. 1993. "Designing High Frequency DC-to-DC Converters with the Si9114." Siliconix Application Note.

2. Riddley, Ray. 1992. POWER 456 - Power Supply Simulation Software. [Riddley Engineering, 152 Jacaranda Drive, Battle Creek, Michigan 49017]

Tel:+1-616-962-1181, Fax:+1-616-962-1180.

3. Blattner, Robert. 1992. "High Efficiency Buck Converter for Notebook Computers." Siliconix Application Note AN710.

4. McLymann, Colonel Wm. "Designing Magnetic Components for High Frequency dc-dc Converters", Kg Magnetics, ISBN #1-883107-00-8

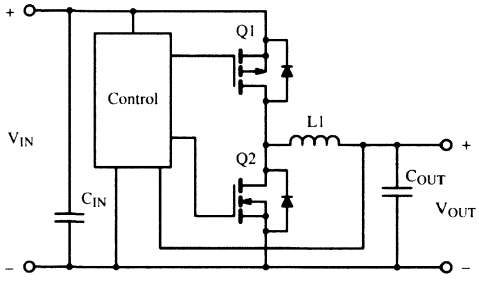
5.Coilcraft , Cary, Illinois, IL60013, USA,

In USA: Tel:+1-708-639-6400, Fax:+1-708-639-1469

In Europe: Tel:+44-236-730595, Fax:+44-236-730627

In Hong Kong: Tel:+852-770-9428, Fax:+852-770-0729

Appendix A: Buck Converter Inductor Design



Specification requirements:

Input Voltage (V_{IN}) = 3 V_{MIN}, 4 V_{MAX} dc

Output Voltage (V_{OUT})= 3 V dc

Switching Frequency (F_{SW}) = 1 MHz

Output Current (I_{OUT}) = 300 mA

Ripple Current (DI_{OUT}) = 30 mA pk-pk

Ripple Voltage (DV_{OUT}) = 30 mV pk-pk

From basic electrical circuit theory, the voltage across an inductor is given by:

$$V_L = L \times \frac{di}{dt}$$

where V_L is the voltage across the inductor.

At maximum input voltage the voltage across the inductor is:

$V_L = V_{IN} - V_{OUT}$ and $di = \Delta I_L$

Therefore

$$L = \frac{(V_{IN} - V_{OUT}) \times T_{ON}}{\Delta I_L}$$

Assuming that the Q1 and Q2 are ideal components, then at maximum input voltage the duty cycle will be:

$$\delta_{MIN} = \frac{V_{OUT}}{V_{IN}}$$

In this case,

$$\delta_{MIN} = \frac{V_{OUT}}{V_{IN}} = \frac{3\ V}{5\ V} = 0.6$$

Therefore,

$$T_{ON} = \frac{\delta_{MIN}}{F_{SW}} = \frac{0.6}{1\ MHz} = 0.6\ \mu s$$

Then

$$L = \frac{(V_{IN} - V_{OUT}) \times T_{ON}}{DI_{OUT}}$$

$$L = \frac{(5\ V - 3\ V) \times 0.6\ \mu s}{30\ mA} = 40\ \mu H$$

The value of the capacitor required for the output ripple needs to be:

$$C_{OUT} = \frac{\Delta I_{OUT}}{8 \times F_{SW} \times \Delta V_{OUT}}$$

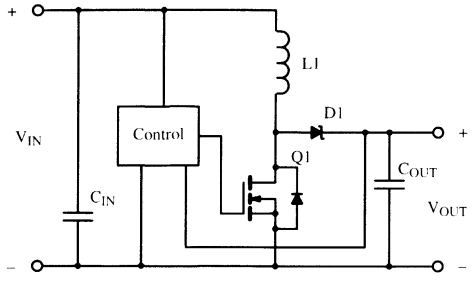
$$C_{OUT} = \frac{30\ mA}{8 \times 1\ MHz \times 30\ mV} = 0.125\ \mu F$$

To ensure that the ripple voltage is not exceeded, the ESR (Equivalent Series Resistance of the capacitor) needs to be less than:

$$ESR_{MAX} = \frac{\Delta V_{OUT}}{\Delta I_{OUT}} = \frac{30\ mV}{30\ mA} = 1\ \Omega$$

In practice, other factors such as ESL will also have an effect on the output ripple, as well as noise, and capacitors in the 1- to 10-µF range are more practical.

Appendix B: Continuous Boost Converter Inductor Design



Specification requirements and design example:

Input Voltage (V_{IN}) = 3 V_{MIN}, 5 V_{MAX} dc

Output Voltage (V_{OUT})= 6 V dc

Switching Frequency (F_{SW}) = 1 MHz

Output Current (I_{OUT}) = 100 to 500 mA

Ripple Voltage (DV_{OUT}) = 60 mV (usually 10% of V_{OUT})

Target efficiency (η%) = 88%

First calculate the period of operation:

$$T = \frac{1}{F_{SW}} = \frac{1}{1\ MHz} = 1\ \mu s$$

Next calculate the minimum and maximum output power:

$$P_{OUT(MIN)} = V_{OUT} \times I_{OUT(MIN)} = 6\ V \times 0.1\ A = 0.6\ W$$

$$P_{OUT(MAX)} = V_{OUT} \times I_{OUT(MAX)} = 6\ V \times 0.5\ A = 3.0\ W$$

Now calculate the maximum input current:

$$I_{IN(max)} = \frac{P_{OUT(MAX)}}{V_{IN(min)} \times \eta} = \frac{3.0\ W}{3\ V \times 0.88} = 1.136\ A$$

Calculate the minimum and maximum duty cycle:

$$\delta_{MIN} = \frac{V_{OUT} + V_{D1} - V_{IN(MAX)}}{V_{OUT} + V_{D1} - V_{DSQ1}} = \frac{6\ V + 0.3\ V - 5.0\ V}{6\ V + 0.3\ V - 0.25\ V} = 0.215$$

$$\delta_{MIN} = \frac{V_{OUT} + V_{D1} - V_{IN(MIN)}}{V_{OUT} + V_{D1} - V_{DSQ1}} = \frac{6\ V + 0.3\ V - 3.0\ V}{6\ V + 0.3\ V - 0.25\ V} = 0.545$$

Now calculate the minimum and maximum load resistance:

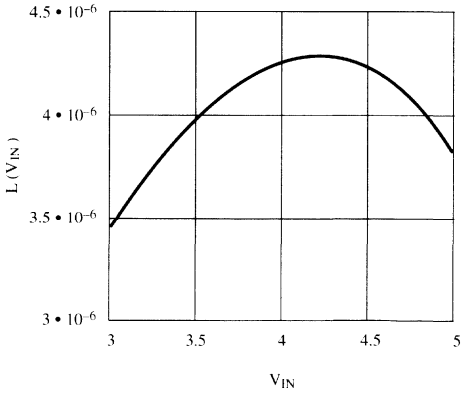
$$R_{MIN} = \frac{V_{OUT}}{I_{OUT(MAX)}} = \frac{6\ V}{0.5\ A} = 12\ \Omega$$

$$R_{MAX} = \frac{V_{OUT}}{I_{OUT(MIN)}} = \frac{6\ V}{0.1\ A} = 60\ \Omega$$

The minimum required inductance can now be calculated:

$$L \geq \frac{V_{IN}^2 \times \delta \times T \times \eta}{2 \times P_{OMIN}}$$

From the equation above, minimum inductance required to maintain continuous inductor current is a function of input voltage. Inductance versus input voltage is plotted in the graph below.



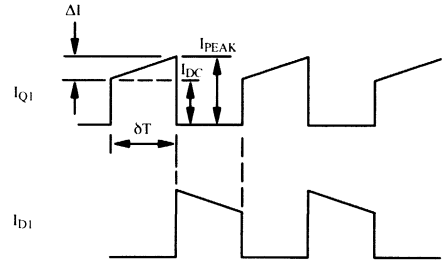
From the graph above, one can clearly see that the minimum inductance required to operate in continuous conduction mode throughout the entire input voltage range must be greater than 4.3 µH. An inductance value greater than 4.3 µH should be used to provide additional margin, 4.7 µH will be used in this example.

L = 4.7 µH

The peak current can now be determined under the worst case condition during minimum input voltage with maximum load.

$$\Delta I = \frac{(V_{IN(MIN)} - V_{DSQ1}) \times \delta_{MAX} \times T}{L}$$

$$= \frac{(3.0\ V - 0.25\ V) \times 0.545 \times 1\ \mu s}{4.7\ \mu H} = 0.319\ A$$



$I_{IN(MAX)} = I_{DC} + 0.5 \times \Delta I$

$I_{DC} = I_{IN(MAX)} - 0.5 \times \Delta I$

$I_{DC} = 1.136\ A - 0.5 \times 0.319\ A$

$I_{DC} = 0.977\ A$

$I_{PEAK} = I_{DC} + \Delta I$

$I_{PEAK} = 0.977\ A + 0.319\ A$

$I_{PEAK} = 1.296\ A$

From this, the RMS current can be calculated:

$$I_{RMS} = \sqrt{(I_{PEAK}^2 + I_{PEAK} \times I_{DC} + I_{DC}^2) \times \frac{\delta_{MAX}}{3}}$$

$$I_{RMS} = \sqrt{(1.296A^2 + 1.296A \times 0.977A^2) \times \frac{0.545}{3}}$$

$I_{RMS} = 0.842\ A$

Output capacitance and ESR (equivalent series resistance) calculation:

Boost converter's output ripple voltage is determined by the output capacitance and ESR. Equal contribution of ripple voltage from capacitance and ESR will be assumed for this example.

$$C_{OUT} = \frac{I_{OUT} \times \delta_{MAX} \times T}{DV_{OUT}}$$

$$= \frac{(0.5\ A)(0.545)(1\ \mu sec)}{0.03\ V} = 9.091\ \mu F$$

$$ESR_{MAX} = \frac{DV_{OUT}}{I_{PEAK}} = \frac{30\ mV}{1.296\ A} = 0.023\ \Omega$$

To minimize the ESR effects, ceramic capacitors should be used.

Appendix C: Standard Inductor Selection*

Buck and boost inductors used in the design examples in this literature were selected from the Coilcraft "Surface-Mount Products" catalog. These devices are suggested for the benefit of designers. For further information contact Coilcraft.

Part Number	L at I_{DC} = 0 A (µH)	L at I_{DC} (µH)	IDC_{MAX} (mA)	DCR (mΩ)
DT3316-102	1.0	0.5	5.0	25
DT3316-152	1.5	0.7	5.0	30
DT3316-222	2.2	1.0	5.0	35
DT3316-332	3.3	1.5	5.0	40
DT3316-472	4.7	2.0	3.0	45
DT3316-682	6.8	4.0	2.5	50
DT3316-103	10	5.0	2.0	55
DT3316-153	15	6.0	1.8	60
DT3316-223	22	10	1.5	84
DT3316-333	33	12	1.3	90
DT3316-473	47	27	1.0	110
DT3316-683	68	40	0.9	150
DT3316-104	100	50	0.8	290
DT3316-154	150	80	0.6	360
DT3316-224	220	90	0.5	390
DT3316-334	330	150	0.4	730
DT3316-474	470	200	0.35	880
DT3316-684	680	300	0.3	1150
DT3316-105	1000	420	0.25	1450
DT1608-102	1.0	0.5	5.0	45
DT1608-152	1.5	0.7	5.0	50
DT1608-222	2.2	1.0	5.0	60
DT1608-332	3.3	1.5	5.0	70
DT1608-472	4.7	2.0	3.0	80
DT1608-682	6.8	4.0	2.5	85
DT1608-103	10	5.0	2.0	95
DT1608-153	15	6.0	1.8	135
DT1608-223	22	10	1.5	160
DT1608-333	33	12	1.3	275
DT1608-473	47	27	1.0	340
DT1608-683	68	40	0.9	575
DT1608-104	100	50	0.8	1100
DT1608-154	150	80	0.6	1400
DT1608-224	220	90	0.5	2250
DT1608-334	330	150	0.4	2900
DT1608-474	470	200	0.35	3600
DT1608-684	680	300	0.3	4550
DT1608-105	1000	420	0.25	8100

* This data is supplied for information purposes only. Siliconix does not recommend or endorse suppliers of components. Designers must determine the suitability of the data and the supplier for use in their applications.

Appendix D:
Figure 10 and Figure 14 Component Specifications

Figure 10: Synchronous Buck Converter	
C1	2.2 µF, 10 V
C2	0.1 µF
C3	0.01 µF
C4	N/A
C5	0.1 µF
C6	2.2 µF, 10 V
C7	100 nF
C8	2200 pF
C9	N/A
C10	N/A
C11	100 pF
R1	N/A
R2	N/A
R3	3.32 k
R4	100 R
R5	9.09 k, ± 1%
R6	N/A
R7	221 R
R8	6.81 k
R9	6.81 k
R10	N/A
R11	10 k
R12	10 k
L1	4.7 µH
D1	DISC 4

Figure 14: Boost Converter	
C1	47 µF, 10 V
C2	10 nF
C3	22 nF
C4	1 nF
C5	100 nF
C6	10 µF, 25 V
C7	100 nF
C8	1800 pF
C9	(Optional)
C10	10 pF
C11	100 pF
R1	1 k
R2	10 k
R3	511 R
R4	100 R
R5	9.09 k, ± 1%
R6	1 k
R7	1 k
R8	10 k
R9	3.3 k
R10	10 R (Optional)
R11	10 k
R12	10 k
R13	15 R
L1	4.7 µH
D1	DISC 4

Powering the Pentium™ VRE with the Si9145 Voltage Mode Controlled PWM Converter

Chae K. Lee and Richard Williams

Benefits

- First and only Intel-approved switching converter solution to provide static and dynamic voltage regulation for the Pentium VRE microprocessor.
- Low cost
- Efficiency greater than 89% at 7 A
- Eliminates the need for heat sinks
- Supplies maximum currents required by P54C
- High operating frequency (recommended 375 kHz) allows use of the smallest possible inductors and capacitors, resulting in lowest voltage ripple and best transient response
- Easily adjustable output voltage to meet the different specs of P54C family.
- PCB layout available
- Available in SO-16 surface-mount package

A Proven Solution for the Pentium™ Converter

Siliconix has developed the first and only Intel-approved switching power supply solution for the Pentium VRE microprocessor. Built on a leading-edge CBiC/D process, the Si9145BY is the only voltage- mode controlled PWM IC capable of switching up to 2 MHz and providing a 25-MHz error amplifier. For the first time, a 100-kHz closed-loop bandwidth switching converter can be designed to meet the dynamic transient requirements of the Pentium microprocessor, without adding numerous output capacitors.

The Si9145BY consistently satisfies Pentium VRE voltage regulation limits within generous margins. Worst-case assumptions for voltage regulation, as provided by Intel, are displayed in Figure 2.

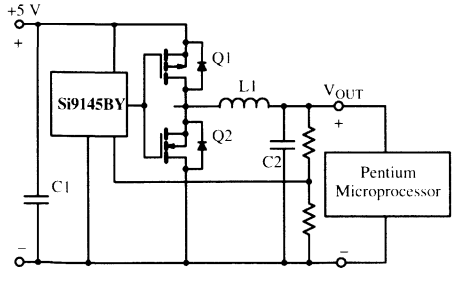


Figure 1. Typical Application Circuit

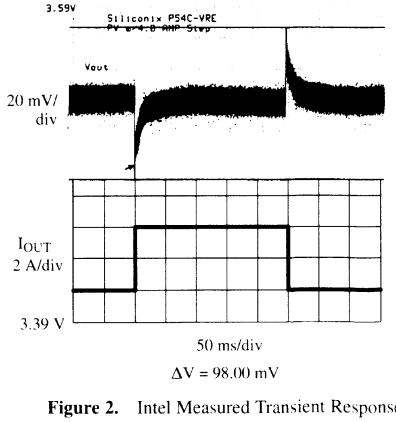


Figure 2. Intel Measured Transient Response

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Regulation Requirements for the VRE Pentium Converter

The Pentium VRE microprocessor has been designed to operate faster and more efficiently than any of its predecessors. To save power, a CPU clock has been implemented with start/stop features, requiring an ultra-fast response from the power supply. To obtain higher clock speeds and to enhance manufacturing yields, the Pentium requires specific output voltage levels with tight voltage regulations (Figure 3). Within this stringent voltage regulation limit, no overshoot or undershoot are permitted to exceed the regulation limit, irrespective of their duration. Not surprisingly, these new demands have overwhelmed the capabilities of existing power supply designs based on conventional PWM ICs.

Meeting the tight static and transient regulation demands of the Pentium VRE microprocessor requires a certain amount of decoupling capacitance both at the processor and at the output of the power supply. Obviously, the greater the decoupling capacitance, the easier it is to meet the transient regulation. Since cost and space limit the amount of capacitance one can use, Intel has recommended the use of six 100-µF low-ESR tantalum capacitors and twenty-five 1-µF ceramic capacitors.

The amount of output capacitance at the output of the converter also determines the transient response of a converter. The greater the output capacitance, the less converter bandwidth is required to meet the transient regulation. A 4-A transient response has been simulated using a SPICE program for various output capacitance characteristics (Table 1). A SPICE simulation with an 800-µF output capacitor with 0.0125-Ω ESR reveals that converter with a 15-µs response time will meet the voltage regulation limit of the Pentium VRE processor (Figure 4). This translates into a converter with approximately 32-kHz unity gain bandwidth, assuming a second-order response system with a damping coefficient of 0.9.

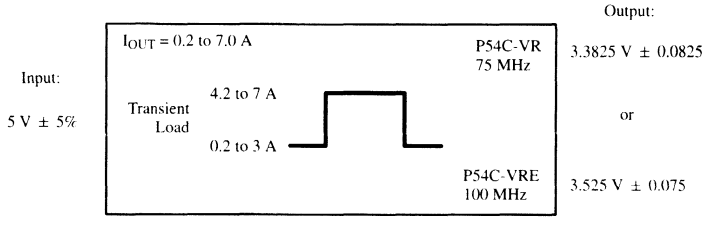


Figure 3. Pentium Converter Requirements

Table 1. Transient Response

Output Capacitance (µF)	ESR	Response Time for ±45-mV Regulation (µs)	BW for ±45-mV Regulation (kHz)	Response Time for ±75-mV Regulation (µs)	BW for ±75-mV Regulation (kHz)
800	0.0125	5	95	15	32
700	0.0143	4	120	14	34
600	0.0167	3	160	13	37
500	0.020	2	240	12	40
400	0.025	1	480	11	43

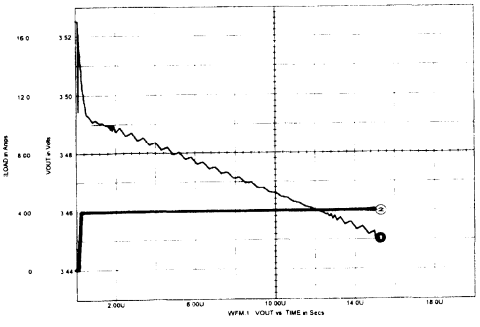


Figure 4. Transient Response

In reality, approximately 25% of the requisite regulation limit will be utilized by variations in the reference voltage and in the resistor dividers. To increase power supply manufacturing yields, it is also necessary to allow an additional tolerance in voltage regulation of 10% or more, further increasing the bandwidth requirement. If remote sensing is not available, delayed sensing of the processor voltage will cause a further drop.

Together, these constraints reduce the regulation limit of VRE Pentium converter from ± 75 mV to approximately ± 45 mV. To meet the ± 45-mV regulation limit requires a converter unity gain bandwidth of approximately 100 kHz. Obtaining a closed-loop bandwidth of 100 kHz requires a converter switching frequency of 375 kHz or greater. It also requires a ultra-fast error amplifier. Typically, the error amplifier must provide a bandwidth between 10 and 20 times the switching frequency to correctly respond to the stimuli. In the case of the Pentium converter, large bulk capacitors at the output of the converter and at the microprocessor require even greater bandwidth.

The Linear Regulation Solution

In the past, linear regulators were the ideal solution for low-power, 5-V/3-V conversion. Linear regulators provided an inherently quiet power system, eliminating EMI/EMC problems. Stability and compensation issues were also minimal, making the application and analysis as simple as possible. The advantages of linear regulators remained significant until power demands increased. Under these new conditions, their disadvantages become obvious. With a 7-A output current, a VRE converter will dissipate over 10 W of power into an already blazing hot system, requiring cumbersome heat sinks. These increase manufacturing difficulties and labor costs, which could easily offset the price advantage of the linear regulator solution. Meanwhile, the physical dimension requirements, 2.60 × 1.81 × 0.8 inches, could be easily exceeded with a large heat sink. Additionally, the cost savings of a linear regulator solution would be transferred to the increased costs of a larger, noisier fan required to circulate the additional heat over the circuit.

Current Mode vs. Voltage Mode

The Pentium's exacting dynamic load requirements makes it crucial for the designers to choose an optimal control method to provide voltage regulation during the transients. There are two modes of control for a buck converter operating in fixed frequency: voltage mode or current mode. The transfer function of current mode control with the converter's loop gain from output to control voltage operating in continuous inductor current can be derived using the state space average model and stated below.

$$Voc = \left(\frac{R_L}{R_{cs}}\right) \cdot \left(\frac{1}{1 + S \cdot C_o \cdot R_L}\right)$$

R_L = load resistance

R_{cs} = current sense resistance

C_o = output capacitance

As the above equation shows, current mode control has inherently good input line regulation since the transfer function is unaffected by the input voltage. As the input voltage changes, the slope of the inductor current changes instantaneously in compensation. Unfortunately, loop gain is load dependent. As the output load varies from minimum to maximum, as in the case of the Pentium, R_L ranges from 0.5 Ω to 17.6 Ω, and the loop gain varies by approximately 31 dB. This could cause the power supply to oscillate, if the loop is not compensated correctly for all load conditions. Typically the power supply is compensated for the maximum load resistance and the design must somehow accommodate the loop bandwidth reduction during the minimum load resistance. With –1 slope, loop bandwidth can decrease by more than a 1.5 decades in frequency. This decrease in bandwidth could have catastrophic effects on the dynamic transient response of the Pentium.

Once its output voltage regulation is exceeded, performance could also be impaired. Violation of output voltage regulations could cause the processor to exhibit failure characteristics ranging from an obvious, flagged software/hardware error to insidious, subtle, and unpredictable computational errors.

Current mode can also decrease noise immunity if the slope of the inductor current is too small to increase efficiency. By having the ramp voltage always close to the error voltage, a small noise injection into the current ramp could cause a large variation in the duty cycle.

Current mode also requires a slope compensation for duty cycles greater than 50%, adding parts and cost. For 5-V to 3.525-V conversion, the duty cycle exceeds 70% without counting FET and parasitic losses.

The transfer function for the voltage-mode control buck converter is stated below.

$$Voc = \left(\frac{V_{IN}}{V_s}\right) \cdot \left(\frac{1}{1 + S \cdot \frac{L}{R_L} + S^2 \cdot L \cdot C_o}\right)$$

V_{IN} = input voltage

V_s = ramp voltage

L = inductance

In the voltage mode control converter, loop gain is a function of input voltage instead of load resistance. Load resistance affects the Q-ing of the converter. Since the input voltage of the Pentium converter is virtually fixed, loop gain is considered constant. Input voltage for the Pentium varies from 4.75 V to 5.25 V, less than 1-dB variation. With the loop gain constant, the converter's bandwidth can be maximized and that same wide bandwidth can be maintained, irrespective of load changes. Therefore, the voltage-mode controlled converter is an ideal control method for the Pentium converter. With virtually fixed input voltages and a wide load variation, bandwidth can be maximized and transient response times minimized.

Voltage-mode control does have a minor disadvantage. As revealed in the above equation, its double-pole filter is generally more complicated to compensate than the single-pole filter of current-mode control. This means the addition of a pole-zero pair compensation network. Siliconix' application circuit solves this problem with optimal compensation values.

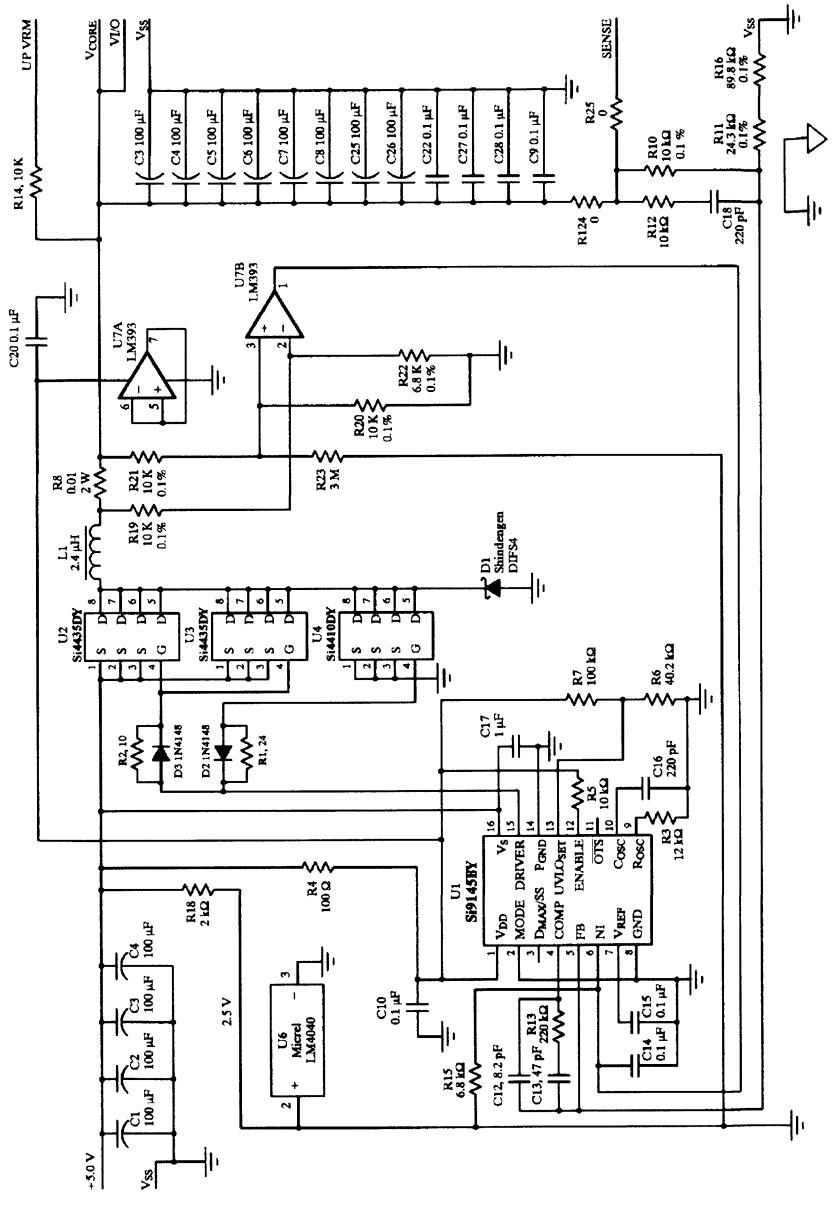
Transient Response

Maintaining the output voltage regulation within the ± 45-mV during the 4-A transient is not a trivial task for any power supply designer. Present solutions advertised by other PWM manufacturers using current-mode control lack bandwidth or dc gain to satisfy the voltage regulation of the VRE Pentium microprocessor. Without a voltage-mode PWM IC capable of switching at 375 kHz or above, designers have been forced to use current-mode controllers with much lower switching frequencies. Operating at a lower switching frequency generally yields slightly greater efficiency, but the disadvantages far outweigh the efficiency tradeoff. A lower operating frequency forces the designers to use much larger inductance and capacitance to maintain the same ripple voltage compared to the higher frequency operation, increasing space and cost. This increase in inductance also has a detrimental effect during the dynamic load transients. During the transition from maximum to minimum load, energy stored in the inductor makes a forced discharge into the output capacitance. Therefore, the larger the inductance, the more energy is stored in the inductor, causing a larger overshoot on the output voltage during the unloading transition. During the minimum-to-maximum current transition, a larger inductor delays the ramping of current demanded by the load, further sagging the output voltage.

The advantages of the Si9145BY, with its higher switching frequency and wide bandwidth error amplifier, are clearly demonstrated by comparing the two converters outlined in Table 2. A complete VRE-specified converter schematic operating at 375 kHz is shown in Figure 5.

Table 2. Converter Response Comparison

	Converter #1	Converter #2
Switching Frequency	375 kHz	125 kHz
Closed Loop BW	100 kHz	33 kHz
Output Capacitance	800 µF	2400 µF
Inductance	2.4 µH	7.2 µH



NOTE:

1. R24 and R25 are designed in the circuit to provide the flexibility to remote sense. Remove R24 if remote sensing is utilized. Remove R25 if remote sensing is not utilized.

2. Remove R17 to float the PWRGOOD signal. The new version of the Intel specification requires the PWRGOOD signal to be an open-collector output or floating.

Figure 5. Pentium Converter

Pin Description

Pin	Description
1A	V_{SS}
1B	V_{SS}
2A	V_{SS}
2B	V_{SS}
3A	ND
3B	VI/O
4A	VI/O
4B	VI/O
5A	+3.3 V
5B	+3.3 V
6A	+3.3 V
6B	+3.3 V
7A	V_{CORE}
7B	V_{CORE}
8A	V_{CORE}
8B	V_{CORE}
9A	V_{SS}
9B	V_{CORE}
10A	V_{CORE}
10B	V_{CORE}
11A	PWRGOOD
11B	UPVRM#
12A	SENSE
12B	DISABLE
13A	V_{SS}
13B	V_{SS}
14A	+5.0 V
15B	+5.0 V
15A	+5.0 V
15B	+5.0 V
CONN2XL15_ALPHA	

Figures 6 and 7 show the dynamic response to 4-A transients. Notice that the settling time of the 375-kHz converter is three times faster than that of the 125-kHz converter. The magnitude of regulation was identical for both converters. Note, however, that the 125-kHz converter's output capacitor and inductor size and value were increased by factor of three to maintain the consistency shown in Table 2. The +45-mV transient regulation result reaffirms the need for a converter bandwidth of 100 kHz or more to meet the regulation needs of the Pentium VRE processor.

Synchronous Rectification

A continuous inductor current mode is necessary to sustain the converter's large bandwidth, irrespective of control method (voltage or current). If the mode of operation changes from continuous to discontinuous inductor current mode, the transfer function of the converter will change drastically. This is precisely why synchronous rectification should be utilized.

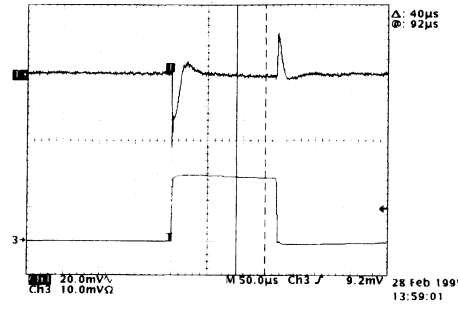


Figure 6. 100-kHz BW Transient Response

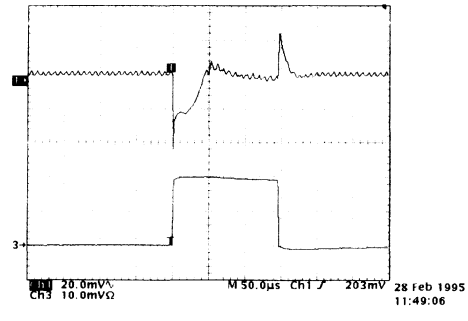


Figure 7. 33-kHz BW Transient Response

Synchronous rectification ensures continuous inductor current, regardless of output current. By maintaining continuous inductor current, the transfer function remains constant, preserving its large bandwidth. Figure 8 shows the bode plot of a non-synchronous converter. Notice the drastic decrease in the loop bandwidth from 100 kHz to 4.2 kHz as a result of the transformation into discontinuous mode.

Synchronous rectification also buys greater efficiency compared with using a Schottky diode as the rectifier, particularly when used in conjunction with

low-on-resistance power MOSFETs built on an innovative Trench technology.

For example, the Si4410DY Trench MOSFET from Siliconix offers an $r_{DS(on)}$ of 0.02 Ω at V_{GS} = 4.5 V. At a 7-A output current, the MOSFET drops only 0.14 V, compared with a typical voltage drop of 0.60 V across the Schottky diode. Efficiency can be increased considerably, since the synchronous rectifier conducts for approximately 30% of the period. Figure 9 shows the efficiency of the Pentium converter using two p-channel Si4435DYs as the high-side switch and one n-channel Si4410DY as the low-side switch.

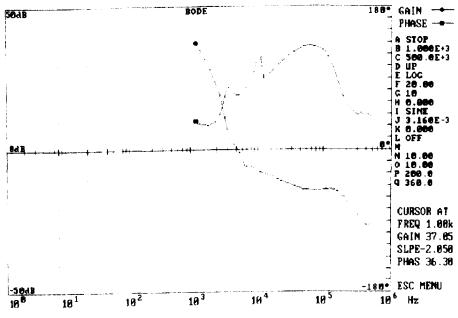


Figure 8. Non-Synchronous Bode Plot

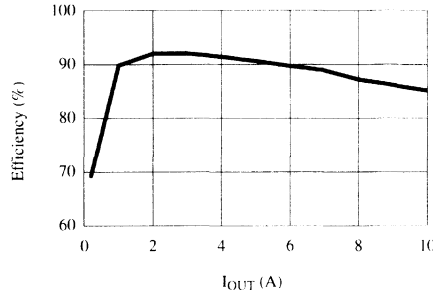


Figure 9. Efficiency Curve

Component Supplier List

Reference Designator	Part Number	Description	Pattern	Vendor	Phone #
C1-C8, C23-C26	TPSD107K010R	Tantalum Capacitor 100 µF, 10 V	D	AVX	(803) 448-9411
D1	DIFS4	1.1 A, 40 V	IF	Shindegen	(800) 543-6525
L1	CTX07-12717-1	2.4 µH, 7 A		Coiltronics	(407) 241-7876
P1	66527-015	15 × 2		Berg Electronics	(800) 237-2374
R8	SL-2	0.01 Ω, 2 W		KRL	(603) 668-3210
U1	Si9145BY	PWM IC	SO-16	Siliconix	(800) 554-5565
U2, U3	Si4435DY	P-Ch MOSFET	SO-8	Siliconix	(800) 554-5565
U4	Si4410DY	N-Ch MOSFET	SO-8	Siliconix	(800) 554-5565
U6	LM4040BIM	Reference	SOT-23	National	(408) 721-5000
U7	LM393M	Comparator	SO-8	National	(408) 721-5000

Bill of Material for Pentium Converter

Part	Used	Part Type	Designators	Footprint Pattern
1	2	0	R24 R25	0805
2	1	0.01, 2 W	R8	9433 2W
3	10	0.1 µF	C9 C10 C11 C14 C15 C19 C20 C22 C27 C28	0805
4	2	1N4148	D2 D3	MLL34
5	1	1 µF	C17	1825
6	1	2.4 µH	L1	INDUCTOR
7	1	2 k	R18	0805
8	1	3 M	R23	1206
9	1	6.8 k	R15	0805
10	1	6.8 k	R22	1206
11	1	8.2 pF	C12	0805
12	1	10	R2	0805
13	4	10K	R5 R12 R14 R17	0805
14	4	10K, 0.1%	R10 R19 R20 R21	1206
15	1	12K	R3	1206
16	1	24	R1	0805
17	1	24.3K, 0.1%	R11	1206
18	1	40.2 k	R6	0805
19	1	47 pF	C13	0805
20	1	89.8	R16	1206
21	1	100	R4	0805
22	1	100 k	R7	0805
23	12	100 µF	C1 C2 C3 C4 C5 C6 C7 C8 C23 C24 C25 C26	7374
24	1	220 k	R13	0805
25	2	220 pF	C16 C18	0805
26	1	CONN2X15 ALPHA	P1	CONN VRM
27	1	LM393M	U7	SO-8
28	1	MICREL LM4040BIM	U6	SOT-23-5
29	1	DIFS4	D1	6032
30	1	Si4410DY	U4	SO-8
31	2	Si4435DY	U2 U3	SO-8
32	1	Si9145BY	U1	SO-16

Dual-Output Power-Supply Controller for Notebook Computers

Features

- Fixed 5-V and 3.3-V Step-down Converters
- Less than 500-µA Quiescent Current per Converter
- 25-µA Shutdown Current
- 5.5-V to 30-V Operating Range

Description

The Si786 Dual Controller for Portable Computer Power Conversion is pin and functionally compatible with the MAX786 dual-output power supply controller for notebook computers. The device is designed as a drop-in replacement for that circuit.

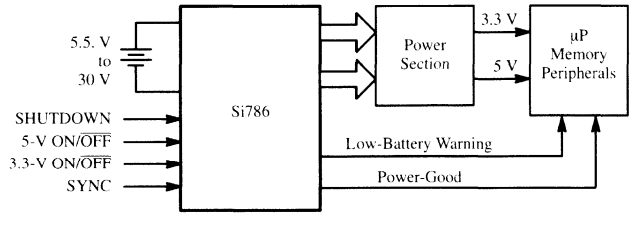
The circuit is a system level integration of two step-down controllers, micropower 5-V and 3.3-V linear regulators, and two comparators. The controllers perform high efficiency conversion of the battery pack energy (typically 12 V) or the output of an ac to dc wall converter (typically 18-V to 24-V dc) to 5-V and 3.3-V system supply voltages. The micropower linear regulator can be used to keep power management and back-up circuitry alive during the shutdown of the step-down converters. The comparators can be biased at any voltage between 2.7 V and the input voltage, simplifying battery monitoring or providing sufficient voltage to enhance the gate of a low on-resistance n-channel FET used in switching power to different zones in the system.

A complete power conversion and management system can be implemented with the Si786 Dual Controller for Portable Computer Power Conversion, an inexpensive linear regulator, the Si9140 SMP Controller for High Performance Processor Power Supplies, five Si4410 n-channel TrenchFET™ Power MOSFETs, one Si4435 p-channel TrenchFET Power MOSFET, and two Si9712 PC Card (PCMCIA) Interface Switches.

The Si9130 Pin-Programmable Dual Controller for Portable PCs is another integrated system level devices for portable PC power systems.

The Si786 is available in 28-pin SSOP package and specified to operate over the commercial (0°C to 70°C) and extended commercial (–10°C to 90°C) temperature ranges. See Ordering Information for corresponding part numbers.

Functional Block Diagram



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New Product

Absolute Maximum Ratings

V+ to GND ..... -0.3 V to 36 V
PGND to GND ..... ± 2 V
V_L to GND ..... -0.3V to 7 V
BST_3, BST_5 to GND ..... -0.3V to 36 V
LX_3 to BST_3 ..... -7 V to 0.3 V
LX_5 to BST_5 ..... -7 V to 0.3 V
Inputs/Outputs to GND
(D_1, D_2, $\overline{SHDN}$, ON_5, REF, SS_5, CS_5, FB_5, SYNC, CS_3, FB_3, SS_3, ON_3)) ..... -0.3 V, (V_L + 0.3 V)
V_H to GND ..... -0.3 V to 20 V
Q_1, Q_2 to GND ..... -0.3 V, (V_H + 0.3 V)
DL_3, DL_5 to PGND ..... -0.3 V, (V_L + 0.3 V)
DH_3 to LX_3 ..... -0.3 V (BST_3 + 0.3)
DH_5 to LX_5 ..... -0.3 V (BST_5 + 0.3)
REF, V_L Short to GND ..... Momentary
REF Current ..... 20 mA
V_L Current ..... 50 mA
Continuous Power Dissipation (T_A = 70°C)[a]
28-Pin SSOP[b] ..... 762 mW
Operating Temperature Range:
Si786CG/CRG/CSG ..... 0 to 70°C
Si786LG/LRG/LSG ..... –10° to 90°C
Lead Temperature (soldering, 10 sec) ..... 300°C

Notes
a. Device mounted with all leads soldered or welded to PC board.
b. Derate 9.52 mW/°C above 70°C.

Exposure to Absolute Maximum rating conditions for extended periods may affect device reliability. Stresses above Absolute Maximum rating may cause permanent damage. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum rating should be applied at any one time

Specifications

Parameter	Test Conditions Unless Otherwise Specified V+ = 15 V, I_{VL} = I_{REF} = 0 mA $\overline{SHDN}$ = ON_3 = ON_5 = 5 V Other Digital Input Levels 0 V or 5 V T_A = T_{MIN} to T_{MAX}		Limits Min[a]	Typ[c]	Max[a]	Unit
3.3-V and 5-V Step-Down Controllers						
Input Supply Range			5.5		30	V
FB_5 Output Voltage	0 mV < (CS_5-FB_5) < 70 mV, 6 V < V + < 30 V (includes load and line regulation)		4.80	5.08	5.20	V
FB_3 Output Voltage	0 mV < (CS_3-FB_3) < 70 mV, 6 V < V + < 30 V (includes load and line regulation)	Si786CG	3.17	3.35	3.46	V
		Si786CRG	3.32	3.50	3.60	V
		Si786CSG	3.46	3.65	3.75	V
Load Regulation	Either Controller (CS_ to FB_ = 0 to 70 mV)			2.5		%
Line Regulation	Either Controller (V+ = 6 V to 30 V)			0.03		%/V
Current-Limit Voltage	CS_3-FB_3 or CS_5-FB_5		80	100	120	mV
SS_3/SS_5 Source Current			2.5	4.0	6.5	µA
SS_3/SS_5 Fault Sink Current			2			mA
Internal Regulator and Reference						
V_L Output Voltage	ON_5 = ON_3 = 0 V, 5.5 V < V+ < 30 V 0 mA < I_L < 25 mA		4.5		5.5	V
V_L Fault Lockout Voltage	Falling Edge, Hysteresis = 1%		3.6		4.2	V
V_L/FB_5 Switchover Voltage	Rising Edge of FB_5, Hysteresis = 1%		4.2		4.7	V
REF Output Voltage	No External Load[b]		3.24		3.36	V
REF Fault Lockout Voltage	Falling Edge		2.4		3.2	V
REF Load Regulation	0 mA < I_L < 5 mA[d]			30	75	mV

Specifications

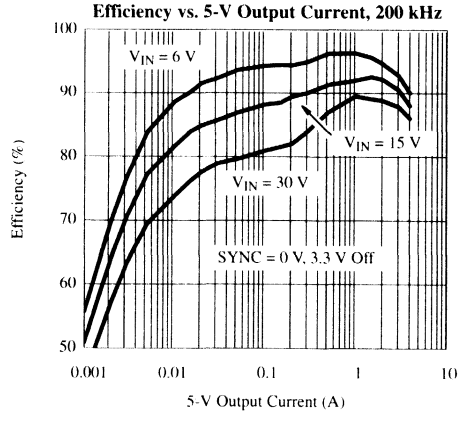
Parameter	Test Conditions Unless Otherwise Specified V+ = 15 V, $I_{VL} = I_{REF}$ = 0 mA $\overline{SHDN}$ = ON_3 = ON_5 = 5 V Other Digital Input Levels 0 V or 5 V $T_A = T_{MIN}$ to T_{MAX}	Limits Min[a]	Typ[c]	Max[a]	Unit
Internal Regulator and Reference (Cont'd)					
V+ Shutdown Current	$\overline{SHDN}$ = D_1 = D_2 = ON_3 = ON_5 = 0 V V+ = 30 V		25	40	µA
V+ Standby Current	D_1 = D_2 = ON_3 = ON_5 = 0 V, V+ = 30 V		70	110	
Quiescent Power Consumption (both PWM controllers on)	D_1 = D_2 = 0 V, FB_5 = CS_5 = 5.25 V FB_3 = CS_3 = 3.5 V		5.5	8.6	mW
V+ Off Current	FB_5 = CS_5 = 5.25 V, V_L Switched Over to FB_5		30	60	µA
Comparators					
D_1, D_2 Trip Voltage	Falling Edge, Hysteresis = 1%	1.61		1.69	V
D_1, D_2 Input Current	D_1 = D_2 = 0 V, 5 V			± 100	nA
Q_1, Q_2 Source Current	V_H = 15 V, V_{OUT} = 2.5 V	12	20	30	µA
Q_1, Q_2 Sink Current		200	500	1000	
Q_1, Q_2 Output High Voltage	I_{SOURCE} = 5 µA, V_H = 3 V	V_H - 0.5			V
Q_1, Q_2 Output Low Voltage	I_{SINK} = 20 µA, V_H = 3 V			0.4	
Quiescent V_H Current	V_H = 18 V, D_1 = D_2 = 5 V, No External Load		4	10	µA
Oscillator and Inputs/Outputs					
Oscillator Frequency	SYNC = 3.3 V	270	300	330	kHz
	SYNC = 0 V, 5 V	170	200	230	
SYNC High Pulse Width		200			ns
SYNC Low Pulse Width		200			
SYNC Rise/Fall Time	Not Tested			200	
Oscillator SYNC Range		240		350	kHz
Maximum Duty Cycle	SYNC = 3.3 V	89	92		%
	SYNC = 0 V, 5 V	92	95		
Input Low Voltage	$\overline{SHDN}$, ON_3, ON_5 SYNC			0.8	V
Input High Voltage	$\overline{SHDN}$, ON_3, ON_5	2.4			
	SYNC	V_L - 0.5			
Input Current	$\overline{SHDN}$, ON_3, ON_5 V_{IN} = 0 V, 5 V			± 1	µA
DL_3/DL_5 Sink/Source Current	V_{OUT} = 2 V		1		A
DH_3/DH_5 Sink/Source Current	BST_3 - LX_3 = BST_5 - LX_5 = 4.5 V, V_{OUT} = 2 V		1		
DL_3/DL_5 On-Resistance	High or Low			7	Ω
DH_3/DH_5 On-Resistance	High or Low BST_3 - LX_3 = BST_5 - LX_5 = 4.5 V			7	

Notes
a. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum.
b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
c. Since the reference uses V_L as its supply, its V+ line regulation error is insignificant.
d. The main switching outputs track the reference voltage. Loading the reference reduces the main outputs slightly according to the closed-loop gain (AV_{CL}) and the reference voltage load-regulation error. AV_{CL} for the 3.3-V supply is unity gain. AV_{CL} for the 5-V supply is 1.54.

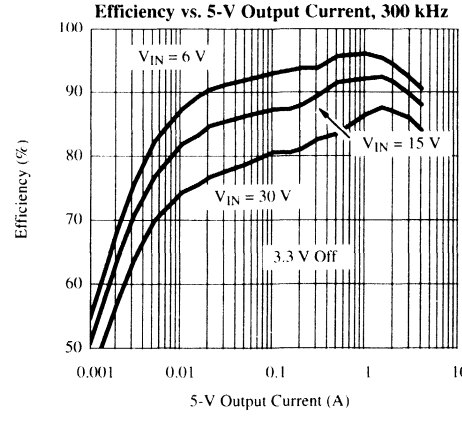
New Product

Typical Characteristics (25°C Unless Noted)

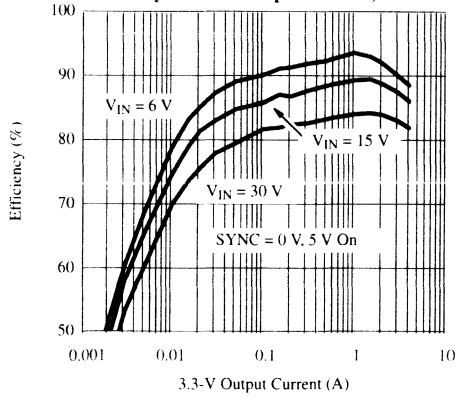
Efficiency vs. 5-V Output Current, 200 kHz



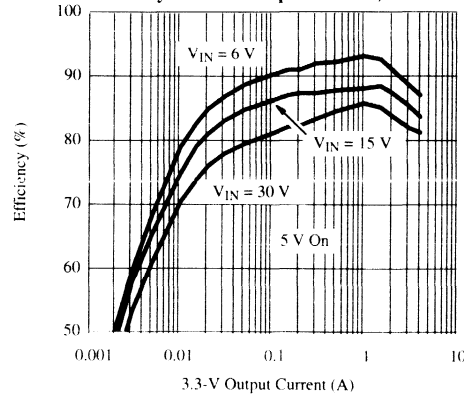
Efficiency vs. 5-V Output Current, 300 kHz



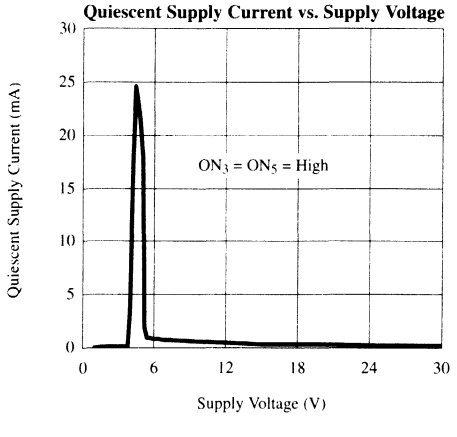
Efficiency vs. 3.3-V Output Current, 200 kHz



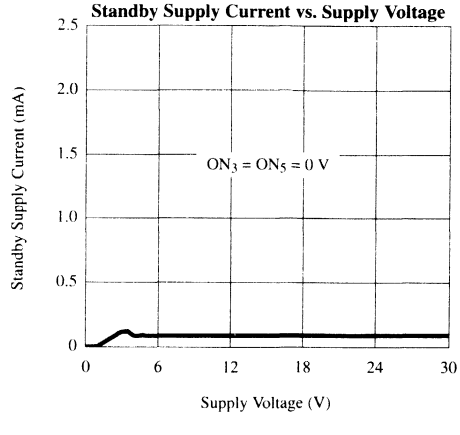
Efficiency vs. 3.3-V Output Current, 300 kHz



Quiescent Supply Current vs. Supply Voltage

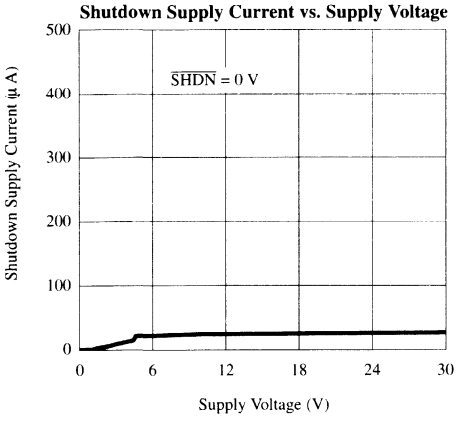


Standby Supply Current vs. Supply Voltage

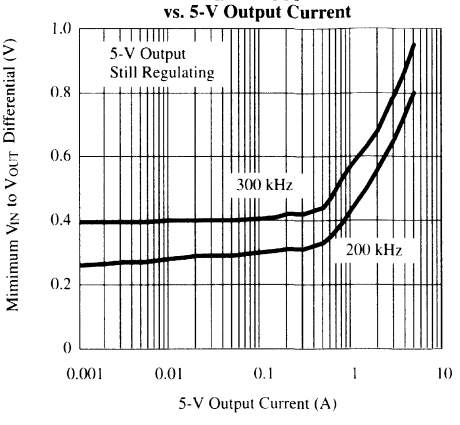


Typical Characteristics (25°C Unless Noted)

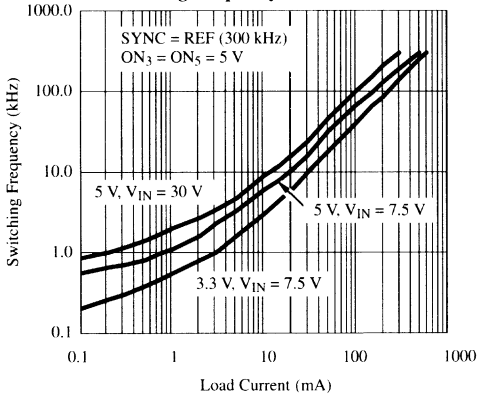
Shutdown Supply Current vs. Supply Voltage



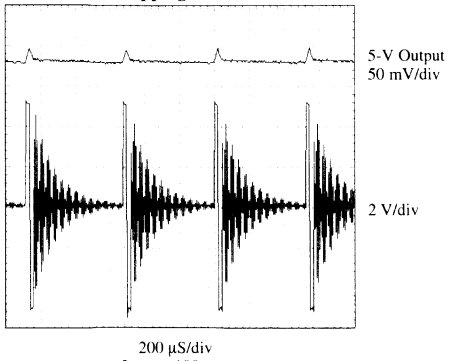
Minimum V_{IN} to V_{OUT} Differential vs. 5-V Output Current



Switching Frequency vs. Load Current

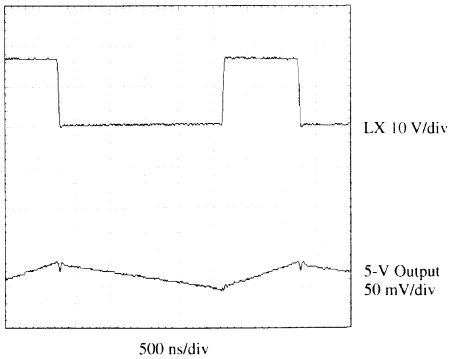


Pulse-Skipping Waveforms



200 μS/div
I_{Load} = 100 mA
V_{IN} = 10 V

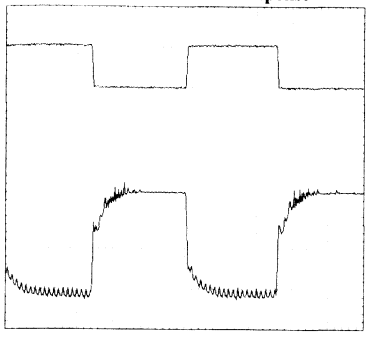
Pulse-Width Modulation Mode Waveforms



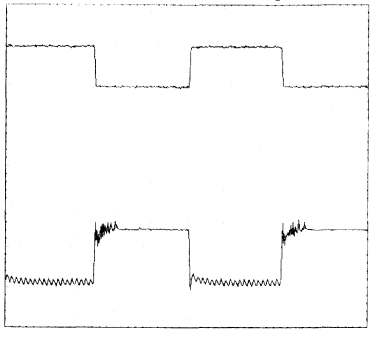
500 ns/div
5-V Output Current = 1 A
V_{IN} = 16 V

Typical Characteristics (25°C Unless Noted)

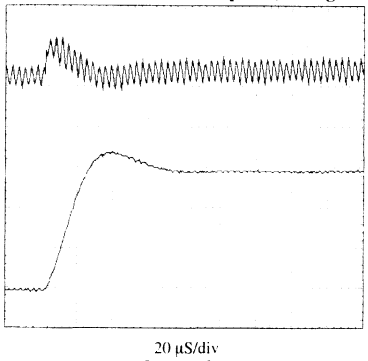
5-V Load-Transient Response



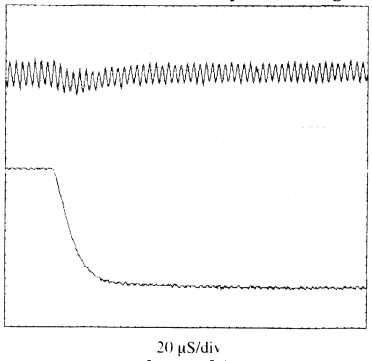
3.3-V Load-Transient Response



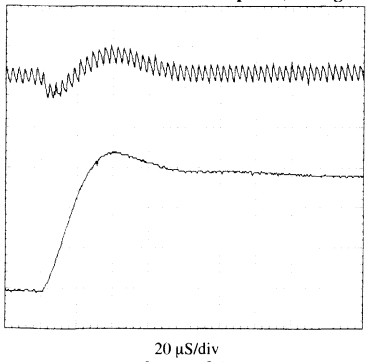
5-V Line-Transient Response, Rising



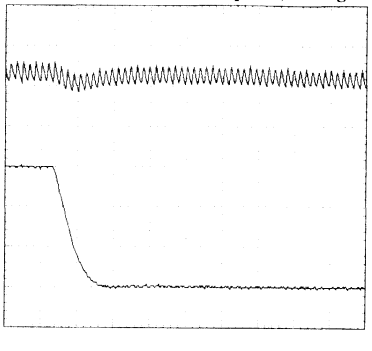
5-V Line-Transient Response, Falling



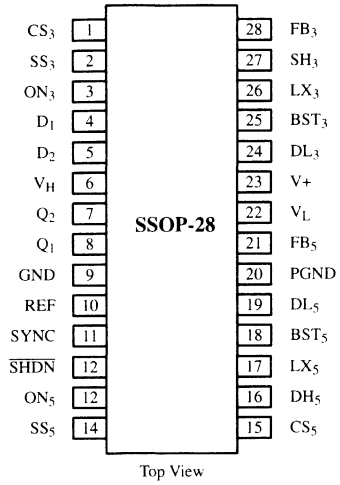
3.3-V Line-Transient Response, Rising



3.3-V Line-Transient Response, Falling



Pin Configuration



Top View

Ordering Information

Part Number	Temperature Range	V_{OUT}
Si786CG	0 to 70°C	3.3 V
Si786CRG		3.45 V
Si786CSG		3.6 V
*Si786LG	−10° to 90°C	3.3 V
*Si786LRG		3.45 V
*Si786LSG		3.6 V

*Pre–Release Information

Demo Board	Temperature Range	Board Type
Si786DB	0 to 70°C	Surface Mount

Pin Number	Symbol	Description
1	CS_3	Current-sense input for 3.3-V Buck controller—this pins over current threshold is 100 mV with respect to FB_3.
2	SS_3	Soft-start input for 3.3 V. Connect capacitor from SS_3 to GND.
3	ON_3	ON/$\overline{OFF}$ logic input disables the 3.3-V Buck controller. Connect directly to V_L for automatic turn-on.
4	D_1	Comparator #1 noninverting input, threshold = 1.650 V. Comparator #1 output = Q1. Connect to GND if unused.
5	D_2	Comparator #2 noninverting input (see D_1).
6	V_H	External bias supply-voltage input for comparators #1 and #2.
7	Q_2	Comparator #2 output. Sources 20 µA from V_H when D_2 is high. Sinks 500 µA to GND when D_2 is low regardless of V_H input voltage.
8	Q_1	Comparator #1 output (see Q_2).
9	GND	Analog ground.
10	REF	3.3-V reference output. Supplies external loads up to 5 mA.
11	SYNC	Oscillator control/synchronization input. Connect capacitor to GND, 1-µF/mA output or 0.22 µF minimum. For external clock synchronization, a rising edge starts a new cycle to start. To use internal 200-kHz oscillator, connect to VL or GND. For 300-kHz oscillator, connect to REF.
12	$\overline{SHDN}$	Shutdown logic input, active low. Connect to V_L for automatic turn-on. The 5-V V_L supply will not be disabled in shutdown allowing connection to $\overline{SHDN}$.
13	ON_5	ON/$\overline{OFF}$ logic input disables the 5-V Buck Controller. Connect to V_L for automatic turn-on.
14	SS_5	Soft-start control input for 5 V Buck controller. Connect capacitor from SS_5 to GND.
15	CS_5	Current-sense input for 5 V Buck controller—this pins over current threshold is 100 mV referenced to FB_3.
16	DH_5	Gate-drive output for the 5-V supply high-side n-channel MOSFET.
17	LX_5	Inductor connection for the 5-V supply.
18	BST_5	Boost capacitor connection for the 5-V supply.
19	DL_5	Gate-drive output for the 5-V supply rectifying n-channel MOSFET.

New Product

Pin Configuration (Cont'd)

Pin Number	Symbol	Description
20	PGND	Power Ground.
21	FB_5	Feedback input for the 5-V Buck controller.
22	V_L	5-V logic supply voltage for internal circuitry—able to source 5-mA external loads. V_L remains on with valid voltage at V+.
23	V+	Supply voltage input.
24	DL_3	Gate-drive output for the 3.3-V supply rectifying n-channel MOSFET.
25	BST_3	Boost capacitor connection for the 3.3-V supply.
26	LX_3	Inductor connection for the 3.3-V supply.
27	DH_3	Gate-drive output for the 3.3-V supply high-side n-channel MOSFET.
28	FB_3	Feedback input for the 3.3-V Buck controller.

Description of Operation

The Si786 is a dual step-down converter, which takes a 5.5-V to 30-V input and supplies power via two PWM controllers (see Figure 1). These 5-V and 3.3-V supplies run on an optional 300-kHz or 200-kHz internal oscillator, or an external sync signal. Amount of output current is limited by external components, but can deliver greater than 6 A on either supply. As well as these two main Buck controllers, additional loads can be driven from two micropower linear regulators, one 5 V (V_L) and the other 3.3 V (REF)—see Figure 2. These supplies are each rated to deliver 5 mA. If the linear regulator circuits fall out of regulation, both Buck controllers are shut down.

Two voltage comparators with adjustable output voltages are included in the Si786. They can be used for gate drive in load switching applications, where n-channel MOSFETs are used. Logic level voltages can be generated as well, for instance to serve as µP interfacing (e.g. a Power-good signal).

3.3-V Switching Supply

The 3.3-V supply is regulated by a current-mode PWM controller in conjunction with several externals: two n-channel MOSFETs, a rectifier, an inductor and output capacitors (see Figure 1). The gate drive supplied by DH_3 needs to be greater than V_L, so it is provided by the bootstrap circuit consisting of a 100-nF capacitor and diode connected to BST_3.

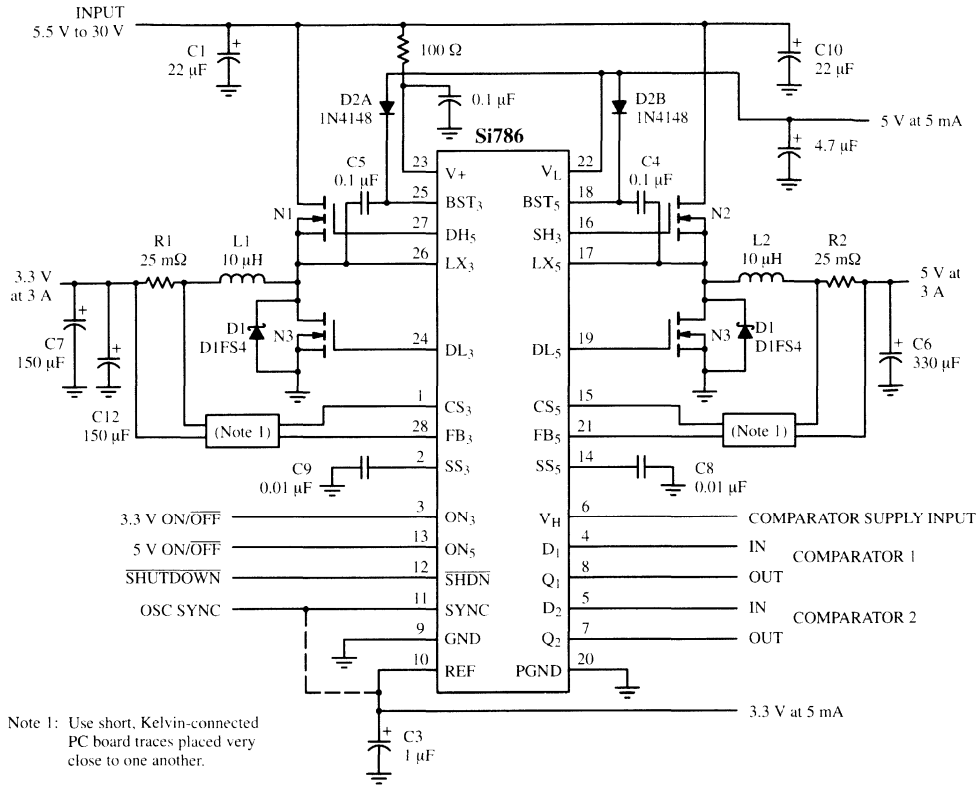
A low-side switching MOSFET connected to DL_3 increases efficiency by reducing the voltage across the rectifier diode. A low value sense resistor in series with the inductor sets the maximum current limit, to disallow current overloads at power-on or in short-circuit situations.

The soft-start feature on the Si786 is capacitor programmable; pin SS_3 functions as a constant current source to the external capacitor connected to GND. Excess currents at power-on are avoided, and power-supplies can be sequenced with different turn-on delay times by selecting the correct capacitor value.

5-V Switching Supply

The 5-V supply is regulated by a current-mode PWM controller which is nearly the same as the 3.3-V output. The dropout voltage across the 5-V supply, as shown in the schematic in Figure 1, is 400 mV (typ) at 2 A. If the voltage at V+ falls, nearing 5 V, the 5-V supply will lower as well, until the V_L linear regulator output falls below the 4-V undervoltage lockout threshold. Below this threshold, the 5-V controller is shut off.

The frequency of both PWM controllers is set at 300 kHz when the SYNC pin is tied to REF. Connecting SYNC to either GND or V_L sets the frequency at 200 kHz.



Note 1: Use short, Kelvin-connected PC board traces placed very close to one another.

Figure 1. Si786 Application Circuit

3.3-V and 5-V Switching Controllers

Each PWM controller on the Si786 is identical with the exception of the preset output voltages. The controllers only share three functional blocks (see Figure 2): the oscillator, the voltage reference (REF) and the 5-V logic supply (V_L). The 3.3-V and 5-V controllers are independently enabled with pins ON_3 and ON_5, respectively. The PWMs are a direct-summing type, without the typical integrating error amplifier along with the phase shift which is a side effect of this type of topology. Feedback compensation is not needed, as long as the output capacitance and its ESR requirements are met, according to the *Design Considerations* section of this data sheet.

The main PWM comparator is an open loop device which is comprised of three comparators summing four signals: the feedback voltage error signal, current sense signal, slope-compensation ramp and voltage reference as shown in Figure 3. This method of control comes closer to the ideal of maintaining the output voltage on a cycle-by-cycle basis. When the load demands high current levels, the controller is in full PWM mode. Every cycle from the oscillator asserts the output latch and drives the gate of the high-side MOSFET for a period determined by the duty cycle (approximately $V_{OUT}/V_{IN} \times 100\%$) and the frequency. The high-side switch turns off, setting the synchronous rectifier latch and 60ns later, the rectifier MOSFET turns on. The low-side switch stays on until the start of the next clock cycle in continuous mode, or until the inductor current becomes positive again in discontinuous mode. In over-current situations, where the inductor current is greater than the 100-mV current-limit threshold, the high-side latch is reset and the high-side gate drive is shut off.

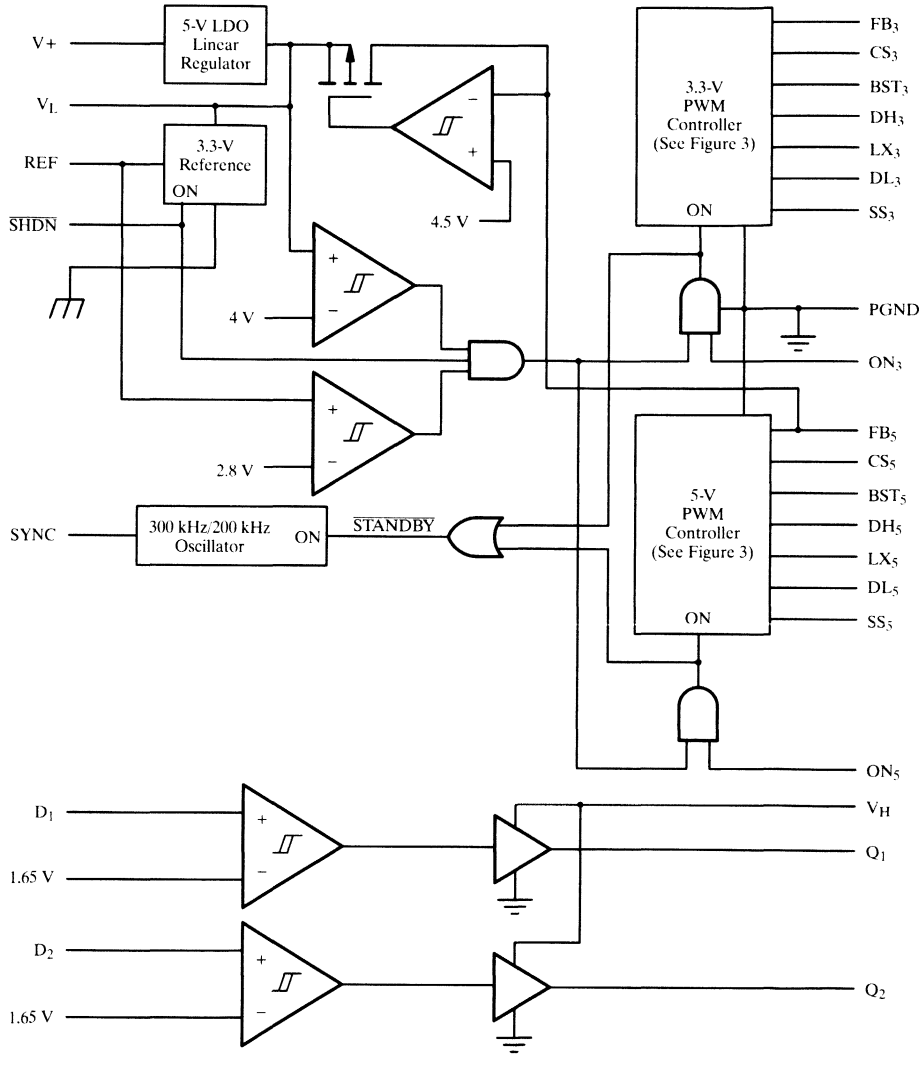


Figure 2. Si786 Block Diagram

During low-current load requirements, the inductor current will not deliver the 25-mV minimum current threshold. The Minimum Current comparator signals the PWM to enter pulse-skipping mode when the threshold has not been reached. Pulse-skipping mode skips pulses to reduce switching losses, the losses which decrease efficiency the most at light load. Entering this mode causes the minimum current comparator to reset the high-side latch at the beginning of each oscillator cycle.

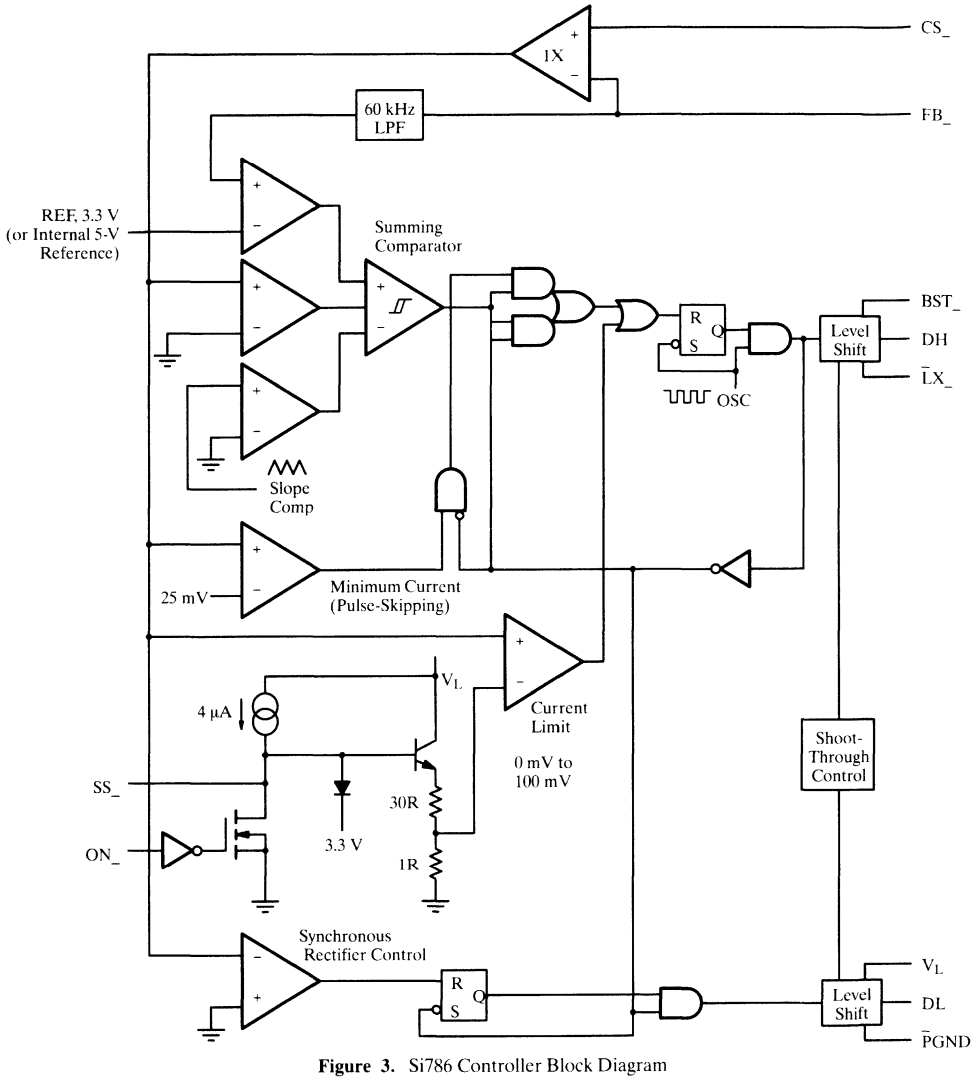


Figure 3. Si786 Controller Block Diagram

Soft-Start

To slowly bring up the 3.3-V and 5-V supplies, connect capacitors from SS_3 and SS_5 to GND. Asserting ON_3 or ON_5 starts a 4-µA constant current source to charge these capacitors to 4 V. As the voltage on these pins ramps up, so does the current limit comparator threshold, to increase the duty cycle of the MOSFETs to their maximum level.

If ON_3 or ON_5 are left low, the respective capacitor is discharged to GND. Leaving the SS_3 or SS_5 pins open will cause either controller to reach the terminal over-current level within 10 µs.

Soft start helps prevent current spikes at turn-on and allows separate supplies to be delayed using external programmability.

Synchronous Rectifiers

Synchronous rectification replaces the Schottky rectifier with a MOSFET, which can be controlled to increase the efficiency of the circuit.

When the high-side MOSFET is switched off, the inductor will try to maintain its current flow, inverting the inductor's polarity. The path of current then becomes the circuit made of the Schottky diode, inductor and load, which will charge the output capacitor. The diode has a 0.5-V forward voltage drop, which contributes a significant amount of power loss, decreasing efficiency. A low-side switch is placed in parallel with the Schottky diode and is turned on just after the diode begins to conduct. Because the $r_{DS(ON)}$ of the MOSFET is low, the I*R voltage drop will not be as large as the diode, which increases efficiency. The low-side rectifier is shut off when the inductor current drops to zero.

Shoot-through current is the result when both the high-side and rectifying MOSFETs are turned on at the same time. Break-before-make timing internal to the Si786 manages this potential problem. During the time when neither MOSFET is on, the Schottky is conducting, so that the body diode in the low-side MOSFET is not forced to conduct.

Synchronous rectification is always active when the Si786 is powered-up, regardless of the operational mode.

Gate-Driver Boost

The high-side n-channel drive is supplied by a flying-capacitor boost circuit (see Figure 4). The capacitor takes a charge from V_L and then is connected from gate to source of the high-side MOSFET to provide gate enhancement. At power-up, the low-side MOSFET pulls LX_ down to GND and charges the BST_ capacitor connected to 5 V. During the second half of the oscillator cycle, the controller drives the gate of the high-side MOSFET by internally connecting node BST_ to DH_. This supplies a voltage 5 V higher than the battery voltage to the gate of the high-side MOSFET.

Oscillations on the gates of the high-side MOSFET in discontinuous mode are a natural occurrence caused by the LC network formed by the inductor and stray capacitance at the LX_ pins. The negative side of the BST_ capacitor is connected to the LX_ node, so ringing at the inductor is translated through to the gate drive.

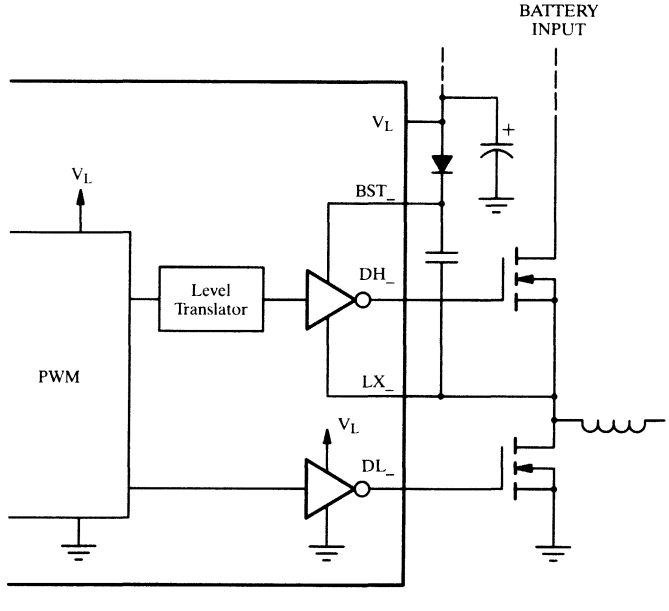


Figure 4. Boost Supply for Gate Drivers

Operational Modes

PWM Mode

The 3.3-V and 5-V Buck controllers operate in continuous-current PWM mode when the load demands more than approximately 25% of the maximum current (see typical curves). The duty cycle can be approximated as Duty_Cycle = V_{OUT}/V_{IN}.

In this mode, the inductor current is continuous; in the first half of the cycle, the current slopes up when the high-side MOSFET conducts and then, in the second half, slopes back down when the inductor is providing energy to the output capacitor and load. As current enters the inductor in the first half-cycle, it is also continuing through to the load; hence, the load is receiving continuous current from the inductor. By using this method, output ripple is minimized and smaller form-factor inductors can be used. The output capacitor's ESR has the largest effect on output ripple. It is typically under 50 mV; the worst case condition is under light load with higher input battery voltage.

Pulse-Skipping Mode

When the load requires less than 25% of its maximum, the Si786 enters a mode which drives the gate for one clock cycle and skips the majority of the remaining cycles. Pulse-skipping mode cuts down on the switching losses, the dominant power consumer at low current levels.

In the region between pulse-skipping mode and PWM mode, the controller may transition between the two modes, delivering spurts of pulses. This may cause the current waveform to look irregular, but will not overly affect the ripple voltage. Even in this transitional mode efficiency will stay high.

Current Limit

The current through an external resistor, is constantly monitored to protect against over-current. A low value resistor is placed in series with the inductor. The voltage across it is measured by connecting it between CS_ and FB_. If this voltage is larger than 100 mV, the high-side MOSFET drive is shut down. Eliminating over-currents protects the MOSFET, the load and the power source. Typical values for the sense resistors with a 3-A load will be 25 mΩ.

Oscillator and SYNC

There are two ways to set the Si786 oscillator frequency: by using an external SYNC signal, or using the internal oscillator. The SYNC pin can be driven with an external CMOS level signal with frequency from 240 kHz and 350 kHz to synchronize to the internal oscillator. Tying SYNC to either V_L or GND sets the frequency to 200 kHz and to REF sets the frequency to 300 kHz.

Operation at 300 kHz is typically used to minimize output passive component sizes. Slower switching speeds of 200 kHz may be needed for lower input voltages.

Internal V_L and REF

A 5-V linear regulator supplies power to the internal logic circuitry. The regulator is available for external use from pin V_L, able to source 5 mA. A 4.7-µF capacitor should be connected between V_L and GND. To increase efficiency, when the 5 V switching supply has voltage greater than 4.5 V, V_L is internally switched over to the output of the 5-V switching supply and the linear regulator is turned off.

The 5-V linear regulator provides power to the internal 3.3-V bandgap reference (REF). The 3.3-V reference can supply 5 mA to an external load, connected to pin REF. Between REF and GND connect a capacitor, 0.22 µF plus 1 µF per mA of load current. The switching outputs will vary with the reference; therefore, placing a load on the REF pin will cause the main outputs to decrease slightly, within the specified regulation tolerance.

V_L and REF supplies stay on as long as V+ is greater than 4.5 V, even if the switching supplies are not enabled. This feature is necessary when using the micropower regulators to keep memory alive during shutdown.

Both linear regulators can be connected to their respective switching supply outputs. For example, REF would be tied to the output of the 3.3 V and V_L to 5 V. This will keep the main supplies up in standby mode, provided that each load current in shutdown is not larger than 5 mA.

Fault Protection

The 3.3 V and 5 V switching controllers as well as the comparators are shut down when one of the linear regulators drops below 85% of its nominal value; that is, shut down will occur when $V_L < 4.0$ V or REF < 2.8 V.

Design Considerations

Inductor Design

Three specifications are required for inductor design: inductance (L), peak inductor current (I_{LPEAK}), and coil resistance (R_L). The equation for computing inductance is:

$$L = \frac{(V_{OUT})(V_{IN(MAX)}-V_{OUT})}{(V_{IN(MAX)})(f)(I_{OUT})(LIR)}$$

Where: V_{OUT} = Output voltage (3.3 V or 5 V);
$V_{IN(MAX)}$ = Maximum input voltage (V);
f = Switching frequency, normally 300 kHz;
I_{OUT} = Maximum dc load current (A);
LIR = Ratio of inductor peak-to-peak ac current to average dc load current, typically 0.3.

When LIR is higher, smaller inductance values are acceptable, at the expense of increased ripple and higher losses.

The peak inductor current (I_{LPEAK}) is equal to the steady-state load current (I_{OUT}) plus one half of the peak-to-peak ac current (I_{LPP}). Typically, a designer will select the ac inductor current to be 30% of the steady-state current, which gives I_{LPEAK} equal to 1.15 times I_{OUT}.

The equation for computing peak inductor current is:

$$I_{LPEAK} = I_{OUT} + \frac{(V_{OUT})(V_{IN(MAX)}-V_{OUT})}{(2)(f)(L)(V_{IN(MAX)})}$$

Output Capacitors

The output capacitors determine loop stability and ripple voltage at the output. In order to maintain stability, minimum capacitance and maximum ESR requirements must be met according to the following equations:

$$C_F > \frac{V_{REF}}{(V_{OUT})(R_{CS})(2)(\pi)(GBWP)}$$

and,

$$ESR_{CF} < \frac{(V_{OUT})(R_{CS})}{V_{REF}}$$

Where: C_F = Output filter capacitance (F)
V_{REF} = Reference voltage, 3.3 V;
V_{OUT} = Output voltage, 3.3 V or 5 V;
R_{CS} = Sense resistor (Ω);
GBWP = Gain-bandwidth product, 60 kHz;
ESR_{CF} = Output filter capacitor ESR (Ω).

Both minimum capacitance and maximum ESR requirements must be met. In order to get the low ESR, a capacitance value of two to three times greater than the required minimum may be necessary.

The equation for output ripple in continuous current mode is:

$$V_{OUT(RPL)} = I_{LPP(MAX)} \times \left(ESR_{CF} + \frac{1}{(2 \times \Pi \times f \times C_F)}\right)$$

The equations for capacitive and resistive components of the ripple in pulse-skipping mode are:

$$V_{OUT(RPL)}(C) = \frac{(4)(10^{-4})(L)}{(R_{CS}^2)(C_F)} \times \left(\frac{1}{V_{OUT}} + \frac{1}{V_{IN}-V_{OUT}}\right)$$

$$V_{OUT(RPL)}(R) = \frac{(0.02)(ESR_{CF})}{R_{CS}}$$

The total ripple, $V_{OUT(RPL)}$, can be approximated as follows:

if $V_{OUT(RPL)}(R) < 0.5\ V_{OUT(RPL)}(C)$,
then $V_{OUT(RPL)} = V_{OUT(RPL)}(C)$,
otherwise, $V_{OUT(RPL)} = 0.5\ V_{OUT(RPL)}(C) + V_{OUT(RPL)}(R)$.

Lower Voltage Input

The application circuit shown here can be easily modified to work with 5.5-V to 12-V input voltages. Oscillation frequency should be set at 200 kHz and increase the output capacitance to 660 µF on the 5-V output to maintain stable performance up to 2 A of load current. Operation on the 3.3-V supply will not be affected by this reduced input voltage.

Pin-Programmable Dual Controller for Portable PCs

Features

- Fixed 5-V and Programmable 3.3-V, 3.45 V, or 3.6 V Step-Down Converters
- Less than 500-µA Quiescent Current per Converter
- 25-µA Shutdown Current
- 5.5-V to 30-V Operating Range

Description

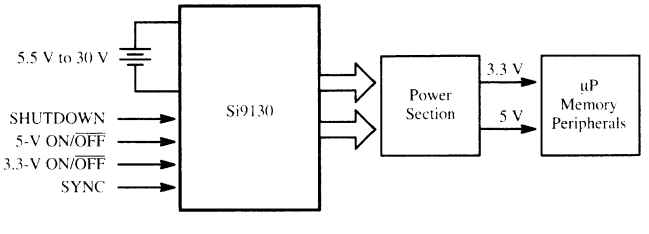
The Si9130 Pin-programmable Dual Controller for Portable PCs is a pin-programmable version of the Si786 dual-output power supply controller for notebook computers. The Buck controllers provide 5 V and a pin-programmable output delivering 3.3 V, 3.45 V, or 3.6 V.

The circuit is a system level integration of two step-down controllers and micropower 5-V and 3.3-V linear regulators. The controllers perform high efficiency conversion of the battery pack energy (typically 12 V) or the output of an ac to dc wall converter (typically 18-V to 24-V dc) to 5-V and 3.3-V system supply voltages. The micropower linear regulator can be used to keep power management and back-up circuitry alive during the shutdown of the step-down converters.

A complete power conversion and management system can be implemented with the Si9130 Pin-programmable Dual Controller for Portable PCs, an inexpensive linear regulator, the Si9140 SMP Controller for High Performance Processor Power Supplies, five Si4410 n-channel TrenchFET™ Power MOSFETs, one Si4435 p-channel TrenchFET™ Power MOSFET, and two Si9712 PC Card (PCMCIA) Interface Switches.

The Si9130 is available in 28-pin SSOP package and specified to operate over the commercial (0°C to 70°C) and extended commercial (–10°C to 90°C) temperature ranges. See Ordering Information for corresponding part numbers.

Functional Block Diagram



Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70190.

New Product

Absolute Maximum Ratings

V+ to GND ..... -0.3 V t0 36 V
PGND to GND ..... ± 2 V
V_L to GND ..... -0.3V to 7 V
BST_3, BST_5 to GND ..... -0.3V to 36 V
LX_3 to BST_3 ..... -7 V to 0.3 V
LX_5 to BST_5 ..... -7 V to 0.3 V
Inputs/Outputs to GND
(3.45ADJ, 3.6ADJ, $\overline{SHDN}$, ON_5, REF, SS_5, CS_5, FB_5, SYNC, CS_3, FB_3, SS_3, ON_3)) ..... -0.3 V, (V_L + 0.3 V)
DL_3, DL_5 to PGND ..... -0.3 V, (V_L + 0.3 V)
DH_3 to LX_3 ..... -0.3 V (BST_3 + 0.3)
DH_5 to LX_5 ..... -0.3 V (BST_5 + 0.3)

REF, V_L Short to GND ..... Momentary
REF Current ..... 20 mA
V_L Current ..... 50 mA
Continuous Power Dissipation (T_A = 70°C)[a]
28-Pin SSOP[b] ..... 762 mW
Operating Temperature Range:
Si9130CG ..... 0 to 70°C
Si9130LG ..... –10° to 90°C
Lead Temperature (soldering, 10 sec) ..... 300°C

Notes
a. Device mounted with all leads soldered or welded to PC board.
b. Derate 9.52 mW/°C above 70°C.

Exposure to Absolute Maximum rating conditions for extended periods may affect device reliability. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied.

Specifications

Parameter	Test Conditions Unless Otherwise Specified V+ = 15 V, I_{VL} = I_{REF} = 0 mA $\overline{SHDN}$ = ON_3 = ON_5 = 5 V Other Digital Input Levels 0 V or 5 V T_A = T_{MIN} to T_{MAX}		Limits Min[a]	Typ[c]	Max[a]	Unit
3.3-V and 5-V Step-Down Controllers						
Input Supply Range			5.5		30	V
FB_5 Output Voltage	0 mV < (CS_5-FB_5) < 70 mV, 6 V < V + < 30 V (includes load and line regulation)		4.80	5.08	5.20	
FB_3 Output Voltage	0 mV < (CS_3-FB_3) < 70 mV, 6 V < V + < 30 V (includes load and line regulation)	3.6ADJ = 3.45ADJ = OPEN	3.17	3.35	3.46	
		3.6ADJ = OPEN, 3.45ADJ = GND	3.32	3.50	3.60	
		3.6ADJ = GND, 3.45ADJ = OPEN	3.46	3.65	3.75	
Load Regulation	Either Controller (CS_ to FB_ = 0 to 70 mV)			2.5		%
Line Regulation	Either Controller (V+ = 6 V to 30 V)			0.03		%/V
Current-Limit Voltage	CS_3-FB_3 or CS_5-FB_5		80	100	120	mV
SS_3/SS_5 Source Current			2.5	4.0	6.5	µA
SS_3/SS_5 Fault Sink Current			2			mA
Internal Regulator and Reference						
V_L Output Voltage	ON_5 = ON_3 = 0 V, 5.5 V < V+ < 30 V 0 mA < I_L < 25 mA		4.5		5.5	V
V_L Fault Lockout Voltage	Falling Edge, Hysteresis = 1%		3.6		4.2	
V_L/FB_5 Switchover Voltage	Rising Edge of FB_5, Hysteresis = 1%		4.2		4.7	
REF Output Voltage	No External Load[b]		3.24		3.36	
REF Fault Lockout Voltage	Falling Edge		2.4		3.2	
REF Load Regulation	0 mA < I_L < 5 mA[d]			30	75	mV

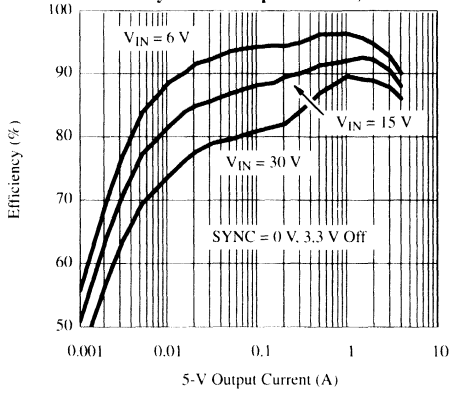
Specifications

Parameter	Test Conditions Unless Otherwise Specified V+ = 15 V, I_{VL} = I_{REF} = 0 mA $\overline{SHDN}$ = ON_3 = ON_5 = 5 V Other Digital Input Levels 0 V or 5 V T_A = T_{MIN} to T_{MAX}	Limits Min[a]	Typ[c]	Max[a]	Unit
Internal Regulator and Reference (Cont'd)					
V+ Shutdown Current	$\overline{SHDN}$ = ON_3 = ON_5 = 0 V, V+ = 30 V		25	40	µA
V+ Standby Current	ON_3 = ON_5 = 0 V, V+ = 30 V		70	110	
Quiescent Power Consumption (both PWM controllers on)	FB_5 = CS_5 = 5.25 V FB_3 = CS_3 = 3.5 V		5.5	8.6	mW
V+ Off Current	FB_5 = CS_5 = 5.25 V, V_L Switched Over to FB_5		30	60	µA
Oscillator and Inputs/Outputs					
Oscillator Frequency	SYNC = 3.3 V	270	300	330	kHz
	SYNC = 0 V, 5 V	170	200	230	
SYNC High Pulse Width		200			ns
SYNC Low Pulse Width		200			
SYNC Rise/Fall Time	Not Tested			200	
Oscillator SYNC Range		240		350	kHz
Maximum Duty Cycle	SYNC = 3.3 V	89	92		%
	SYNC = 0 V, 5 V	92	95		
Input Low Voltage	$\overline{SHDN}$, ON_3, ON_5 SYNC			0.8	V
Input High Voltage	$\overline{SHDN}$, ON_3, ON_5	2.4			
	SYNC	V_L - 0.5 V			
Input Current	$\overline{SHDN}$, ON_3, ON_5 V_{IN} = 0 V, 5 V			± 1	µA
DL_3/DL_5 Sink/Source Current	V_{OUT} = 2 V		1		A
DH_3/DH_5 Sink/Source Current	BST_3 - LX_3 = BST_5 - LX_5 = 4.5 V, V_{OUT} = 2 V		1		
DL_3/DL_5 On-Resistance	High or Low			7	Ω
DH_3/DH_5 On-Resistance	High or Low BST_3 - LX_3 = BST_5 - LX_5 = 4.5 V			7	

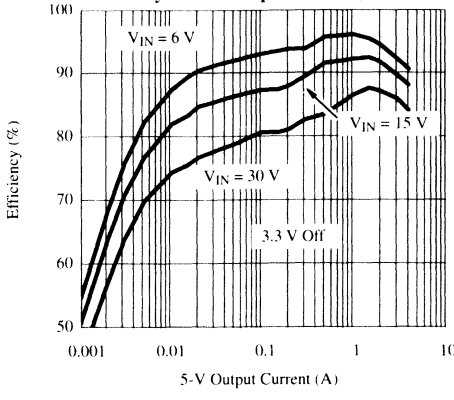
Notes
a. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum.
b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
c. Since the reference uses V_L as its supply, its V+ line regulation error is insignificant.
d. The main switching outputs track the reference voltage. Loading the reference reduces the main outputs slightly according to the closed-loop gain (AV_{CL}) and the reference voltage load-regulation error. AV_{CL} for the 3.3-V supply is unity gain. AV_{CL} for the 5-V supply is 1.54.

Typical Characteristics (25°C Unless Noted)

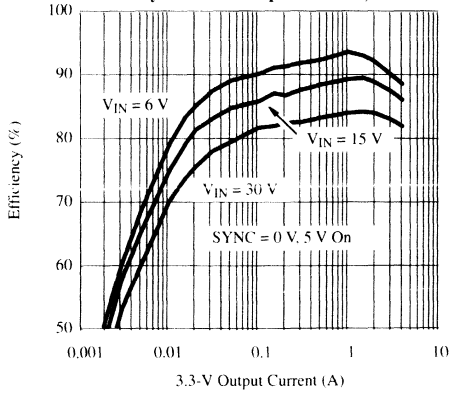
Efficiency vs. 5-V Output Current, 200 kHz



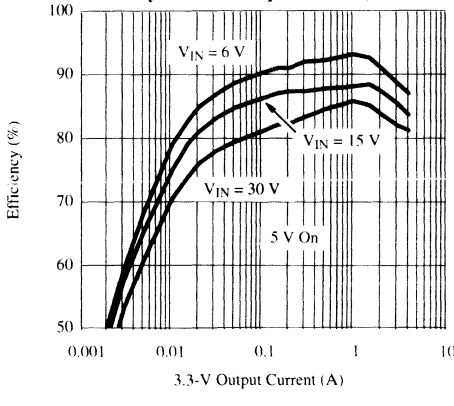
Efficiency vs. 5-V Output Current, 300 kHz



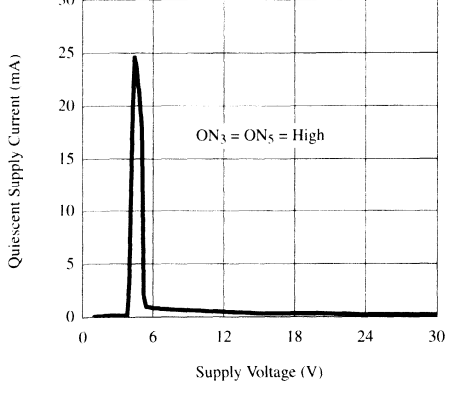
Efficiency vs. 3.3-V Output Current, 200 kHz



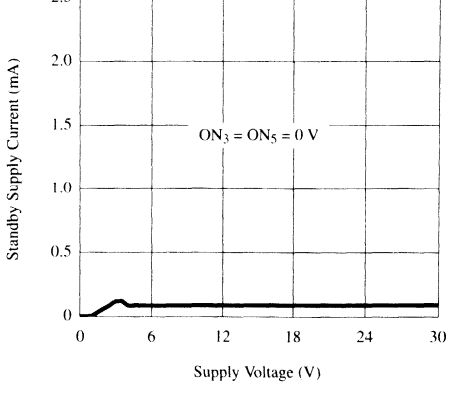
Efficiency vs. 3.3-V Output Current, 300 kHz



Quiescent Supply Current vs. Supply Voltage

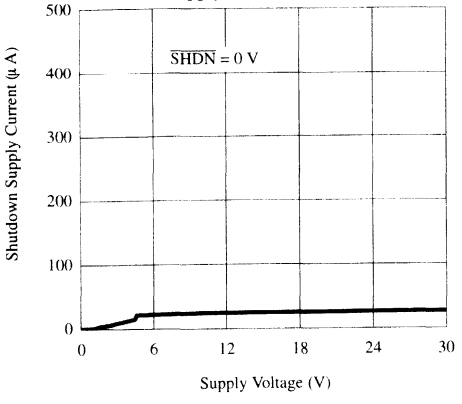


Standby Supply Current vs. Supply Voltage

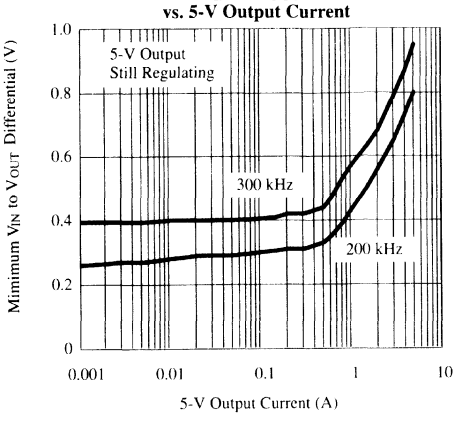


Typical Characteristics (25°C Unless Noted)

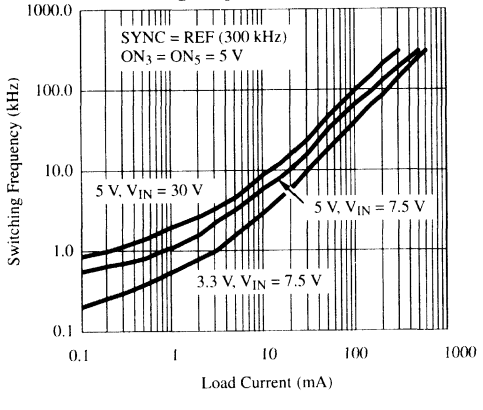
Shutdown Supply Current vs. Supply Voltage



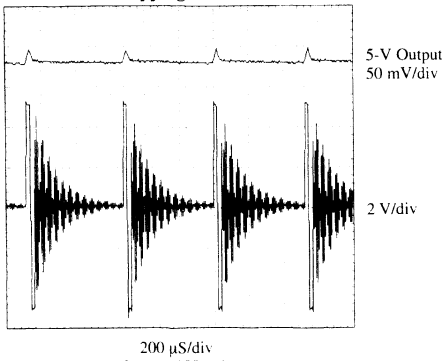
Minimum V_{IN} to V_{OUT} Differential vs. 5-V Output Current



Switching Frequency vs. Load Current

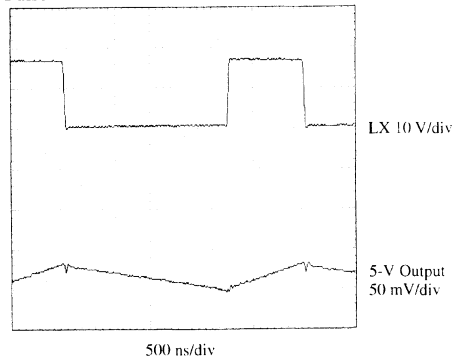


Pulse-Skipping Waveforms



200 μS/div
I_{Load} = 100 mA
V_{IN} = 10 V

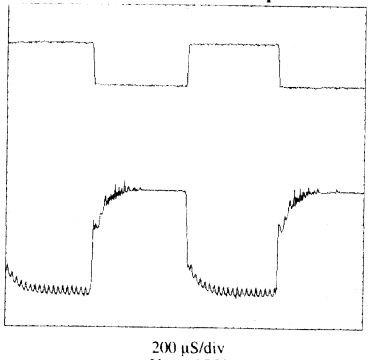
Pulse-Width Modulation Mode Waveforms



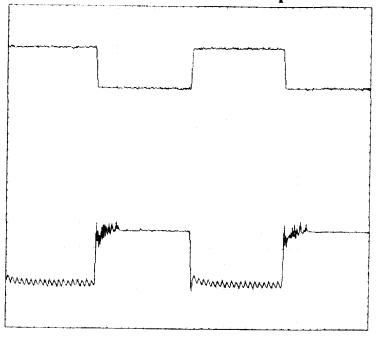
500 ns/div
5-V Output Current = 1 A
V_{IN} = 16 V

Typical Characteristics (25°C Unless Noted)

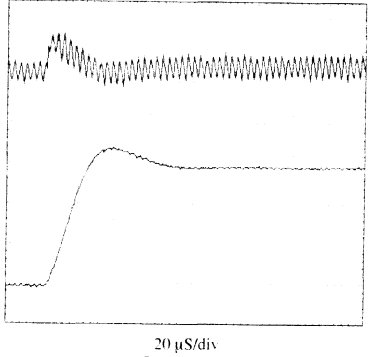
5-V Load-Transient Response



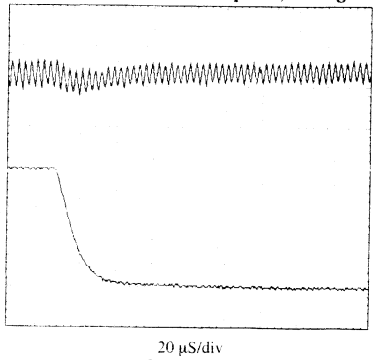
3.3-V Load-Transient Response



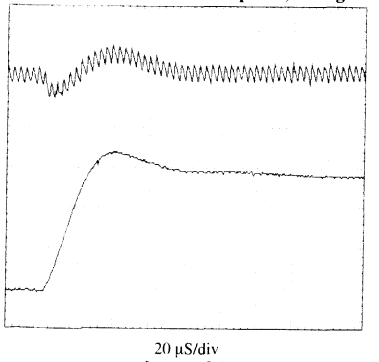
5-V Line-Transient Response, Rising



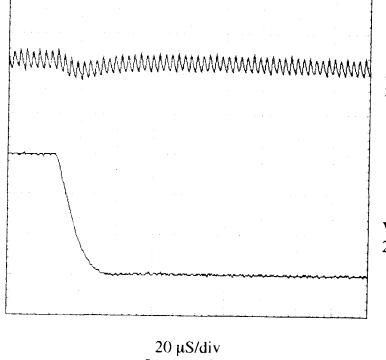
5-V Line-Transient Response, Falling



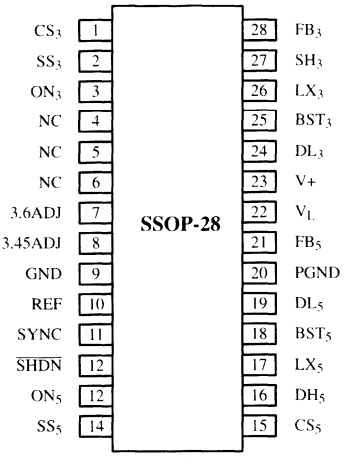
3.3-V Line-Transient Response, Rising



3.3-V Line-Transient Response, Falling



Pin Configuration



Top View

Ordering Information

Part Number	Temperature Range	V_{OUT}
Si9130CG	0 to 70°C	5 V and 3.3 V, 3.45 V, or 3.6 V
*Si9130LG	–10° to 90°C	

*Pre–Release Information

Demo Board	Temperature Range	Board Type
Si9130DB	0 to 70°C	Surface Mount

Pin Number	Symbol	Description
1	CS_3	Current-sense input for 3.3-V Buck controller—this pins over current threshold is 100 mV with respect to FB_3.
2	SS_3	Soft-start input for 3.3 V. Connect capacitor from SS_3 to GND.
3	ON_3	ON/$\overline{OFF}$ logic input disables the 3.3-V Buck controller. Connect directly to V_L for automatic turn-on.
4	NC	Not internally connected.
5	NC	Not internally connected.
6	NC	Not internally connected.
7	3.6ADJ	Control input to select 3.6-V output. See Voltage Selection Table for input and output combinations.
8	3.45ADJ	Control input to select 3.45-V output. See Voltage Selection Table for input and output combinations.
9	GND	Analog ground.
10	REF	3.3-V reference output. Supplies external loads up to 5 mA.
11	SYNC	Oscillator control/synchronization input. Connect capacitor to GND, 1-µF/mA output or 0.22 µF minimum. For external clock synchronization, a rising edge starts a new cycle to start. To use internal 200-kHz oscillator, connect to VL or GND. For 300-kHz oscillator, connect to REF.
12	$\overline{SHDN}$	Shutdown logic input, active low. Connect to V_L for automatic turn-on. The 5-V V_L supply will not be disabled in shutdown allowing connection to $\overline{SHDN}$.
13	ON_5	ON/$\overline{OFF}$ logic input disables the 5-V Buck Controller. Connect to V_L for automatic turn-on.
14	SS_5	Soft-start control input for 5 V Buck controller. Connect capacitor from SS_5 to GND.
15	CS_5	Current-sense input for 5 V Buck controller—this pins over current threshold is 100 mV referenced to FB_3.
16	DH_5	Gate-drive output for the 5-V supply high-side n-channel MOSFET.
17	LX_5	Inductor connection for the 5-V supply.
18	BST_5	Boost capacitor connection for the 5-V supply.
19	DL_5	Gate-drive output for the 5-V supply rectifying n-channel MOSFET.

New Product

Pin Configuration (Cont'd)

Pin Number	Symbol	Description
20	PGND	Power Ground.
21	FB_5	Feedback input for the 5-V Buck controller.
22	V_L	5-V logic supply voltage for internal circuitry—able to source 5-mA external loads. V_L remains on with valid voltage at V+.
23	V+	Supply voltage input.
24	DL_3	Gate-drive output for the 3.3-V supply rectifying n-channel MOSFET.
25	BST_3	Boost capacitor connection for the 3.3-V supply.
26	LX_3	Inductor connection for the 3.3-V supply.
27	DH_3	Gate-drive output for the 3.3-V supply high-side n-channel MOSFET.
28	FB_3	Feedback input for the 3.3-V Buck controller.

Voltage Selection Table

Input		Output
3.45ADJ	**3.6ADJ**	**FB_3**
OPEN	OPEN	3.3 V
GND	OPEN	3.45 V
OPEN	GND	3.6 V

Description of Operation

The Si9130 is a dual step-down converter, which takes a 5.5-V to 30-V input and supplies power via two PWM controllers (see Figure 1). These 5-V and 3.3-V supplies run on an optional 300-kHz or 200-kHz internal oscillator, or an external sync signal. Amount of output current is limited by external components, but can deliver greater than 6 A on either supply. As well as these two main Buck controllers, additional loads can be driven from two micropower linear regulators, one 5 V (V_L) and the other 3.3 V (REF)—see Figure 2. These supplies are each rated to deliver 5 mA. If the linear regulator circuits fall out of regulation, both Buck controllers are shut down.

3.3-V PWM Voltage Selection (Pins 3.45ADJ, 3.6ADJ)

The voltage at this output can be selected to 3.3 V, 3.45 V or 3.6 V, depending on the configuration of pins 3.45ADJ and 3.6ADJ. Leaving both pins open results in 3.3V nominal output. Grounding pin 3.45ADJ while leaving 3.6ADJ open delivers 3.45-V nominal output. Grounding 3.6 ADJ while leaving 3.45ADJ open sets a 3.6-V nominal output.

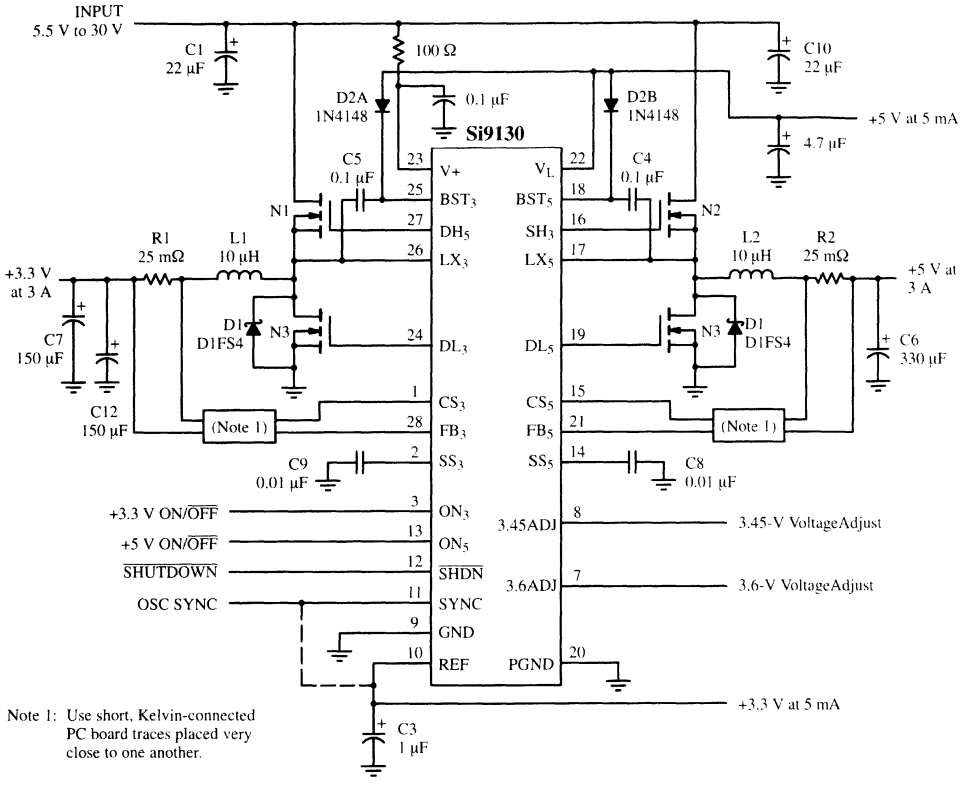


Figure 1. Si9130 Application Circuit

3.3-V Switching Supply

The 3.3-V supply is regulated by a current-mode PWM controller in conjunction with several externals: two n-channel MOSFETs, a rectifier, an inductor and output capacitors (see Figure 1). The gate drive supplied by DH_3 needs to be greater than V_L, so it is provided by the bootstrap circuit consisting of a 100-nF capacitor and diode connected to BST3.

A low-side switching MOSFET connected to DL_3 increases efficiency by reducing the voltage across the rectifier diode. A low value sense resistor in series with the inductor sets the maximum current limit, to disallow current overloads at power-on or in short-circuit situations.

The soft-start feature on the Si9130 is capacitor programmable; pin SS_3 functions as a constant current source to the external capacitor connected to GND. Excess currents at power-on are avoided, and power-supplies can be sequenced with different turn-on delay times by selecting the correct capacitor value.

5-V Switching Supply

The 5-V supply is regulated by a current-mode PWM controller which is nearly the same as the 3.3-V output. The dropout voltage across the 5-V supply, as shown in the schematic in Figure 1, is 400 mV (typ) at 2 A. If the voltage at V+ falls, nearing 5 V, the 5-V supply will lower as well, until the V_L linear regulator output falls below the 4-V undervoltage lockout threshold. Below this threshold, the 5-V controller is shut off.

The frequency of both PWM controllers is set at 300 kHz when the SYNC pin is tied to REF. Connecting SYNC to either GND or V_L sets the frequency at 200 kHz.

3.3-V and 5-V Switching Controllers

Each PWM controller on the Si9130 is identical with the exception of the preset output voltages. The controllers only share three functional blocks (see Figure 3): the oscillator, the voltage reference (REF) and the 5-V logic supply (V_L). The 3.3-V and 5-V controllers are independently enabled with pins ON_3 and ON_5, respectively. The PWMs are a direct-summing type, without the typical integrating error amplifier along with the phase shift which is a side effect of this type of topology. Feedback compensation is not needed, as long as the output capacitance and its ESR requirements are met, according to the *Design Considerations* section of this data sheet.

The main PWM comparator is an open loop device which is comprised of three comparators summing four signals: the feedback voltage error signal, current sense signal, slope-compensation ramp and voltage reference as shown in Figure 3. This method of control comes closer to the ideal of maintaining the output voltage on a cycle-by-cycle basis. When the load demands high current levels, the controller is in full PWM mode. Every cycle from the oscillator asserts the output latch and drives the gate of the high-side MOSFET for a period determined by the duty cycle (approximately $V_{OU}T/V_{IN}$ × 100%) and the frequency.

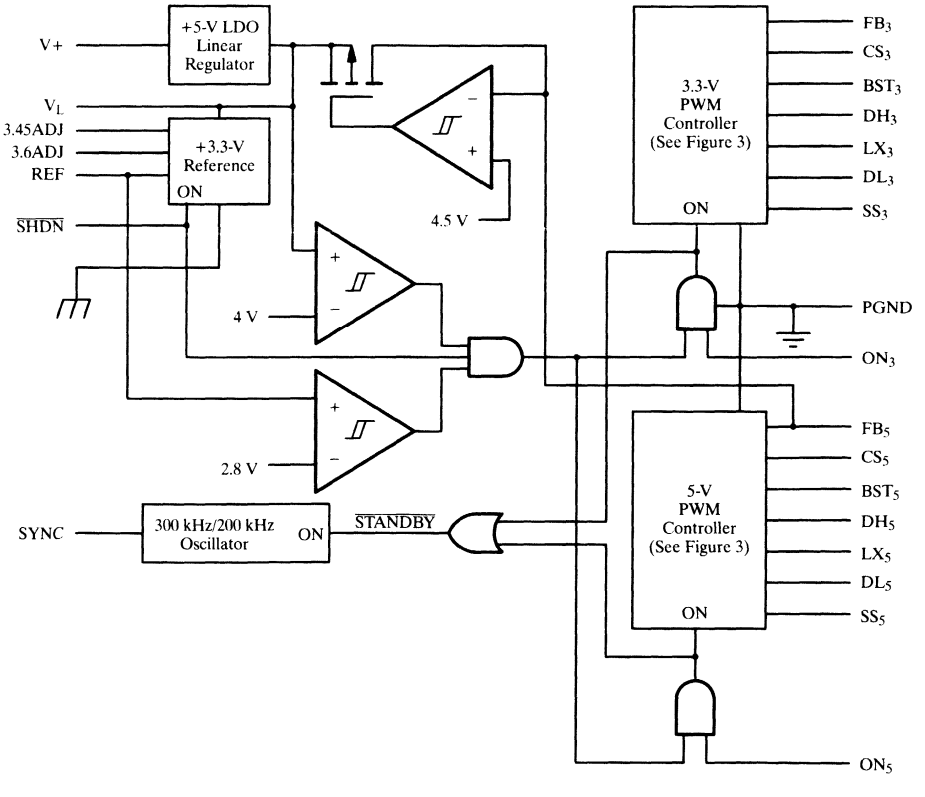


Figure 2. Si9130 Block Diagram

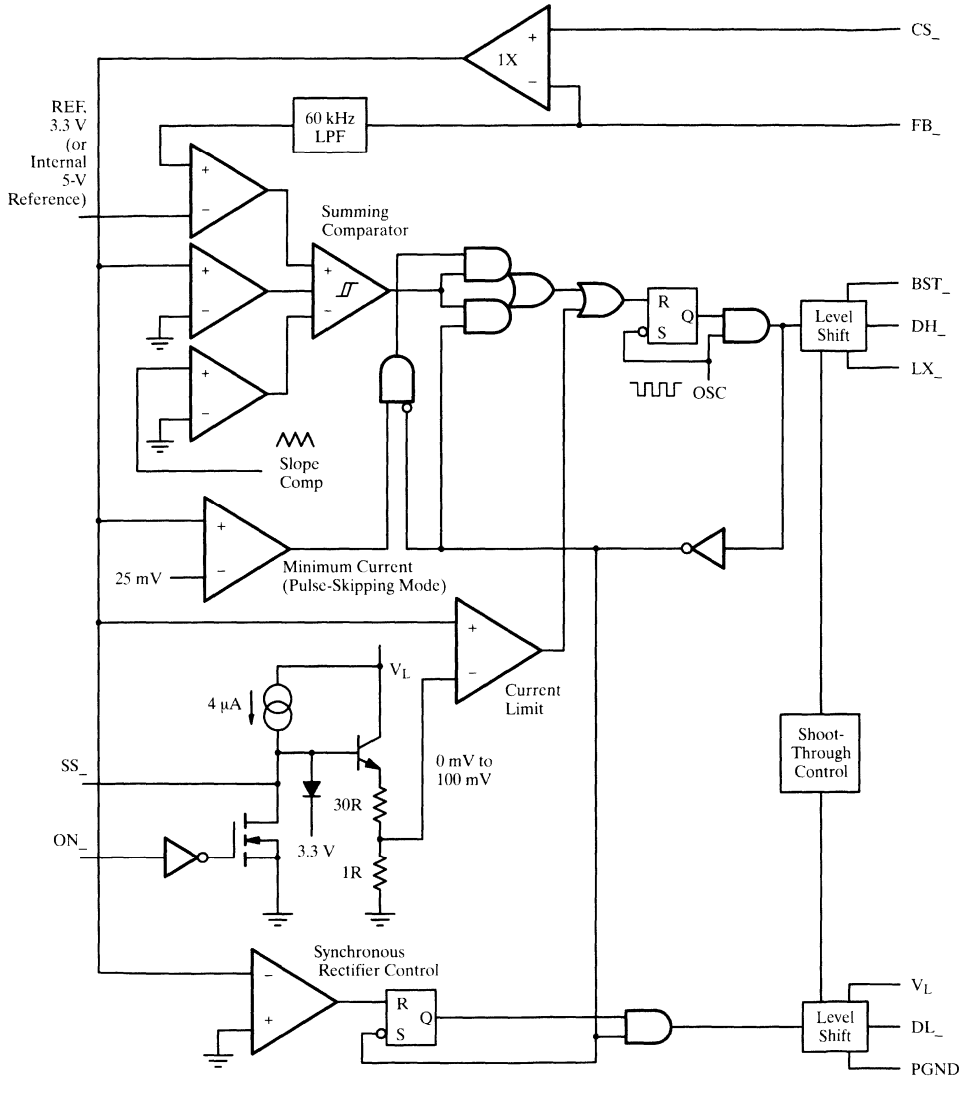


Figure 3. Si9130 Controller Block Diagram

The high-side switch turns off, setting the synchronous rectifier latch and 60 ns later, the rectifier MOSFET turns on. The low-side switch stays on until the start of the next clock cycle in continuous mode, or until the inductor current becomes positive again, in discontinuous mode.

In over-current situations, where the inductor current is greater than the 100-mV current-limit threshold, the high-side latch is reset and the high-side gate drive is shut off.

During low-current load requirements, the inductor current will not deliver the 25-mV minimum current threshold. The Minimum Current comparator signals the PWM to enter pulse-skipping mode when the threshold has not been reached. pulse-skipping mode skips pulses to reduce switching losses, the losses which decrease efficiency the most at light load. Entering this mode causes the minimum current comparator to reset the high-side latch at the beginning of each oscillator cycle.

Soft-Start

To slowly bring up the 3.3-V and 5-V supplies, connect capacitors from SS_3 and SS_5 to GND. Asserting ON_3 or ON_5 starts a 4-A constant current source to charge these capacitors to 4 V. As the voltage on these pins ramps up, so does the current limit comparator threshold, to increase the duty cycle of the MOSFETs to their maximum level. If ON_3 or ON_5 are left low, the respective capacitor is discharged to GND. Leaving the SS_3 or SS_5 pins open will cause either controller to reach the terminal over-current level within 10 µs.

Soft start helps prevent current spikes at turn-on and allows separate supplies to be delayed using external programmability.

Synchronous Rectifiers

Synchronous rectification replaces the Schottky rectifier with a MOSFET, which can be controlled to increase the efficiency of the circuit.

When the high-side MOSFET is switched off, the inductor will try to maintain its current flow, inverting the inductor's polarity. The path of current then becomes the circuit made of the Schottky diode, inductor and load, which will charge the output capacitor. The diode has a 0.5-V forward voltage drop, which contributes a significant amount of power loss, decreasing efficiency. A low-side switch is placed in parallel with the Schottky diode and is turned on just after the diode begins to conduct. Because the $r_{DS(ON)}$ of the MOSFET is low, the I*R voltage drop will not be as large as the diode, which increases efficiency.

The low-side rectifier is shut off when the inductor current drops to zero.

Shoot-through current is the result when both the high-side and rectifying MOSFETs are turned on at the same time. Break-before-make timing internal to the Si9130 manages this potential problem. During the time when neither MOSFET is on, the Schottky is conducting, so that the body diode in the low-side MOSFET is not forced to conduct.

Synchronous rectification is always active when the Si9130 is powered-up, regardless of the operational mode.

Gate-Driver Boost

The high-side n-channel drive is supplied by a flying-capacitor boost circuit (see Figure 4). The capacitor takes a charge from V_L and then is connected from gate to source of the high-side MOSFET to provide gate enhancement. At power-up, the low-side MOSFET pulls LX_ down to GND and charges the BST_ capacitor connected to 5 V. During the second half of the oscillator cycle, the controller drives the gate of the high-side MOSFET by internally connecting node BST_ to DH_. This supplies a voltage 5 V higher than the battery voltage to the gate of the high-side MOSFET.

Oscillations on the gates of the high-side MOSFET in discontinuous mode are a natural occurrence caused by the LC network formed by the inductor and stray capacitance at the LX_ pins. The negative side of the BST_ capacitor is connected to the LX_ node, so ringing at the inductor is translated through to the gate drive.

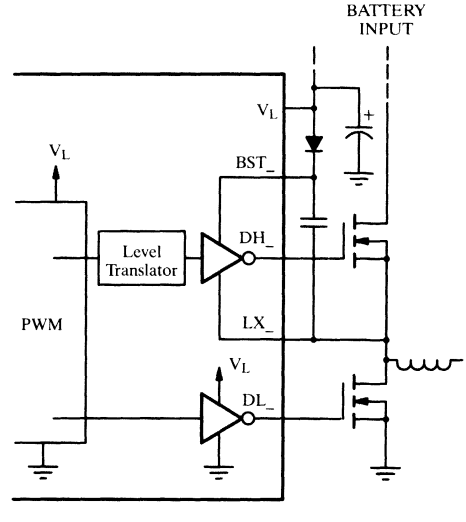


Figure 4. Boost Supply for Gate Drivers

Operational Modes

PWM Mode

The 3.3-V and 5-V Buck controllers operate in continuous-current PWM mode when the load demands more than approximately 25% of the maximum current (see typical curves). The duty cycle can be approximated as Duty_Cycle = V_{OUT}/V_{IN}.

In this mode, the inductor current is continuous; in the first half of the cycle, the current slopes up when the high-side MOSFET conducts and then, in the second half, slopes back down when the inductor is providing energy to the output capacitor and load. As current enters the inductor in the first half-cycle, it is also continuing through to the load; hence, the load is receiving continuous current from the inductor. By using this method, output ripple is minimized and smaller form-factor inductors can be used. The output capacitor's ESR has the largest effect on output ripple. It is typically under 50mV; the worst case condition is under light load with higher input battery voltage.

Pulse-Skipping Mode

When the load requires less than 25% of its maximum, the Si9130 enters a mode which drives the gate for one clock cycle and skips the majority of the remaining cycles. Pulse-skipping mode cuts down on the switching losses, the dominant power consumer at low current levels.

In the region between pulse-skipping mode and PWM mode, the controller may transition between the two modes, delivering spurts of pulses. This may cause the current waveform to look irregular, but will not overly affect the ripple voltage. Even in this transitioning mode efficiency will stay high.

Current Limit

The current through an external resistor, is constantly monitored to protect against over-current. A low value resistor is placed in series with the inductor. The voltage across it is measured by connecting it between CS_ and FB_. If this voltage is larger than 100 mV, the high-side MOSFET drive is shut down. Eliminating over-currents protects the MOSFET, the load and the power source. Typical values for the sense resistors with a 3-A load will be 25 mΩ.

Oscillator and SYNC

There are two ways to set the Si9130 oscillator frequency: by using an external SYNC signal, or using the internal oscillator. The SYNC pin can be driven with an external CMOS level signal with frequency from 240 kHz and 350 kHz to synchronize to the internal oscillator. Tying SYNC to either V_L or GND sets the frequency to 200 kHz and to REF sets the frequency to 300 kHz.

Operation at 300 kHz is typically used to minimize output passive component sizes. Slower switching speeds of 200 kHz may be needed for lower input voltages.

Internal V_L and REF

A 5-V linear regulator supplies power to the internal logic circuitry. The regulator is available for external use from pin V_L, able to source 5 mA. A 4.7-µF capacitor should be connected between V_L and GND. To increase efficiency, when the 5-V switching supply has voltage greater than 4.5 V, V_L is internally switched over to the output of the 5-V switching supply and the linear regulator is turned off.

The 5-V linear regulator provides power to the internal 3.3-V bandgap reference (REF). The 3.3-V reference can supply 5 mA to an external load, connected to pin REF. Between REF and GND connect a capacitor, 0.22 µF plus 1 µF per mA of load current. The switching outputs will vary with the reference; therefore, placing a load on the REF pin will cause the main outputs to decrease slightly, within the specified regulation tolerance.

V_L and REF supplies stay on as long as V+ is greater than 4.5 V, even if the switching supplies are not enabled. This feature is necessary when using the micropower regulators to keep memory alive during shutdown.

Both linear regulators can be connected to their respective switching supply outputs. For example, REF would be tied to the output of the 3.3 V and V_L to 5 V. This will keep the main supplies up in standby mode, provided that each load current in shutdown is not larger than 5 mA.

Fault Protection

The 3.3-V and 5-V switching controllers are shut down when one of the linear regulators drops below 85% of its nominal value; that is, shut down will occur when $V_L < 4.0$ V or REF < 2.8 V.

Design Considerations

Inductor Design

Three specifications are required for inductor design: inductance (L), peak inductor current (I_{LPEAK}), and coil resistance (R_L). The equation for computing inductance is:

$$L = \frac{(V_{OUT})(V_{IN(MAX)}-V_{OUT})}{(V_{IN(MAX)})(f)(I_{OUT})(LIR)}$$

Where: V_{OUT} = Output voltage (3.3 V or 5 V);
$V_{IN(MAX)}$ = Maximum input voltage (V);
f = Switching frequency, normally 300 kHz;
I_{OUT} = Maximum dc load current (A);
LIR = Ratio of inductor pea-to-peak ac current to average dc load current, typically 0.3.

When LIR is higher, smaller inductance values are acceptable, at the expense of increased ripple and higher losses.

The peak inductor current (I_{LPEAK}) is equal to the steady-state load current (I_{OUT}) plus one half of the peak-to-peak ac current (I_{LPP}). Typically, a designer will select the ac inductor current to be 30% of the steady-state current, which gives I_{LPEAK} equal to 1.15 times I_{OUT}.

The equation for computing peak inductor current is:

$$I_{LPEAK} = I_{OUT} + \frac{(V_{OUT})(V_{IN(MAX)}-V_{OUT})}{(2)(f)(L)(V_{IN(MAX)})}$$

Output Capacitors

The output capacitors determine loop stability and ripple voltage at the output. In order to maintain stability, minimum capacitance and maximum ESR requirements must be met according to the following equations:

$$C_F > \frac{V_{REF}}{(V_{OUT})(R_{CS})(2)(\pi)(GPWP)}$$

and,

$$ESR_{CF} < \frac{(V_{OUT})(R_{CS})}{V_{REF}}$$

Where: C_F = Output filter capacitance (F)
V_{REF} = Reference voltage, 3.3 V;
V_{OUT} = Output voltage, 3.3 V or 5 V;
R_{CS} = Sense resistor (Ω);
GBWP = Gain-bandwidth product, 60 kHz;
ESR_{CF} = Output filter capacitor ESR (Ω).

Both minimum capacitance and maximum ESR requirements must be met. In order to get the low ESR, a capacitance value two to three times greater than the required minimum may be necessary.

The equation for output ripple in continuous current mode is:

$$V_{OUT(RPL)} = I_{LPP(MAX)} \times \left(ESR_{CF} + \frac{1}{(2 \times f \times CF)}\right)$$

The equations for capacitive and resistive components of the ripple in pulse-skipping mode are:

$$V_{OUT(RPL)}(C) = \frac{(4)(10^{-4})(L)}{(R_{CS}^2)(C_F)} \times \left(\frac{1}{V_{OUT}} + \frac{1}{V_{IN}-V_{OUT}}\right) \text{ Volts}$$

$$V_{OUT(RPL)}(R) = \frac{(0.02)(ESR_{CF})}{R_{CS}} \text{ Volts}$$

The total ripple, $V_{OUT(RPL)}$, can be approximated as follows:

if $V_{OUT(RPL)}(R) < 0.5\ V_{OUT(RPL)}(C)$,
then $V_{OUT(RPL)} = V_{OUT(RPL)}(C)$,
otherwise, $V_{OUT(RPL)} = V_{OUT(RPL)}(C) + V_{OUT(RPL)}(R)$.

Lower Voltage Input

The application circuit shown here can be easily modified to work with 5.5-V to 12-V input voltages. Oscillation frequency should be set at 200 kHz and increase the output capacitance to 660 µF on the 5-V output to maintain stable performance up to 2 A of load current. Operation on the 3.3-V supply will not be affected by this reduced input voltage.

Synchronous Buck Converter Controller

Features

- 6- to 16.5-V Input Range (Si9150CY)
- Voltage-Mode PWM Control
- Low-Current Standby Mode
- Enable Control
- Dual 100-mA Output Drivers
- 2% Band Gap Reference
- Multiple Converters Easily Synchronized
- Over-Current Protection

Description

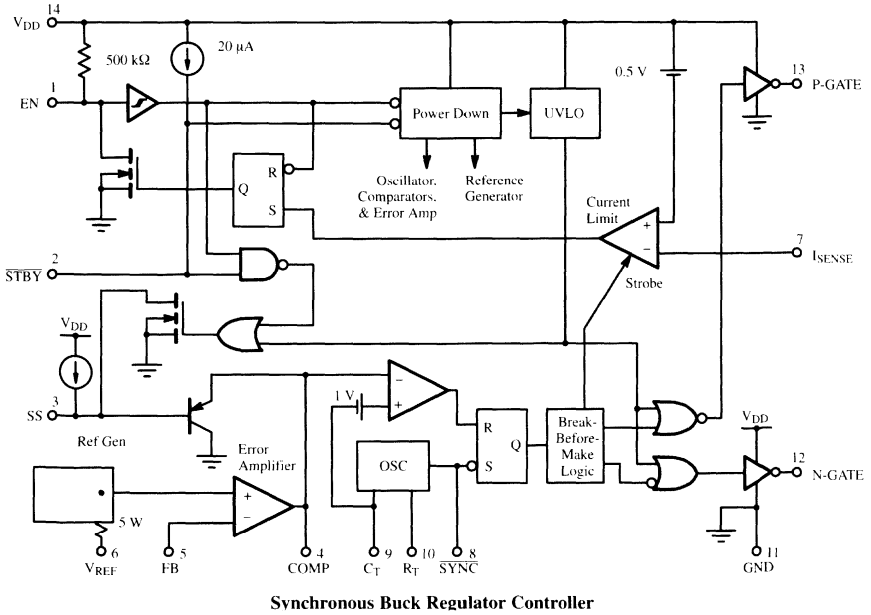
The Si9150 synchronous buck regulator controller is ideally suited for high-efficiency step down converters in battery-powered equipment. Combined with the Si9943DY MOSFET half-bridge, a 90% efficient, 7.5-W, 3.3-V or 5-V power supply can be implemented using standard surface-mount assembly techniques. The wide input range allows operation from NiCd or NiMH battery packs using six to ten cells.

Over-current protection is achieved by sensing the on-state voltage drop across the high side p-channel MOSFET, which eliminates the need for a current sense resistor.

Duty ratios of 0 to 100% and switching frequencies up to 300 kHz are possible. The IC can be disabled by pulling EN low (I_{DD} = 100 µA), or the 2.5-V reference can be maintained, with all other functions disabled, by pulling $\overline{STBY}$ low (I_{DD} = 500 µA).

The Si9150 is available in a 14-pin SOIC and rated for the commercial temperature range of 0 to 70°C (C suffix), and the industrial temperature range of –40 to +85°C (D suffix).

Functional Block Diagram



Synchronous Buck Regulator Controller

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70020.

Absolute Maximum Ratings

Voltages Referenced to GND.
V_{DD} ..... 18 V
I_{SENSE} Input ..... −2 V to V_{DD} +2 V
All Other Inputs ..... −0.3 to V_{DD} + 0.3 V
P-Gate, N-Gate Continuous Source/Sink Current ..... 50 mA
Storage Temperature ..... −65 to 125°C
Operating Junction Temperature ..... 150°C

Power Dissipation (Package)a
14-Pin SOIC (Y Suffix)[b] ..... 900 mW
Thermal Impedance (Θ_{JA})
14-Pin SOIC ..... 140°C/W

Notes
a. Device mounted with all leads soldered or welded to PC board.
b. Derate 7.2 mW/°C.

Specifications[a]

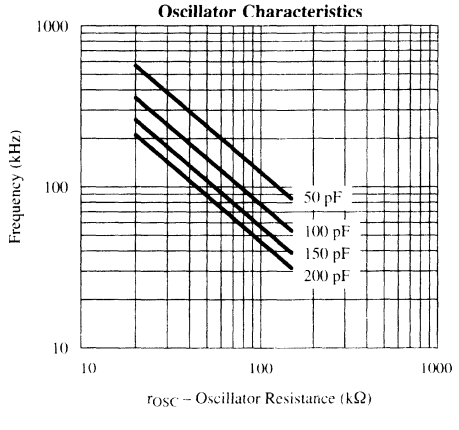
Parameter	Symbol	Test Conditions Unless Otherwise Specified $6.0 \le V_{DD} \le 16.5$ V	Limits C Suffix 0 to 70°C Min[b]	Typ[c]	Max[b]	Limits D Suffix −40 to 85°C Min[b]	Typ[c]	Max[b]	Unit
Reference									
Output Voltage	V_{REF}	T_A = 25°C Measured at Feedback[e] Pin 5	2.45	2.50	2.55	2.45	2.50	2.55	V
		T_{MIN} to T_{MAX}[d]	2.425	2.500	2.575	2.40	2.500	2.60	
Oscillator									
Maximum Frequency	f_{MAX}	C_{OSC} =94.3 pF, R_{OSC} = 28.7 kΩ T_A = 25°C[f]	255	300	345	255	300	345	kHz
Initial Accuracy	f_{OSC}	C_{OSC} =212 pF, R_{OSC} = 41.2 kΩ T_A = 25°C[f]	85	100	115	85	100	115	
Oscillator Ramp Amplitude	V_{OSC}	T_A = 25°C, 100 kHz	2.05	2.65	2.85	2.05	2.65	2.85	V
Temperature Stability[d]	f_{TEMP}	V_{DD} = 10 V, T_{MIN} to T_{MAX}	−5	±3	+5	−6	±4	+6	%
Error Amplifier									
Input BIAS Current	I_B	$V_{FB} = V_{REF}$		25	500		25	750	nA
Open Loop Voltage Gain[d]	A_{VOL}		60	72		58	72		dB
Offset Voltage	V_{OS}			10	25		10	30	mV
Unity Gain Bandwidth[d]	BW		1	1.5		1	1.5		MHz
Output Current	I_{OUT}	Source, V_{COMP} = 2.50 V		−0.30	−0.20		−0.30	−0.15	mA
		Sink, V_{COMP} = 1.0 V	1	2.5		0.9	2.5		
Power Supply Rejection	PSRR		50	70		48	70		dB
Protection									
Current Limit Threshold Voltage	V_{CL}	T_A = 25°C, V_{DD} = 10 V	0.43	0.49	0.55	0.43	0.49	0.55	V
Current Limit Delay to Output[d]	t_d	T_A = 25°C		500	1000		500	1000	ns
Undervoltage Lockout Voltage	V_{UVLO}	Upper Threshold	5.4	5.7	6.0	5.38	5.7	6.01	V
Undervoltage Hysteresis	V_{HYS}		0.10	0.17	0.25	0.10	0.17	0.26	
Softstart Pull-Up Current	I_{SS}			20			20		µA
Supply									
Supply Current (Enable Low)	I_{OFF}			60	100		60	100	µA
Supply Current (Enable High)	I_{CC}	C_L = 0 pF, f_{OSC} = 100 kHz V_{DD} = 10 V		2.2	3.0		2.2	3.0	mA
Supply Current ($\overline{STBY}$ Low)	I_{SB}			300	500		300	550	µA

Specifications[a]

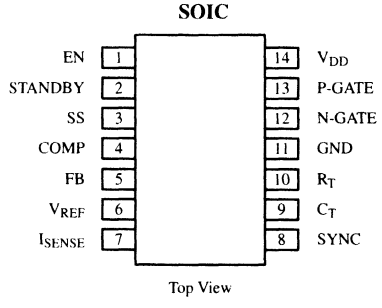
Parameter	Symbol	Test Conditions Unless Otherwise Specified 6.0 ≤ V_{DD} ≤ 16.5 V	Limits C Suffix 0 to 70°C			Limits D Suffix –40 to 85°C			Unit
			Min[b]	Typ[c]	Max[b]	Min[b]	Typ[c]	Max[b]	
Output									
Output High Voltage	V_{OH}	I_{OUT} = 10 mA, V_{DD} = 10 V	9.75			9.7			V
Output Low Voltage	V_{OL}	I_{OUT} = –10 mA, V_{DD} = 10 V			0.25			0.3	
Output Resistance	R_{OUT}	I_{OUT} = 100 mA, V_{DD} = 10 V		10	20		10	25	Ω
Rise Time[d]	t_r	C_L = 800 pF, V_{DD} = 10 V		30	60		30	70	ns
Fall Time[d]	t_f			30	60		30	70	
Logic									
Delay to Output	$t_{d(EN)}$	Transition High to Low		0.25	1		0.25	1	µs
Enable Pull-Up Resistance	R_{EN}			500			500		kΩ
$\overline{STBY}$ Pull-Up Current	$I_{\overline{STBY}}$	T_A = 25°C, $V_{\overline{STBY}}$ = 0 V V_{DD} = 10 V	–25	–20	–15	–28	–20	–12	µA
Turn-On Threshold	V_{ENH}	V_{DD} = 10 V, Rising Input Voltage	6	6.8	8	6	6.8	8	V
Turn-Off Threshold	V_{ENL}	V_{DD} = 10 V, Falling Input Voltage	2	3.75	5	2	3.75	5	

Notes
a. Refer to PROCESS OPTION FLOWCHART for additional information.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. Guaranteed by design, not subject to production test.
e. The voltage reference is trimmed with the feedback (Pin 5) connected to compensation (Pin 4) so that the effect of the error amplifier's input offset voltage is eliminated.
f. C_{OSC} includes the PC board's parasitic capacitance.

Typical Characteristics



Pin Configuration



Pin Description

Pin 1: EN

When this pin is low, the IC is shut down. After a low signal is applied to EN, then COMP, REF, R_T, and C_T settle toward ground; N-GATE, $\overline{STBY}$ and Soft-Start are grounded; and P-GATE is pulled high. The current consumption is no more than 100 µA in this state. This input's threshold has substantial hysteresis so that a capacitor to GND can be used to delay restart after the current limit is activated. After V_{ENH} is exceeded, one clock cycle elapses before N-GATE and P-GATE are enabled. EN is pulled up to V_{DD} through a 500-k resistor and is pulled down internally when the current limit is triggered.

Pin 2: $\overline{STBY}$

Has a function similar to EN. The differences are that the EN pin is unaffected, that the reference is still available, that bias currents are still present internally, and that this pin's pull up current is present. This pin should be used to disable an application if the reference voltage is still needed.

Pin 3: Soft-Start (SS)

This pin limits the maximum voltage that the error amplifier can output. A capacitor between this pin and ground will limit the rate at which the duty factor can increase during initial power up, during a restart when EN or $\overline{STBY}$ goes high, or after the current limit is triggered. A capacitor here can prevent an application from triggering the Si9150's current limit during startup. Soft-Start is pulled low if either EN or $\overline{STBY}$ is low.

Pin 4: Compensation (COMP)

This pin is tied directly to the output of the error amplifier. The feedback network which insures the stability of an application uses this pin. COMP settles low when either EN or $\overline{STBY}$ is pulled low.

Pin 5: Feedback (FB)

This pin is attached directly to the inverting input of the error amplifier. This pin is used to regulate the power supply's output voltage.

Pin 6: Reference (V_{REF})

The internal 2.5-V reference generator is attached to this pin through a 5-Ω resistor. A 0.1-µF bypass capacitor is needed to suppress noise. Also note that the generator has an open emitter; it will not pull down. The maximum current that the generator will source before it current limits is about 10 mA. Many parts of the IC use this voltage, so it is important not to overload the reference generator.

Pin 7: I_{SENSE}

This pin should be attached to the switched node (the drains of the application's p-channel and n-channel MOSFETs). If the voltage between V_{DD} and this pin is more then 0.46 V while the P-GATE is low, the current limit is activated. The current limit is relatively slow to prevent false triggering due to noise. Activating the current limit causes EN to be pulled to GND. I_{SENSE} may be operated from V_{DD} + 2 V to GND – 2 V.

Pin 8: $\overline{SYNC}$

This pin forces the clock to reset when low, and is also pulled low when the clock resets itself. Thus if several Si9150's have their sync pins shorted together, they will be synchronized; the shortest duration clock will control the other clocks.

Pin Description (Cont'd)

Pin 9: C_T

A capacitor from this pin to ground is charged until it reaches 2.5 V, at which point the capacitor is rapidly discharged. The resulting sawtooth with about 1 V added is compared to the input voltage at COMP to determine whether P-GATE and N-GATE should be high or low. The maximum recommended value for C_{OSC} is 200 pF (See Typical Characteristics). The capacitor's charging current is controlled by Pin 10, R_T.

Pin 10: R_T

The IC applies 2.5 V to this pin, and the current is mirrored and applied to Pin 9 while charging the capacitor. The minimum recommended value of R_{OSC} is 20 kΩ (Figure 1).

Pin 11: GND

Since the Si9150 has a high-side current limit, it is important that V_{DD} track the voltage on the source of the p-channel power MOSFET. For noise immunity, it is best to separate the logic ground from the power ground. The logic ground should be decoupled to V_{DD} through at least a 1-µF capacitor. The two grounds may be connected by a path that is long compared to the the path from V_{DD} to the source of the application's p-channel MOSFET.

Pin 12: N-GATE

This pin is used to drive the application's n-channel MOSFET. When turning the n-channel MOSFET off, the p-channel MOSFET will not be turned on until N-GATE is within a few volts of ground. This pin is low while either EN or $\overline{\text{STBY}}$ is low.

Pin 13: P-GATE

This pin is used to drive the application's p-channel MOSFET. The break before make circuitry for the P-GATE is complimentary to that for the N-GATE. This pin is high while either EN or $\overline{\text{STBY}}$ is low.

Pin 14: V_{DD}

This pin powers the IC. The connection between this pin and the source of the p-channel FET should be as short as practical. Read Pin 11's description for bypassing suggestions.

Applications

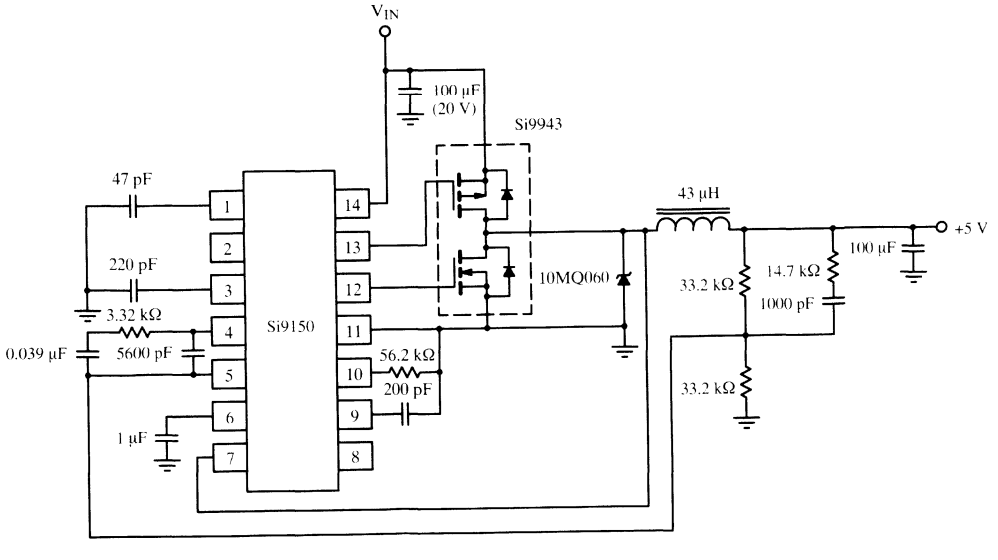


Figure 1. Typical Application Circuit

High-Efficiency Buck Converter for Notebook Computers

Robert Blattner

Introduction

Today, the untethering of electronic equipment has given rise to the need for lightweight power sources and power regulation. Extremely efficient buck converters answer one part of this need. The low losses of these converters eliminate the need for heavy heat sinks and power device packaging. In addition, the energy that is normally consumed by the power converter is available for the application.

In this application note, we present a dc-to-dc converter which is intended for use in notebook computers and other portable products. This converter is designed for maximum efficiency, which is made possible by two innovations—lossless current sensing and synchronous rectification. The converter is rated for a load current of 1.5 A and achieves a maximum efficiency of 94% while producing 400 mA at 3.3 V with input voltage of 6 V. The same design was also configured to produce 5 V. 97% efficiency was achieved with input of 6 V, output of 5 V, and output current of 400 mA. The total PCB area is about 2.25 in.^{2}, with a height of 0.25 in. All components except the inductor use surface-mount packages. Furthermore, there are no lead-formed TO-220s or DPAKs, which results in very light weight and small size.

Si9150CY IC Description

The Si9150CY is a BiCMOS PWM controller IC with all active components necessary for a synchronous buck converter. It is designed to be used with the LITTLE FOOT® series of low-voltage MOSFETs.

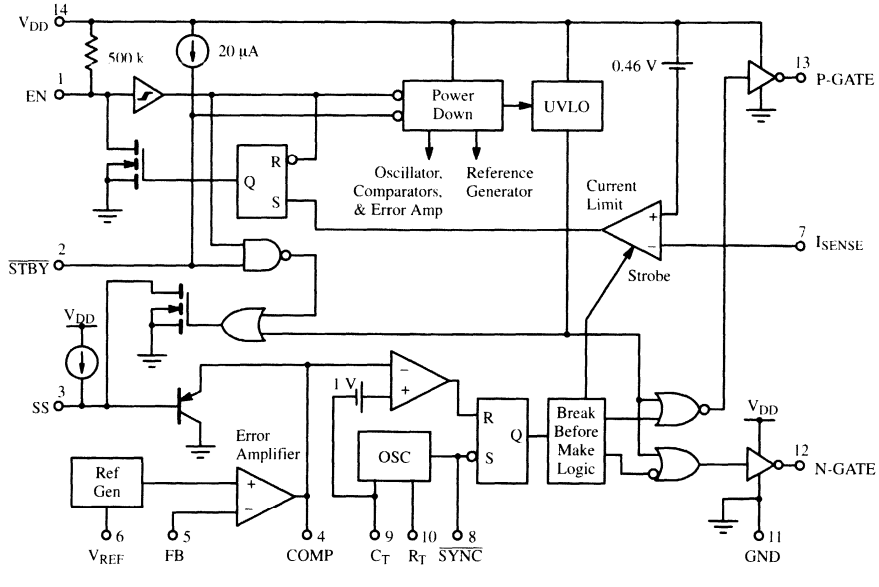


Figure 1. Si9150CY Block Diagram

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By using higher cell densities (2.5 to 3 million cells per square inch), both the high-side MOSFET switch and the synchronous rectifier (SR) can be housed in a single 8-pin small-outline IC package. While an n-channel MOSFET is the obvious choice for the ground-referenced SR, either p- or n-channel MOSFETs can be used for the high-side switch. N-channel MOSFETs require charge pump and/or bootstrap circuits to generate sufficient gate voltage for channel enhancement. P-channel devices are simple to drive but have higher on-resistance for a given die size. Because of recent improvements in p-channel MOSFET designs, the p-channel approach was chosen for its simplicity. The Si9943 includes a 160-mΩ p-channel and a 100-mΩ n-channel MOSFET in an SOIC-8 package. The Si9150CY controller is housed in a 14-pin SOIC.

Since a pin-by-pin description of the Si9150CY is included in its data sheet, we limit this discussion to some interesting details of the functional blocks.

Break-Before-Make

To prevent shoot-through it is essential to turn off one MOSFET before turning on the opposing MOSFET. The Si9150CY senses the voltages on the N-GATE and P-GATE pins. N-GATE will not be pulled high until P-GATE is within a few volts of V_{DD}. Likewise, P-GATE will not be pulled down until N-GATE is a few volts above GND. The thresholds are determined by using asymmetrical CMOS inverters, i.e., one transistor is significantly larger than the other, so that the logic threshold becomes the gate-to-source threshold of the larger device. There is also a delay while the signal, once enabled, is buffered by the output drivers. This delay is typically 75 to 100 ns. The total deadtime (both MOSFETs off) is equal to about 150 ns.

Current Limit

The current limit is a strobed slow-acting comparator which monitors the drain of the p-channel MOSFET. It is triggered when the voltage on the V_{DD} pin minus that on the I_{SENSE} pin is greater than 0.46-V typical, provided that the P-GATE pin has been pulled below about 1.5 V. Once the current limit is triggered, the EN pin is pulled low until the IC shuts down, resetting the dc-to-dc converter and the current limit. The comparator is relatively slow, allowing about 400 ns for the system to settle down after the p-channel MOSFET has turned on. Once the p-channel MOSFET is driven on, it appears in the circuit as a drain-to-source resistance. By using this resistor to sense the current, additional resistors or current transformers are eliminated. This reduces both cost and losses, making it possible to achieve extremely high efficiency. It does, however, restrict the current limit trip point, which is now determined by the MOSFET on-resistance.

Oscillator

The oscillator works by applying 2.5 V to the R_T pin. The current flowing out of the R_T pin is mirrored and fed into the C_T pin. When the C_T pin reaches 2.5 V, an internal MOSFET pulls the $\overline{SYNC}$ pin low. The low voltage on $\overline{SYNC}$ causes the C_T pin to be pulled low, resetting the clock. Allowing for small offset voltages, the frequency, f, is

$$f = \frac{0.9}{C_{OSC} \times R_{OSC}} \quad (1)$$

where C_{OSC} and R_{OSC} are the capacitor and resistor values tied to the C_T and R_T pins, respectively.

The $\overline{SYNC}$ voltage is also passed through three inverters to square the edges, and the signal is used to reset the PWM circuitry in the IC. Since the clock resets whenever the $\overline{SYNC}$ pin is pulled low, two Si9150CYs can be synchronized by connecting their $\overline{SYNC}$ pins together. If synchronization to an external clock is desired, $\overline{SYNC}$ should be pulled low for a short period using a 2N7002 or similar MOSFET. The recommended reset pulsewidth is approximately 100 ns.

Reference Generator

The reference generator is a temperature-compensated bandgap, which is powered whenever the EN pin is high. The output from the bandgap is run through a trimmed voltage divider to an amplifier that can source about 10 mA to the V_{REF} pin. If more than 10 mA is drawn from the amplifier, it will shut down momentarily.

The sink current capability is only about 100 µA, however. Since the reference has available more than a hundred times as much pull-up as pull-down current, noise on the power pins is effectively rectified. When this happens, either a dc voltage higher than 2.5 V or a relatively low-frequency sawtooth is present on the V_{REF} pin. Since this voltage is used in all parts of the IC, it will not perform to specification if the reference is out of specification. We recommend bypassing the V_{REF} pin with a minimum capacitor value of 0.1 µF to ground.

Power Down

The power down section of the IC is a group of load switches and switchable current mirrors. With the EN pin high and the $\overline{\text{STBY}}$ pin low, only the reference generator, the UV lockout, and the pull-up for the $\overline{\text{STBY}}$ pin will operate. With both the EN and the $\overline{\text{STBY}}$ pins high, all other systems are switched on. With EN pulled low, only the EN pull-up resistor consumes power.

Under very low load conditions the efficiency of switch mode power converters decreases very rapidly. When it is desirable to operate under light load (<50 mA) for an extended period of time it may be beneficial to implement a linear regulator. With $\overline{\text{STBY}}$ low and EN high, the Si9150CY provides the voltage reference needed for implementation of a linear regulator.

Design Example

The dc-to-dc converter shown in Figure 2 is designed especially for use in notebook computers. With a 6-, 8-, or 10-cell NiCd battery to power the computer, it is necessary to convert a variable voltage to 5 V and 3.3 V.

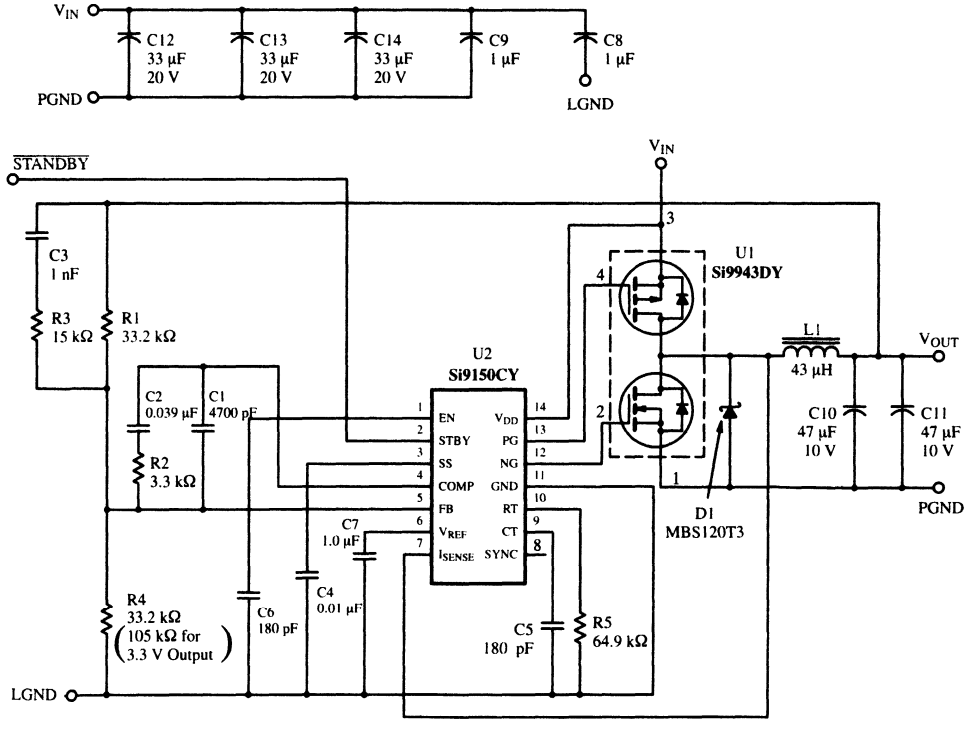


Figure 2. 5-V Synchronous Buck Regulator Schematic

We assumed the use of two converters, one for each output voltage. This duplication increases the component cost somewhat but allows simple implementation of independent regulation and current limits. A typical computer would use about 500 mA at each voltage, but at times would need up to 1.5 A. While weight and efficiency are optimized, cost effectiveness is also kept in mind. The 5-V converter is considered in depth because, in many respects, it is more difficult to design. In order to reconfigure the resulting converter for a 3.3 V output, it is necessary merely to change R4 to 105 kΩ.

Converter Specification

The specifications given in Table 1 are representative of a typical portable application. The current limit has been specified fairly loosely, because most applications will permit it and because the lossless current limit circuit requires a wide current limit spread.

Table 1. DC-to-DC Converter Specifications

Spec	Typ	Min	Max	Unit	Conditions
I_{max}		1.5		A	
I_{CL}	2.1	1.5	5.7	A	T_J < 150°C under fault conditions
$I_{no\ load}$	4		8	mA	
$I_{shutdown}$	300		500	µA	
V_{in}	10	6	16.5	V	
V_{out}	5	4.85	5.15	V	
Step-load	150		300	mV	I_{out} 10% to 90%
Output ripple	40		100	mV_{rms}	V_{in} = 16.5 V
Input ripple	300		400	mV_{rms}	V_{in} = 16.5 V, I_{out} = 1.5 A
Start time	2	1	5	ms	
Efficiency	97	94		%	I_{out} = 0.5 A
Operating temp	25	0	50	°C	
Switching frequency	76	65	85	kHz	

$I_{no\ load}$ is the maximum current that is permissible for the unloaded converter to consume while operating. But this level is too high for a typical computer's shut-down mode, so a linear regulator or small bang-bang converter is assumed to supply power while the computer is shut down. The $I_{shutdown}$ specification is important during this time. I_{max} is the current that the load needs to operate. (Actually, this specification is redundant with minimum I_{cl}, but we include it here for clarity.) The maximum current limit trip point must occur at a current that does not cause safety concerns. Likewise, the output voltage must be within the operating voltage requirements of the load. For most 5-V circuitry, this is 5 V ± 10%. This range must be padded to account for voltage drops and noise generated in the load. The deviation from 5 V can be broken down into dc accuracy, noise, and step-load response. Since, in most designs, the load will not jump from 10% to 90% in a few microseconds, the step-load figure may be divided in half. The load's decoupling capacitors and trace resistances provide an RC filter which smooths the output voltage, allowing the RMS value for output ripple voltage to be used. Thus, the sum of the dc error, half of the step-load response, and the RMS ripple should be less than or equal to about 8% of 5 V. The above explanation is based on rules of thumb and should be scrutinized by the system designer before use. The safest specification uses peak ripple and full step response. Also note that the converter will tend to run a few degrees above the ambient temperature, and it will not be operated while the computer is outside its temperature range.

Design Methodology

A description of the buck converter design procedure is given here. This particular design employs the Si9150CY driving the Si9943DY complementary half-bridge, but other converters can be designed using the same method.

The first step in designing with the Si9150CY is to choose the p-channel MOSFET switch to meet the load current requirements. $r_{DS(on)}$ variations over the spec ranges for voltage and temperature will affect the output current limit trip point, I_{CL}, since $r_{DS(on)}$ is used as the current sensing resistor. Once it is verified that maximum load requirements can be met, the inductor can be designed to meet efficiency and size requirements. In the discussion below, the ripple and power losses are calculated for the surface-mount tantalum capacitors, and some criteria are given for selection of the Schottky diode. An explanation of the feedback network is given, and finally soft-start capacitor selection and board layout considerations are discussed.

Worst-Case Current Limit Calculations

There are three important current limit values that must be considered when choosing the p-channel MOSFET. First, the minimum current at which the current limit will trip (I_{CLmin}). This value is needed to ensure that the converter will power the load under all conditions. Secondly, the maximum current at which the current limit will trip (I_{CLmax}). This value is needed to satisfy safety and system specifications, as well as for inductor design. Finally, the maximum current ($I_{CLtherm}$) with the MOSFET's junction at its maximum rated temperature is needed to verify the converter's ability to survive a short circuit under worst-case conditions.

The current limit will trip if the voltage across the p-channel MOSFET is more than V_{CL} while the MOSFET is fully on. The peak drain current is the sum of the average inductor current and one half the ripple current. Therefore,

$$I_{CL} = \frac{V_{CL}}{r_{DS(on)}} - \frac{I_{ripple}}{2} \quad (2)$$

The values of V_{CL}, $r_{DS(on)}$, T_J, and I_{ripple} that are used to calculate each of the current limit ratings are given in Table 2. Unfortunately, the equations for these parameters are non-linear and interdependent. Therefore, an iterative approach is needed, consisting of the following steps.

Table 2. Worst-case Parameters as Used for the Current Limit Calculations

Type	V_{CL}	$r_{DS(on)}$	T_J	I_{ripple}
I_{CLmin}	Min	Max	Max	Max
I_{CLmax}	Max	Min	Min	Min
$I_{CLtherm}$	Max	Min	Max	Min

Begin by estimating T_J = 150°C at V_{in} = 16.5 V and assuming I_{ripple} = 0, so that $r_{DS(on)}$ can be determined. Calculate the power dissipation, including switching and conduction losses. Iterate the calculations to find the correct T_J. Determine the allowable ripple for $I_{CLmin} \geq I_{out(MAX)}$ = 1.5 A, which yields the minimum value for L. Having found L, use $r_{DS(on)}$ and T_J to verify operation at I_{CLmin} and $I_{CLtherm}$.

Power dissipation comes from two sources—switching losses and conduction losses. The conduction losses are equal to the square of the RMS current times the $r_{DS(on)}$ of the MOSFET. Assuming that the inductor is operating in its linear region and that the converter is efficient, the current running through the p-channel MOSFET is given by equation 3.

$$I_P(t) = \frac{V_{in} - V_{out}}{L} \times t + I_{out} - \frac{I_{ripple}}{2} \quad (3)$$

where $I_p(t)$ is the current through the p-channel MOSFET, V_{in} is the input voltage, V_{out} is the output voltage, I_{out} is converter output current, L is the inductance in Henries, and I_{ripple} is the inductor peak-to-peak ripple current. t is 0 when the p-channel MOSFET turns on and, t is I_{ripple} times L divided by the quantity V_{in} - V_{out} when the MOSFET turns off. The RMS current through the MOSFET (I_{rmsp}) is given by

$$I_{rmsp} = \sqrt{\left[I_{out}^2 + \frac{I_{ripple}}{12}\right]^2 \times \frac{V_{out}}{V_{in}}} \quad (4)$$

Conduction loss (P_{conp}) can now be calculated.

$$P_{conp} = r_{DS(on)} \times \frac{V_{out}}{V_{in}} \times \left[I_{out}^2 + \frac{I_{ripple}^2}{12}\right] \quad (5)$$

Energy lost per switching transition may be approximated by

$$E_{swp} = V_{in} \times I_p \times t_f \quad (6)$$

Here, t_f is the equivalent switching time for the MOSFET. A conservative number to use with the Si9943DY is 80 ns. This number will scale with gate charge, q_G, if other MOSFETs are used. Including both transitions, switching losses (P_{swp}) can be calculated using equation 7.

$$P_{swp} = 2 \times V_{in} \times I_{out} \times t_f \times f \quad (7)$$

where f is the clock frequency. The total power dissipated by the p-channel MOSFET is

$$P_p = P_{conp} + P_{swp} \quad (8)$$

To calculate allowable I_{ripple}, the I_{CLmin} specification must be recalculated using the calculated value for T_J. Using

$$T_J = P_p \ R_{thJA} + T_a \quad (9)$$

the equations for P_p, frequency (76kHz), and the graph of normalized $r_{DS(on)}$ versus T_J, an estimated T_J may be calculated. Here T_a, the ambient temperature, is 50°C, and R_{thja}, the junction-to-ambient thermal resistance, is assumed to be 62.5°C/W. After a couple of iterations, T_J is 90.7°C and I_{CLmin} is 2.02 A. This allows a maximum I_{ripple} of 1.0 A. Using the equation for $I_p(t)$ above,

$$I_{ripple} = \frac{(V_{in} - V_{out}) \times V_{out}}{f \times L \times V_{in}} \quad (10)$$

Therefore, this ripple current corresponds to an inductance of 43 µH with the worst case V_{in} = 16.5 V.

Now that the limits of the ripple current are known, the survivability of the converter can be checked for $r_{DS(on)}$ values corresponding to both V_{in} = 6 V and V_{in} = 16.5 V. Using equation 9 for T_J and the graph of $r_{DS(on)}$ versus T_J, the actual T_J and $I_{CLtherm}$ are calculated.

Table 3. Calculated Worst-case Current Limits Including Temperature and Ripple Current Effects

Spec	V_{in}	Inductance	Current	T_j
I_{CLmin}	6 V	Large	1.62 A	91°C
I_{CLmin}	6 V	43 µH	1.53 A	86°C
$I_{CLtherm}$	6 V	Large	2.89 A	141°C
$I_{CLtherm}$	6 V	43 µH	2.76 A	134°C
I_{CLmax}	16.5 V	Large	5.6 A	N/A

When used together, the Si9943DY and Si9150CY produce a converter which can be counted on to produce 1.5 A and which will tolerate any overcurrent situation which might arise.

Inductor Design

Having selected the p-channel MOSFET and determined the ripple current and the minimum current at which the inductor can be fully saturated, the inductor and other power components may be selected.

The inductor must meet five criteria:

1) Inductance of more than 43 µH
2) Linear while current is in the converter's operating range
3) Not fully saturated at a current of I_{CLmax}
4) Low cost and small size
5) Acceptable efficiency

To meet all of these criteria, a conveniently sized core is chosen, and the efficiency of the resulting inductor is checked. If the efficiency is acceptable, the design is done. If not, the inductor's size is adjusted until acceptable efficiency is reached. An approximate size and type of material must be chosen. Usually, either MPP or a power ferrite with an air gap is used in this type of application.

In this example, an MPP toroid will be used. The following values are needed—inductance (L), the peak magnetic field at which the core material is linear (B_{pk}), the peak current at which the inductor is linear (I_{pk}), the core equivalent length (l_e), the core equivalent cross section (A_e), and the available core permeability values. Using cgs units, the inductance is

$$L = \frac{4 \times \pi \times A_e \times N^2}{l_e} \times 10^{-9} \quad (11)$$

where π is 3.14 and N is the number of turns. Also, using the following relationships,

$$n = \frac{N}{l_e} \quad (12)$$

$$H_{pk} = \frac{4 \times \pi \times n \times I_{pk}}{10} \quad (13)$$

$$\mu = \frac{B_{pk}}{H_{pk}} \quad (14)$$

the maximum value of µ can be determined from

$$\mu_{MAX} = \frac{A_e \times l_e \times B_{pk}^2}{4 \times L \times \pi \times I_{pk}^2} \times 10^{-7} \quad (15)$$

A Magnetics Inc. MPP core size of 55040 is larger than necessary, so the 55290 size is checked. Under normal operation the inductance should remain constant, so use I_{pk} = 3 A. Since MPP has a soft saturation characteristic, it may be used aggressively, and B_{pk} = 5500 gauss is chosen. If a ferrite is used, I_{pk} = 5.7 A and the ferrite's B_{sat} at 150°C would be used to prevent complete saturation under worst-case conditions.

The gap can be adjusted to give the desired equivalent permeability. An ungapped ferrite should not be used. The 55290 core has $A_e = 0.095\ cm^2$ and l_e of 2.18 cm. Plugging these numbers and 43 µH into the above equation, μ_{max} is 131. Referring to the catalog, 125 is the next lower permeability available. Using the above equations,

$$N \leq \frac{10 \times l_e \times B_{pk}}{4 \times \mu \times \pi \times I_{pk}} \qquad (16)$$

If µ = 125, N is less than 25.4 turns. Using a 55290 core with 25 turns and the equation for L above, L is 42.7 µH. Since there is some leeway in the $I_{CL\,min}$ specification, this value is acceptable.

Now, losses in the inductor are calculated. While the p-channel MOSFET is on, the current in the inductor is the same as the current through the p-channel MOSFET. When the MOSFET is off, the current ramps back down to the same level as at t = 0. Thus, the inductor RMS current (I_{rmsi}) can be calculated as

$$I_{rmsi} = \sqrt{I_{out}^2 + \frac{I_{ripple}^2}{12}} \qquad (17)$$

The resistance of the inductor wire equals the wire length times its resistance per unit length, which for 25 turns of 24-gauge copper wire is

$$R_W = 0.839\ \frac{m\Omega}{cm} \times 48\ cm = 40\ m\Omega \qquad (18)$$

Next the wire losses (P_{wire}) in the inductor can be calculated. Since the converter will typically run at less than 1 A, I_{out} has been set to 1 A.

$$P_{wire} = I_{rms}^2 \times R_W = 40\ mW \qquad (19)$$

or about 0.8% of the output power. Finally, core losses are calculated. The ripple in the B field (ΔB) is given by

$$\Delta B = \frac{(V_{in} - V_{out}) \times V_{out}}{f \times N \times A_e \times V_{in}} \times 10^8 \qquad (20)$$

Substituting V_{in} = 10 V (the input voltage at which the inductor voltage is a symmetric square wave), ΔB = 1,238 gauss. Using the equation supplied by the core vendor, the loss is

$$P_{core} = 0.489 \times 10^{-11} \times 0.0039 \times f^{1.28} \times \left(\frac{\Delta B}{2}\right)^{2.14} \qquad (21)$$

or 37 mW. Although this number is not exact, it is evident that core losses are not a problem. The total loss due to the inductor is about 1.5% of the output power—small enough for this application.

Capacitor Selection

If the load and source capacitances are ignored, the minimum capacitance and maximum ESR values are obtained, which may be used for conservative design. Such an approach leads to overdesign. Instead, the input capacitor was chosen to avoid significant losses or voltage drop, and the input and output capacitor ESR values are assumed to be halved by the power source and load capacitors. 33-µF, 20-V and 47-µF, 10-V tantalum capacitors are checked for the input and output filters. Three capacitors are paralleled for the input, and two for the output. After halving, the maximum rated ESR for AVX surface-mount capacitors are 166 mΩ and 225 mΩ for the input and output, respectively.

Although the ripple voltage is usually the limiting factor, the power dissipated in the capacitors will be discussed first. The current flowing through the input capacitor (I_{cap}) is

$$I_{cap}(t) = I_p(t) - \overline{I_p(t)} \qquad (22)$$

where $I_p(t)$ is the current through the p-channel MOSFET and $\overline{I_p(t)}$ is the average input current. The input capacitor RMS current (I_{rmsci}) is

$$I_{rmsci} = \sqrt{\overline{I_p^2(t)} - \overline{I_p(t)^2}} \qquad (23)$$

or

$$I_{rmsci} = \left[I_{out}^2 + \frac{I_{ripple}^2}{12}\right] \times \frac{V_{out}}{V_{in}} - \frac{V_{out}^2}{V_{in}^2} \times I_{out}^2 \qquad (24)$$

Now, the power dissipated by the input capacitor can be calculated by using the capacitor ESR.

$$P_{ci} = ESR_{in}\ I_{rmsci}^2 \qquad (25)$$

With ESR_{in} = 166 mΩ, V_{in} = 10 V, V_{out} = 5 V, and I_{out} = 1 A, the power dissipated is 59 mW (or 1.2% of the converter's output power). Likewise, the RMS current through the output capacitor (I_{rmsco}) is

$$I_{rmsco} = \sqrt{\frac{1}{12}} \times I_{ripple} \quad (26)$$

and the power dissipated is

$$P_{co} = ESR_{out} \; I^2_{rmsco} \quad (27)$$

Under the same conditions used for the input capacitor power calculation above, P_{co} is 21 mW or 0.4%.

Now the input and output voltage ripple will be considered. Voltage ripple is caused by two effects, capacitor ESR times the ripple current, and the charge transfer divided by the capacitance.

$$V_{pkio} = ESR_{out} \; I_{ripple} \quad (28)$$

and

$$V_{RMSIO} = ESR_{out} \; I_{RMSCO} \quad (29)$$

where V_{pkio} is the peak-to-peak output ripple voltage and V_{rmsio} is the RMS output ripple voltage, both due to the output capacitor ESR. The peak-to-peak ripple voltage due to capacitance (V_{pkqo}) is

$$V_{pkqo} = \frac{1}{C_{out}} \times \frac{1}{2} \times \left[\frac{1}{2 \times f} \times \frac{I_{ripple}}{2} \right] \quad (30)$$

Since the input ripple is somewhat harder to calculate, the input current is assumed to be larger than I_{ripple}. Under these conditions,

$$V_{pkii} = ESR_{in} \times \left[I_{out} \times \frac{I_{ripple}}{2} \right] \quad (31)$$

and

$$V_{pkqi} = \frac{1}{C_{in}} \times \frac{1}{f} \times \left[1 - \frac{V_{out}}{V_{in}} \right] \times I_{out} \times \frac{V_{out}}{V_{in}} \quad (32)$$

where V_{pkii} in the input ripple's ESR component and V_{pkqi} is the input ripple's capacitive component. Using worst-case conditions for the input and output ripple voltages (V_{in} = 16.5 V, I_{out} = 1.5 A, ESR_{out} = 200 mΩ, and C_{out} = 100 µF), V_{rmsio} is 69 mV. Comparing the peak-to-peak ESR and capacitive ripples, respectively 238 mV and 69 mV, the capacitive component will not add enough voltage to make the RMS ripple exceed 80 mV. This is a high number, but still less than specified. A similar analysis of the voltage across the input capacitor reveals an expected RMS voltage at the input of less than 140 mV.

Schottky Diode

A Schottky diode is included in the circuit to prevent the internal diode of the n-channel MOSFET from turning on. The internal MOSFET should remain off for two reasons. First, being a silicon p-n diode, it has a reverse recovery charge that will cause an effect similar to shoot-through. To estimate these losses, the reverse recovery charge should be multiplied by the input voltage and the converter clock frequency. The charge can be estimated as 130% of half of the di/dt times the reverse recovery time squared. In this converter, with V_{in} = 16.5 V and I_{out} = 1.5 A, the loss would be about 130 mW or 2%. Note that while the n-channel MOSFET is causing this power loss, heat is generated in the p-channel MOSFET. The second reason that the Schottky is included is that it has a lower forward drop than the n-channel MOSFET internal diode. The Schottky diode conducts while both MOSFETs are off. During normal operation, this period totals about 300 ns per cycle. During a current limit caused by a very low load resistance, the inductor may completely discharge though the Schottky. The Schottky will generate much less heat than the MOSFET diode while the inductor is discharging.

The Schottky should be chosen so that its forward drop is less than the forward drop of the n-channel MOSFET internal diode at $I_{CLtherm}$. This selection will prevent the additional heat from reverse-recovery charge from overheating the p-channel MOSFET during a high current condition.

Feedback Network Design

A high-efficiency converter requires an output filter with low losses (a high Q). The fast 180-degree phase shift and large increase in gain at the filter resonant frequency complicate the design of the feedback network. For purposes of this discussion, the converter will be simplified to the behavioral model shown in Figure 3. The gain and phase of the output filter are given in Figure 4.

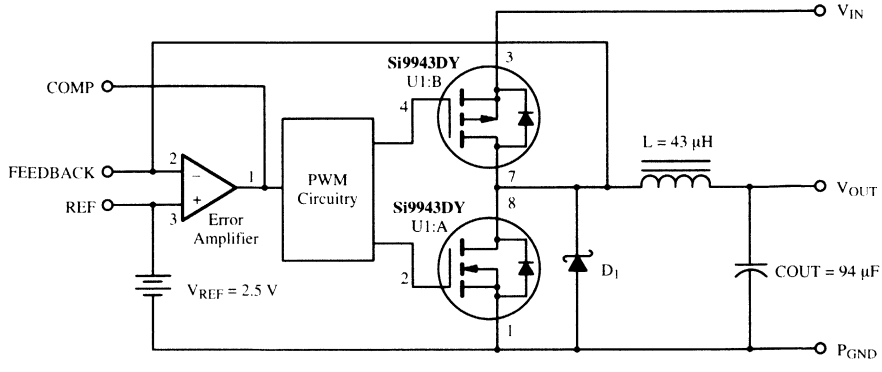


Figure 3a. The Actual Circuit

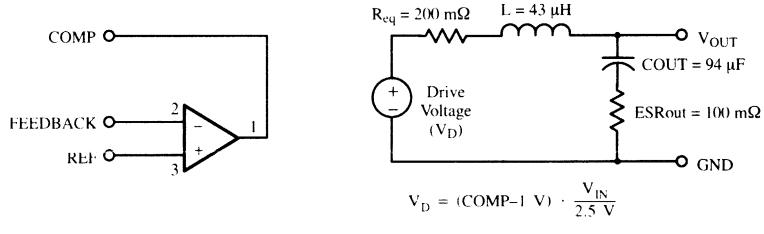


Figure 3b. Behavioral Model for Feedback Loop Analysis

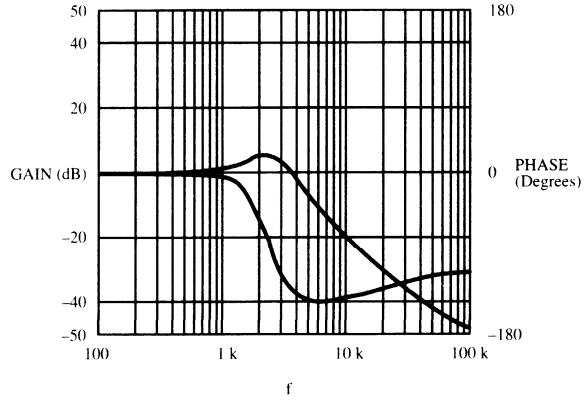


Figure 4. Output Filter Response

At low frequencies, the impedance of the inductor is small while the impedance of the capacitor is large, causing the output voltage to be about the same as the input voltage. At high frequencies, the inductor controls the current reaching the capacitor. The current through the inductor lags the input voltage by 90 degrees. Likewise, the voltage across the capacitor lags the current through the inductor by 90 degrees. Therefore, since the output voltage lags the input voltage by 180 degrees, the voltage is actually inverted by the filter.

Two approaches may be used for compensation of the buck converter power stage. Figure 5 shows the low-performance (integrator) compensation method. The circuit values corresponding to these plots are as follows: R_1 = 150 kΩ, C_1 = 0.01 µF (R_2, R_3, C_2, and C_3 are not used). By using a dominant low-frequency pole the loop gain can be reduced to 0 dB at a frequency substantially below the filter resonant frequency. This results in a slow dynamic response.

To obtain better performance, the gain of the converter must be greater than one at the resonant frequency. We can achieve this improvement by designing the feedback circuit to differentiate, rather than integrate, near the resonant frequency. This approach, which is referred to as a lead-lag network, was used for the compensation of the buck converter. Figure 6 gives the Bode plots for the feedback network and the total loop gain for the circuit values given in Figure 2.

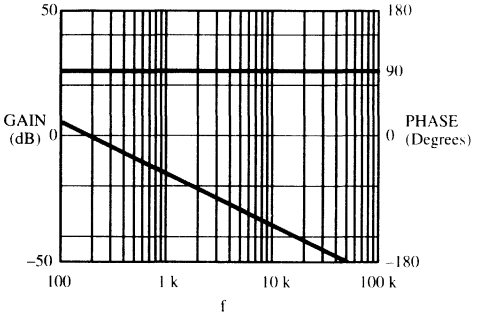


Figure 5a. Low-performance Feedback Network Transfer Function

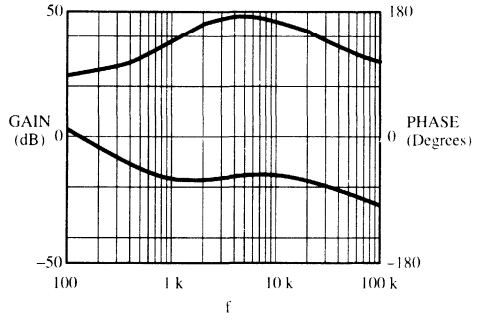


Figure 6a. High-performance Feedback Network Transfer Function

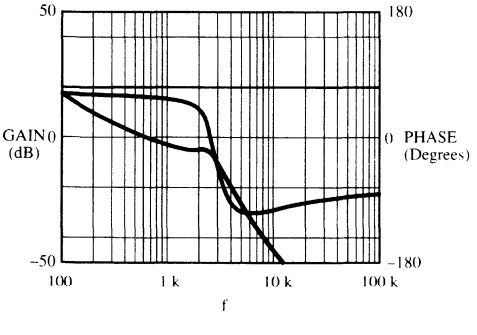


Figure 5b. Open-loop Gain for the Converter With Low-performance Feedback Network

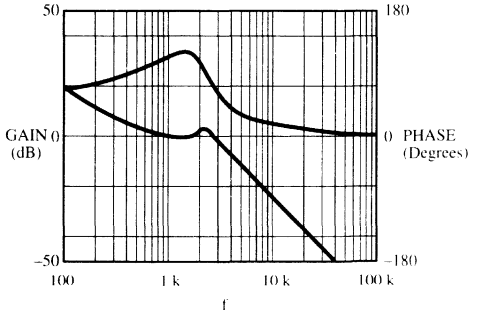


Figure 6b. Open-loop Gain for the Converter With High-performance Feedback Network

Dynamic Response Limitations

Synchronous operation of the converter ensures that the inductor flux is not left at zero, since the inductor current can flow in the reverse direction. Thus the converter runs in continuous conduction mode at all times. The minimum excursion of the output voltage which can be theoretically achieved in continuous conduction is limited by the output filter components.

Assuming an ideal feedback network, the controller responds to a step increase in load by immediately applying full voltage, V_{in}, to the output filter. Also assume that the output filter and switching circuit are lossless. Thus, using the behavioral model in Figure 3 with both resistors set to 0 Ω and solving for V_{out}, the following equations are obtained:

$$V_{in} - V_{out}(t) = L \times C \times \frac{d^2}{dt^2} \times V_{out}(t) \quad (33)$$

$$V_{ex}(t) = V_{out}(t) - V_{out}(0) \quad (34)$$

$$V_{ex}(0) = 0 \quad (35)$$

$$\frac{d}{dt} V_{ex}(t)|_0 = \frac{-I_{step}}{C} \quad (36)$$

$$\frac{d^2}{dt^2} V_{ex}(t)|_0 = \frac{V_{in} - V_{out}}{C \times L} \quad (37)$$

Solving equation 37 yields

$$V_{ex}(t) = \frac{-I_{step} \times \sin(\omega \times t)}{C \times \omega} + [V_{in} - V_{out}(0)]\ [1 - \cos(w\,t)] \quad (38)$$

where

$$\omega = \sqrt{\frac{1}{L \times C}} \quad (39)$$

$V_{ex}(t)$ is at an extreme at t_m as given by

$$t_m = \frac{\tan^{-1}\left[\frac{-I_{step}}{C \times \omega \times [V_{in} - V_{out}(0)]}\right]}{\omega} \quad (40)$$

Thus, for any given inductor, there is a minimum capacitor which must be used to achieve a given step response. This value should be padded by a factor of two if a high-performance compensation circuit is to be used. If a low-performance compensation circuit is to be used, the size of the capacitor will be even larger.

The error amplifier has a few characteristics which limit the feedback loop as well. First, the open loop gain is typically 75 dB. This is represented by a pole where the feedback network with an ideal op amp would reach a gain of 75 dB. Secondly, the op amp can source only about 1 mA. At a frequency and amplitude where more than 1 mA is required to keep the feedback pin at the reference voltage, the network will begin to resemble a wire, instead of an integrator. This should happen well above the unity gain crossover frequency of the control loop. Finally, the op amp has a limited gain bandwidth, as illustrated below in Figure 7.

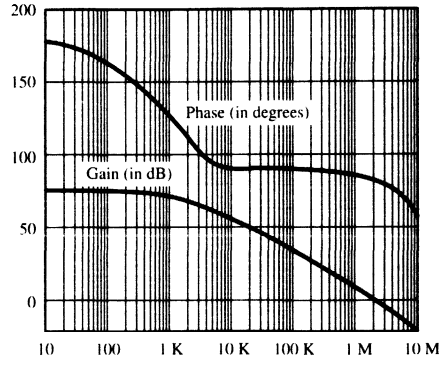


Figure 7. Error Amplifier Bode Plot

Soft-Start Capacitor Selection

After the current limit has been triggered, the following sequence of events occurs. First, the EN and SS pins are pulled low by the current limit circuitry. Once the EN pin has shut off the Si9150CY, both Si9943DY MOSFETs are off. The EN resistor pulls up the EN pin at a rate determined by the EN capacitor (C_6 = 180 pF). Once EN passes its threshold voltage, the reference and the current source for the $\overline{\text{STBY}}$ pin are activated. After $\overline{\text{STBY}}$ passes its threshold, the current for R_T and the feedback circuitry are turned on. After one clock cycle, the PWM circuitry is activated. Meanwhile, the error amplifier output is restricted to about 0.6 V above the SS voltage. Now the SS voltage ramps up, allowing the COMP voltage to increase. During this period, the converter output voltage will ramp up at a rate of approximately $V_{in}/2.5$ times the ramp rate of the SS voltage.

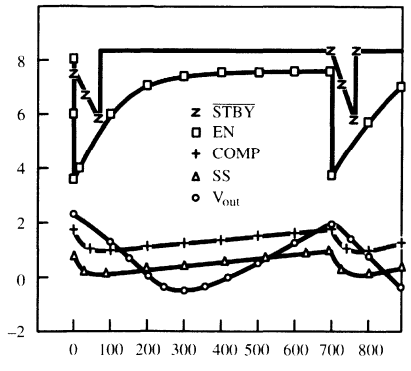


Figure 8. Startup Waveforms for V_{in} = 8.2 V, R_{LOAD} = Ω

Since the SS pin is pulled up by 25 µA (typical), the current needed to charge the output capacitor ($I_{startup}$) is

$$I_{startup} = C_{out} \times \frac{V_{in}}{2.5} \times \frac{25 \times 10^{-6}}{C_{SS}} \quad (41)$$

where C_{SS} the value of the soft start capacitor in Farads. $I_{startup}$ should be limited to a value low enough so as not to trigger the current limit when combined with the load that the converter will see initially.

Layout Considerations

For stable PWM operation and reliable current limiting (i.e., no false trips), it is necessary to use bypass capacitors for the Si9150CY and to lay out the grounds properly. Also, for high-efficiency the high-current traces should be made wide to minimize parasitic losses. These layout-related topics are covered here.

The lossless current sense circuit uses the V_{DD} pin as its reference. Therefore, the V_{DD} pin of the Si9150CY should be tied directly to the source of the p-channel MOSFET. Since there is switching noise on the source of the p-channel MOSFET, the ground should be broken into logic ground and power ground as shown in Figure 9. The bypass capacitor for the Si9150CY should be tied to the logic ground. The connection between the power and logic grounds should be much longer than the V_{DD} to p-channel source connection. As a result, the logic ground will track spikes on the p-channel source rather than the n-channel source. Of course, all the signal components, including the feedback network, should be referenced to the logic ground.

Figure 9 also shows the ac current paths. The most critical loop is defined by C_9, the p-channel MOSFET, and the n-channel MOSFET in parallel with D_1.

This loop should be kept very short to keep its resonant frequencies high, so that it will not be excited by the switching of the p-channel MOSFET.

There are two high-current dc paths whose trace resistances should be minimized, as shown in Figure 10. The figure also shows the RMS currents which must be carried by the input and output filter capacitors.

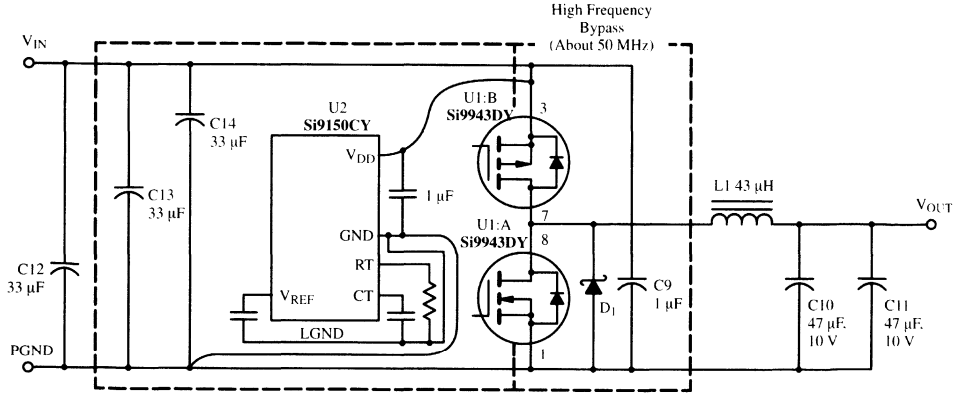


Figure 9. Ground Layout and High-frequency Bypassing

Conclusion

Cost-effective and small dc-to-dc converters with greater than 90% efficiency no longer require exotic technologies. Figure 11 plots the efficiency versus load current for the converter design described above. Peak efficiency of 97% is achieved at V_{in} = 6 V and I_{out} = 400 mA. Over a broad range of line and load conditions the efficiency exceeds 90%. The converter efficiency was also measured for 3.3-V output (change R_4 from 33.2 kΩ to 105 kΩ), as shown in Figure 12. Peak efficiency is 94% at V_{in} = 6 V and I_{out} = 400 mA.

For both the 3.3-V and 5-V cases, the efficiency is reduced as V_{in} increases. This reduction is due mainly to increased switching and inductor core losses and indicates that six NiCd or NiMH cells should be used for maximum efficiency .

The Si9150CY control IC integrates all of the required control functions for a synchronous rectified buck converter—including lossless current sensing, break-before-make timing, and PWM control functions. When driving the Si9943DY MOSFET half-bridge, an all surface-mount, 1.5-A buck regulator occupies only 2.25 square inches of circuit board.

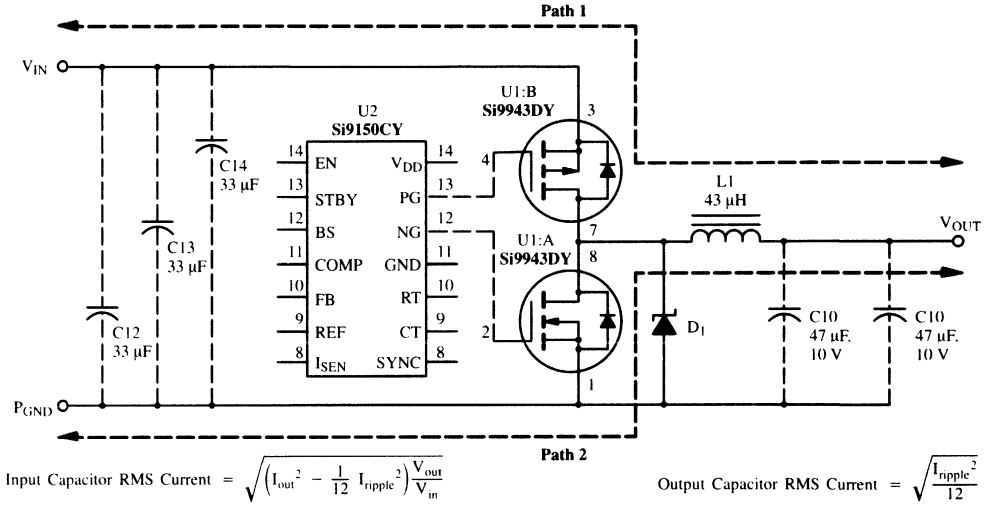


Figure 10. DC Current Paths

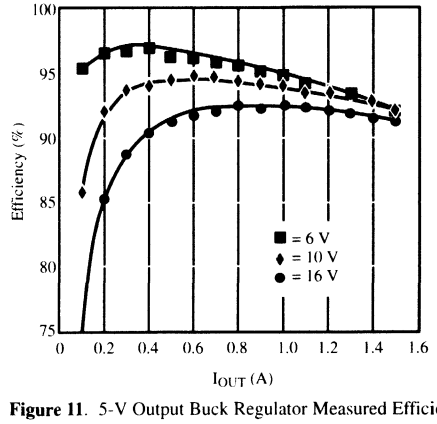


Figure 11. 5-V Output Buck Regulator Measured Efficiency

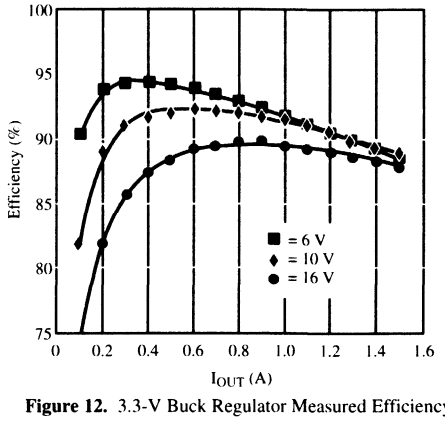


Figure 12. 3.3-V Buck Regulator Measured Efficiency

Controller for RF Power Amplifier Boost Converter

Features

- High Frequency Switching (up to 2 MHz)
- Optimized Output Drive Current (350 mA)
- Standby Mode
- Wide Bandwidth Feedback Amplifier
- Single-Cell LiIon and Three-cell NiCd or NiMH Operation

Description

The Si9160 Controller for RF Power Amplifier Boost Converter is a fixed-frequency, pulse-width-modulated power conversion controller designed for use with the Si6801 application specific MOSFET. The Si9160 and the Si6801 are optimized for high efficiency switched-mode power conversion at 1 MHz and over. The device has an enable pin which can be used to put the converter in a low-current mode compatible with the standby mode of most cellular phones. A wide bandwidth feedback amplifier minimizes transient response time allowing the device to meet the instantaneous current demands of today's digital protocols. The input voltage range accommodates minimal size and cost battery pack configurations.

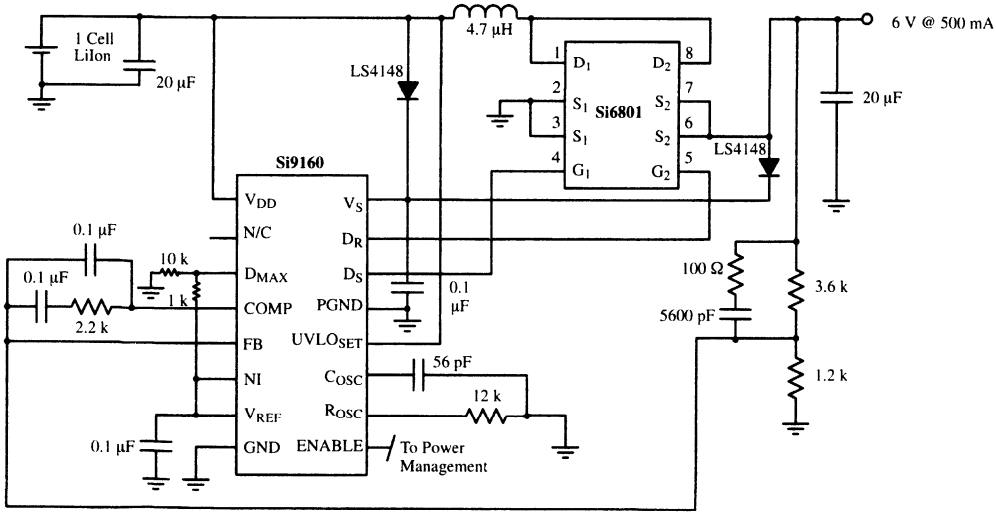
Frequency control in switching is important to noise management techniques in RF communications. The Si9160 is easily synchronized for high efficiency power conversion at frequencies in excess of 1 MHz.

Optimizing the controller and the synchronous FETs results in the highest conversion efficiency over a wide load range at the switching frequencies of interest (1 MHz or greater). It also minimizes the overshoot and gate ringing associated with drive current and gate charge mismatches.

When disabled, the converter requires less than 330 µA. This capability minimizes the impact of the converter on battery life when the phone is in the standby mode.

Finally, operating voltage is optimized for LiIon battery operation (2.7 V to 4.5 V) and can also be used with three-cell NiCd or NiMH (3 V to 3.6 V), as well as four-cell NiCd or NiMH (4 V to 4.8 V) battery packs.

Application Circuit



Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70029.

New Product

Absolute Maximum Ratings

Voltages Referenced to GND.
V_{DD}, V_S ..... 7 V
P_{GND} ..... ±0.3 V
Linear Inputs ..... –0.3 V to V_{DD} +0.3 V
Logic Inputs ..... –0.3 V to V_{DD} +0.3 V
Peak Output Drive Current ..... 350 mA
Storage Temperature ..... –65 to 125°C
Operating Junction Temperature ..... 150°C

Power Dissipation (Package)[a]
16-Pin TSSOP (Q Suffix)[a, b] ..... 925 mW

Thermal Impedance (Θ_{JA})[a]
16-Pin TSSOP ..... 135°C/W

Notes
a. Device mounted with all leads soldered or welded to PC board.
b. Derate 7.4 mW/°C above 25°C.

* *Exposure to Absolute Maximum rating conditions for extended periods may affect device reliability. Stresses above Absolute Maximum rating may cause permanent damage. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum rating should be applied at any one time.*

Specifications

Parameter	Symbol	Test Conditions Unless Otherwise Specified[a] 2.7 V ≤ V_{DD}, V_S ≤ 6.0 V, GND = P_{GND}	Limits B Suffix –25 to 85°C Min[b]	Typ	Max[b]	Unit
Reference						
Output Voltage	V_{REF}	I_{REF} = –10 µA	1.455		1.545	V
		T_A = 25°C	1.477	1.50	1.523	
Oscillator						
Maximum Frequency[c]	f_{MAX}	V_{DD} = 5 V, C_{OSC} = 47 pF, R_{OSC} = 5.0 kΩ	2.0			MHz
Oscillator Frequency Accuracy		V_{DD} = 2.7 V, f_{OSC} = 1 MHz (nominal) C_{OSC} = 100 pF, R_{OSC} = 7.5 kΩ, T_A = 25°C	–15		15	%
R_{OSC} Peak Voltage	V_{ROSC}			1.0		V
Voltage Stability[c]	Δf/f	4 V ≤ V_{DD} ≤ 6 V, Ref to 5 V, T_A = 25°C	–8		8	%
Temperature Stability[c]		Referenced to 25°C		±5		
Error Amplifier (C_{OSC} = GND, OSC DISABLED)						
Input Bias Current	I_B	V_{NI} = V_{REF}, V_{FB} = 1.0 V	–1.0		1.0	µA
Open Loop Voltage Gain	A_{VOL}		47	55		dB
Offset Voltage	V_{OS}	V_{NI} = V_{REF}	–15	0	15	mV
Unity Gain Bandwidth[c]	BW			10		MHz
Output Current	I_{OUT}	Source (V_{FB} = 1 V, NI = V_{REF})		–2.0	–1.0	mA
		Sink (V_{FB} = 2 V, NI = V_{REF})	0.4	0.8		
Power Supply Rejection[c]	PSRR	4 V < V_{DD} < 6 V		60		dB
$UVLO_{SET}$ Voltage Monitor						
Under Voltage Lockout	V_{UVLOHL}	$UVLO_{SET}$ High to Low	0.85	1.0	1.15	V
	V_{UVLOLH}	$UVLO_{SET}$ Low to High		1.2		
Hysteresis	V_{HYS}	V_{UVLOLH} – V_{UVLOHL}		200		mV
UVLO Input Current	$I_{UVLO(SET)}$	V_{UVLO} = 0 to V_{DD}	–100		100	nA

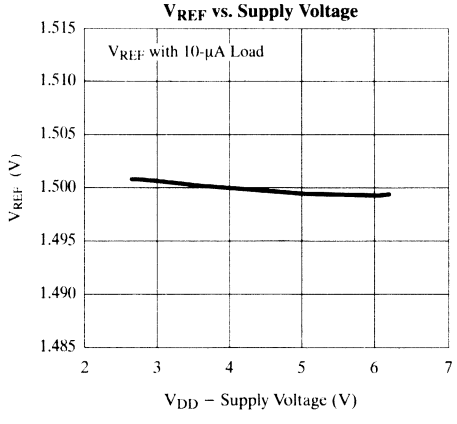
Specifications

Parameter	Symbol	Test Conditions Unless Otherwise Specified[a] 2.7 V ≤ V_{DD}, V_S ≤ 6.0 V, GND = P_{GND}		Limits B Suffix −25 to 85°C Min[b]	Typ	Max[b]	Unit
Output Drive (D_R and D_S)							
Output High Voltage	V_{OH}	V_{DD} = 2.7 V, V_S = 5.3 V	I_{OUT} = −10 mA	5.15	5.2		V
Output Low Voltage	V_{OL}		I_{OUT} = 10 mA		0.06	0.15	
Peak Source Output Current	I_{SOURCE}	V_{DD} = 2.7 V	V_S = 0 V		−300	−250	mA
Peak Sink Output Current	I_{SINK}		V_S = 5.3 V	250	300		
Break-Before-Make	t_{BBM}	V_{DD} = 6.0 V			40		ns
Logic							
ENABLE Delay to Output	td_{EN}	ENABLE Rising to OUTPUT, V_{DD} = 6.0 V			1.4		µs
ENABLE Logic Low	V_{ENL}					0.2 V_{DD}	V
ENABLE Logic High	V_{ENH}			0.8 V_{DD}			
ENABLE Input Current	I_{EN}	ENABLE = 0 to V_{DD}		−1.0		1.0	µA
Duty Cycle							
Maximum Duty Cycle	$CYCLE_{MAX}$	V_{DD} = 6.0 V			80	95	%
Supply							
Supply Current—Normal Mode	I_{DD}	f_{OSC} = 1 MHz, R_{OSC} = 7.5 kΩ	V_{DD} = 2.7 V		1.1	1.5	mA
			V_{DD} = 4.5 V		1.6	2.3	
Supply Current—Standby Mode		ENABLE = Low			250	330	µA

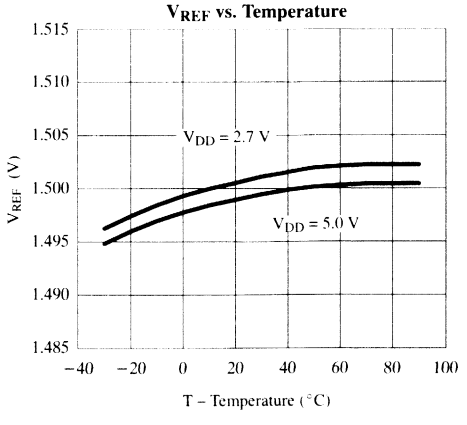
Notes
a. C_{STRAY} < 5 pF on C_{OSC}. After Start-Up, V_{DD} of ≥ 3 V.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
c. Guaranteed by design, not subject to production testing.

Typical Characteristics (25°C Unless Otherwise Noted)

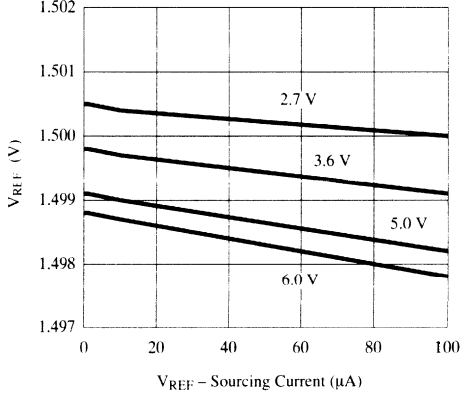
V_{REF} vs. Supply Voltage



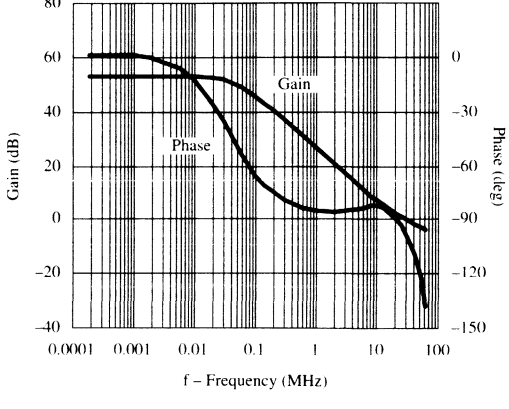
V_{REF} vs. Temperature



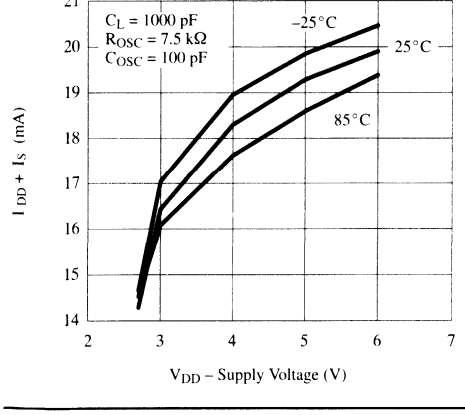
V_{REF} vs. Load Current



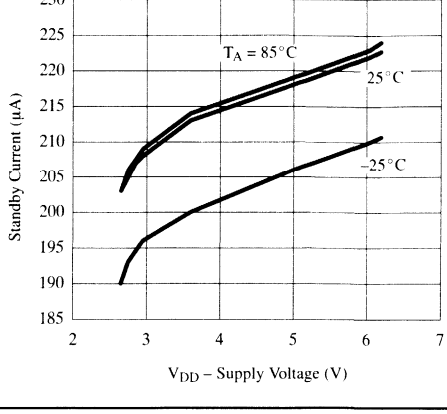
Error Amplifier Gain and Phase



Supply Current vs. Supply Voltage and Temperature

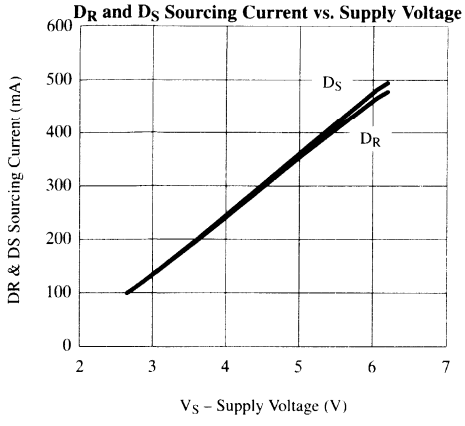


Standby Current vs. Supply Voltage and Temperature

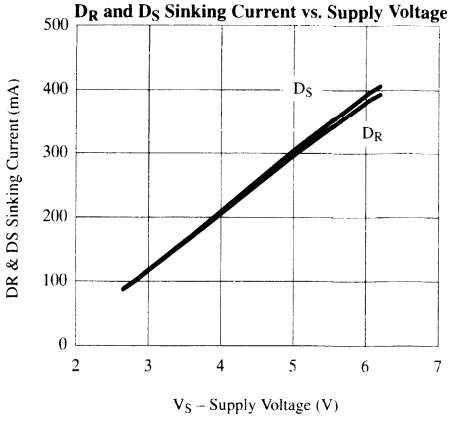


Typical Characteristics (25°C Unless Otherwise Noted)

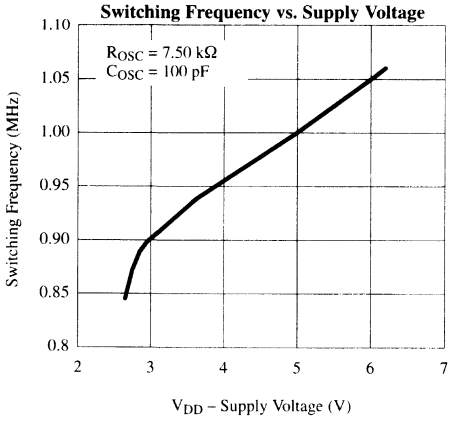
D_R and D_S Sourcing Current vs. Supply Voltage



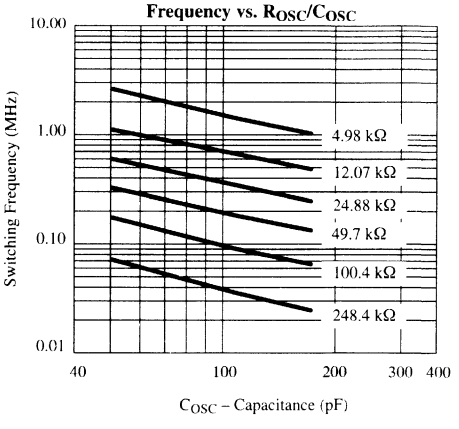
D_R and D_S Sinking Current vs. Supply Voltage



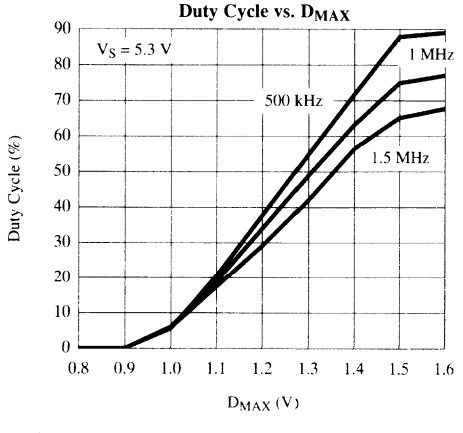
Switching Frequency vs. Supply Voltage



Frequency vs. R_{OSC}/C_{OSC}

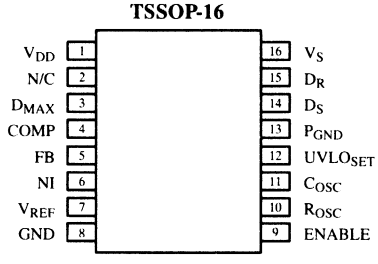


Duty Cycle vs. D_{MAX}



New Product

Pin Configurations



Order Number: Si9160BQ-T1

Pin Description

Pin 1: V_{DD}

The positive power supply for all functional blocks except output driver. A bypass capacitor of 0.1 µF (minimum) is recommended.

Pin 2: N/C

There is no internal connection to this pin.

Pin 3: D_{MAX}

Used to set the maximum duty cycle.

Pin 4: COMP

This pin is the output of the error amplifier. A compensation network is connected from this pin to the FB pin to stabilize the system. This pin drives one input of the internal pulse width modulation comparator.

Pin 5: FB

The inverting input of the error amplifier. An external resistor divider is connected to this pin to set the regulated output voltage. The compensation network is also connected to this pin.

Pin 6: NI

The non-inverting input of the error amplifier. In normal operation it is externally connected to V_{REF} or an external reference.

Pin 7: V_{REF}

This pin supplies a 1.5-V reference.

Pin 8: GND (Ground)

Pin 9: ENABLE

A logic high on this pin allows normal operation. A logic low places the chip in the standby mode. In standby mode, normal operation is disabled, supply current is reduced, the oscillator stops, and D_S goes low while D_R goes high.

Pin 10: R_{OSC}

A resistor connected from this pin to ground sets the oscillator's capacitor (C_{OSC}) charge and discharge current. See the oscillator section of the description of operation.

Pin 11: C_{OSC}

An external capacitor is connected to this pin to set the oscillator frequency.

$$f_{osc} \simeq \frac{0.75}{R_{OSC} \times C_{OSC}} \quad \text{(at } V_{DD} = 5.0 \text{ V)}$$

Pin Description (Cont'd)

Pin 12: $UVLO_{SET}$

This pin will place the chip in the standby mode if the $UVLO_{SET}$ voltage drops below 1.2 V. Once the $UVLO_{SET}$ voltage exceeds 1.2 V, the chip operates normally. There is a built-in hysteresis of 200 mV.

Pin 13: P_{GND}

The negative return for the V_S supply.

Pin 14: D_S

This CMOS push-pull output pin drives the external n-channel MOSFET. This pin will be low in the standby mode. A break-before-make function between D_S and D_R is built-in.

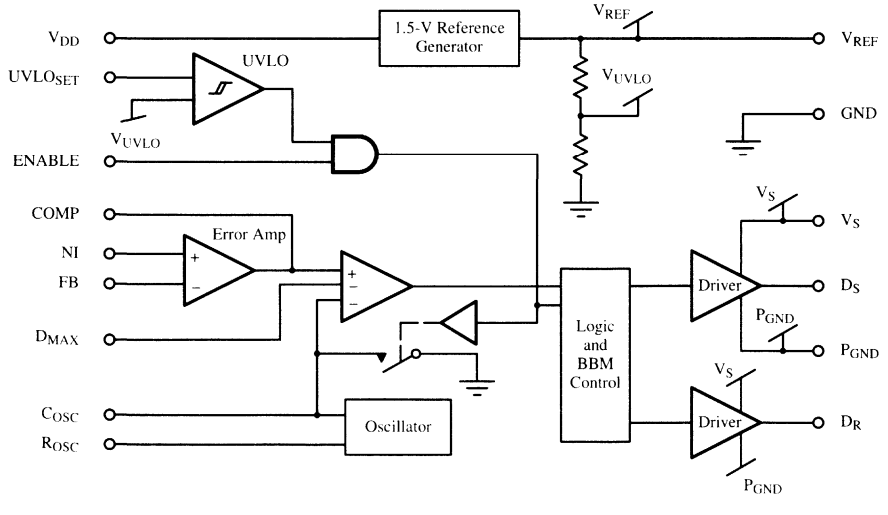
Pin 15: D_R

This CMOS push-pull output pin drives the external p-channel MOSFET. This pin will be high in the standby mode. A break-before-make function between the D_S and D_R is built-in.

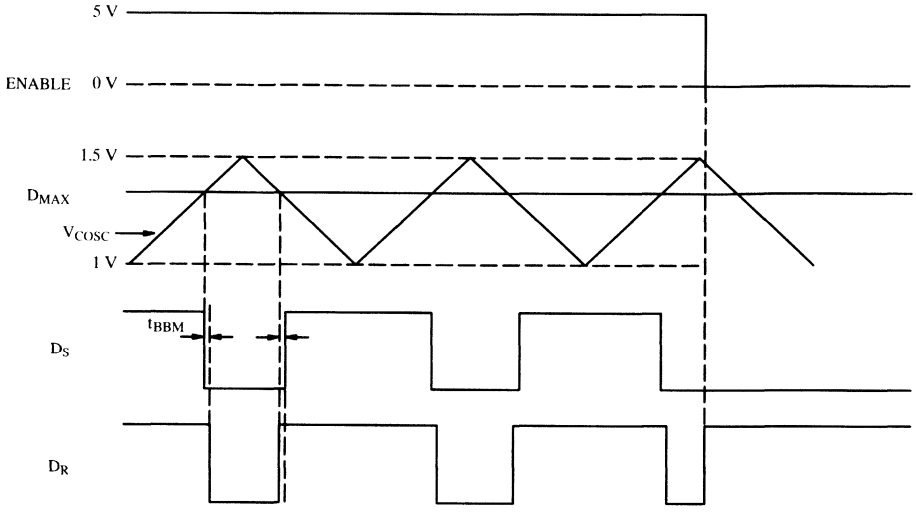
Pin 16: V_S

The positive terminal of the power supply which powers the CMOS output drivers. A bypass capacitor is required.

Functional Block Diagram



Timing Waveforms



Operation of the Si9160 Boost Converter

The Si9160 combined with optimized complementary MOSFETs provides the ideal solution to small, high efficiency, synchronous boost power conversion. Optimized for a 1-cell lithium ion, or 3-cell to 4-cell Nickel metal hydride battery, it is capable of switching at frequencies of up to 2 MHz. Combined with the Si6801, a complimentary high-frequency MOSFET, efficiencies of over 90% are easily achieved in a very small area.

PWM Controller

The Si9160 implements a synchronous voltage mode PWM control topology and is especially designed for battery power conversion. Voltage-mode control results in the most efficient power conversion solution. Figure 1 below illustrates a schematic for a synchronous boost converter with an input range of 2.7 V to 5 V which covers the range of 1-cell LiIon and 3-cell or 4-cell NiMH/NiCd battery input respectively, and an output voltage of 6 V. Note the maximum input voltage is limited to the output voltage for a boost converter.

The switching frequency is determined by an external capacitor and resistor connected to C_{osc} and R_{osc} pins. The graph on page 5 in the Typical Characteristics section shows the typical C_{osc} and R_{osc} values for various switching frequency. Si9160 oscillator frequency can be easily synchronized to external frequency as long as external switching frequency is higher than the internal oscillator frequency. The synchronization circuit is a series resistor and capacitor fed into the C_{osc} pin of the Si9160. The synchronization pulse should be greater than 1.5 V in amplitude and a near square wave pulsed clock. Figure 1 shows typical values for the synchronization components.

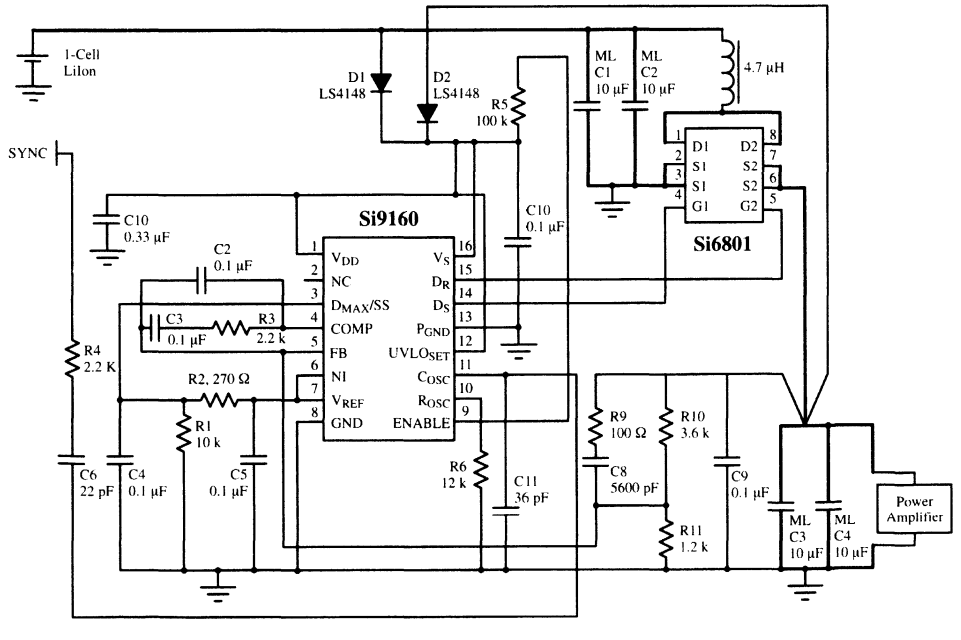


Figure 1. Si9160 Boost Converter

Startup

Designed to operate with single cell Lithium Ion battery voltage, the Si9160 has an operating range of 2.7 V to 6.0 V. During start-up, the device requires 3.0 V to guarantee proper operation, although it will typically start up at less than 2.2 V. Once powered, Si9160 will continue to operate until the voltage at V_{DD} is 2.7 V; at this point, the battery is basically dead. During start-up, power for the chip is provided by the battery through schottky diode D1 to V_{DD} and V_S pins. Once the converter is fully operating, supply power is provided by the converter output through diode D2, which overrides the D1 diode. This self perpetuating method of powering further improves the converter efficiency by utilizing higher gate drive to lower the on-resistance loss of the MOSFET.

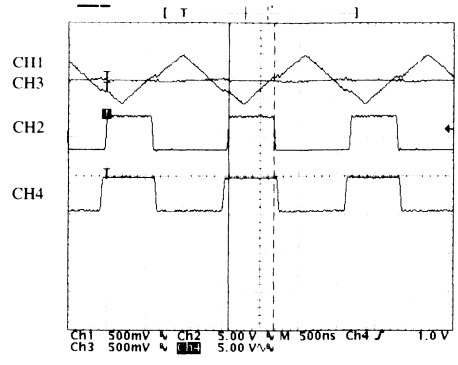
Another benefit of powering from the output voltage is it provides minimum load on the converter. This prevents the converter from skipping frequency pulses typically referred to as Burst or Pulse-Skipping modes. Pulse skipping mode could be dangerous, especially if it generates noise in RF, IF, or signal processing frequency bands.

Enable and Under Voltage Shutdown

The Si9160 is designed with programmable under-voltage lockout and enable features. These features give designers flexibility to customize the converter design. The under-voltage lockout threshold is 1.2 V. With a simple resistor divider from V_{DD}, Si9160 can be programmed to turn-on at any V_{DD} voltage. The ENABLE pin, a TTL logic compatible input, allows remote shutdown as needed.

Gate Drive and MOSFETs

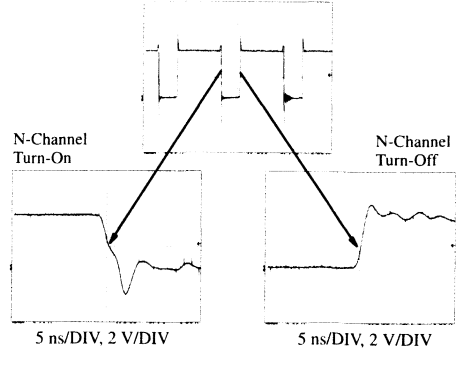
The gate drive section is designed to drive the high-side p-channel switch and low-side n-channel synchronous rectifier. The internal 40 ns break-before-make (BBM) timing prevents both MOSFETs from turning-on simultaneously. The BBM circuit monitors both drive voltages, once the gate-to-source voltage drops below 2.5 V, the other gate drive is delayed 40-ns before it is allowed to drive the external MOSFET (see Figure 2 for timing diagram). This smart gate drive control provides additional assurance that shoot-through current will not occur.



CH1: C_{OSC} ; CH2: D_S
CH3: COMP; CH4: D_R

Figure 2. Gate Drive Timing Diagrams

The MOSFET used is the Si6801, an n- and p-channel in a single package TSSOP-8. This package is called LITE FOOT®. The Si6801 is optimized to have very low gate charge and gate resistance. This results in a great reduction in gate switching power losses. The average time to switch on and off a MOSFET in a conventional structure is about 20 ns. The Si6801 will switch on and off in < 5 ns, see Figure 3.



Note the Speed

These MOSFETs have switching speeds of <5 ns. This high speed is due to the fast, high current output drive of the Si9160 and the optimized gate charge of the Si6801.

Figure 3. Gate Switching Times

Stability Components

A voltage mode boost converter is normally stabilized with simple lag compensation due to the additional 90° phase lag introduced by the additional right hand plane zero, as well as having a duty factor dependent resonant frequency for the output filter. The stability components shown in Figure 1 have been chosen to ensure stability under all battery conditions while maintaining maximum transient response. To do this we have used a 2-pole-zero pair configuration (type 3 amplifier configuration). Figure 4 shows the bode plot for the above circuit, maintaining > 50° phase margin over the entire battery voltage range.

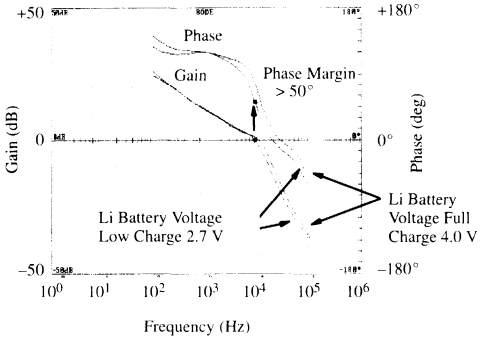


Figure 4. Stability, with 1-cell Li battery input, 5 V @ 600-mA output.

Energy Storage Components

The input and output ripple voltage is determined by the switching frequency, and the inductor and capacitor values. The higher the frequency, inductance, or capacitance values, the lower the ripple. The efficiency of the converter is also improved with higher inductance by reducing the conduction loss in the switch, synchronous rectifier, and the inductor itself. In the past, Tantalum was the preferred material for the input and output capacitors. Now, with 2-MHz switching frequencies, Tantalum capacitors are being replaced with smaller surface mount ceramic capacitors. Ceramic capacitors have almost no equivalent series resistance (ESR). Tantalum capacitors have at least 0.1-Ω ESR. By reducing ESR, converter efficiency is improved while decreasing the input and output ripple voltage. With ceramic capacitors, output ripple voltage is a function of capacitance only. The equation for determining output capacitance is stated below.

$$C = \frac{I_{OUT} \cdot (V_{OUT} - V_{IN})}{V_{OUT} \cdot \Delta V_{RIPPLE} \cdot f}$$

I_{OUT} = output dc load current
V_{OUT} = output voltage
V_{IN} = input voltage
ΔV_{RIPPLE} = desired output ripple voltage
f = switching frequency

The inductance value for the converter is a function of the desired ripple voltage and efficiency as stated below. In order to keep the ripple small and improve efficiency, the inductance needs to be large enough to maintain continuous current mode. Continuous current mode has lower RMS current compared to discontinuous current mode since the peak current is lower. This lowers the conduction loss and improves efficiency. The equation that shows the critical inductance which separates continuous and discontinuous current mode at any given output current is stated below. This equation is also plotted in Figure 5 as a function of input voltage.

$$L = \frac{V_{IN}^2 \cdot (V_{OUT} - V_{IN}) \cdot \eta}{2 \cdot V_{OUT}^2 \cdot I_{OUT} \cdot f}$$

η = efficiency

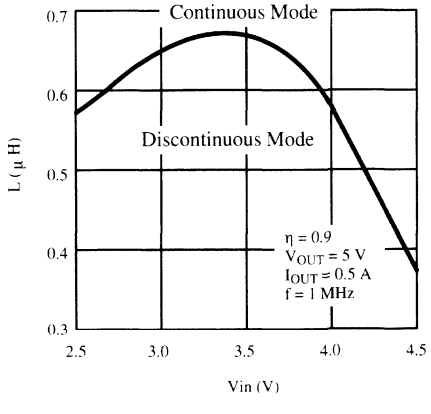


Figure 5. Continuous and Discontinuous Inductance Curve

Designed with small surface mount inductors and capacitors, the Si9160 solution can fit easily within a small space such as a battery pack. Another distinct advantage of a smaller converter size is that it reduces the noise generating area by reducing the high current path; therefore radiated and conducted noise is less likely to couple into sensitive circuits.

Results Section

The following section shows the actual results obtained with the circuit diagram shown in Figure 1.

Efficiency

The graph below shows the efficiency of the above design at various constant switching frequencies. The frequencies were generated using a 3-V square wave of the desired frequency to the sync input to the circuit. The input voltage to the circuit is 3.6-V dc.

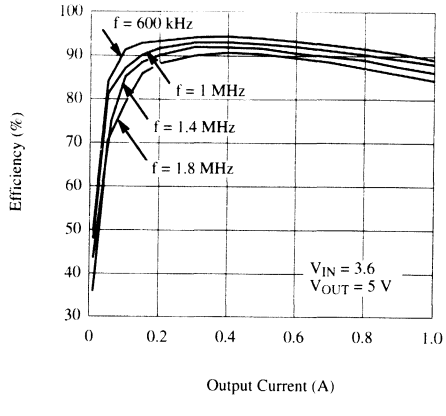


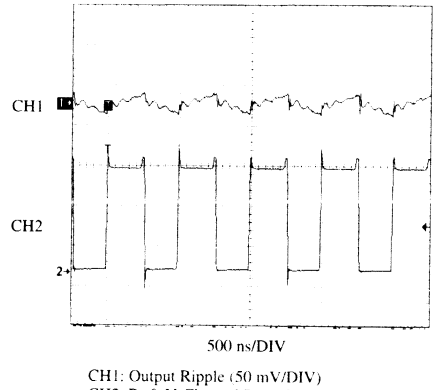
Figure 6. Efficiency of Si9160 and Si6801 Boost converter at various fixed frequencies

Output Noise

The noise generated by a dc-dc converter is always an issue within the mobile phone. The Si9160 offers two benefits.

1. The noise spectrum is a constant, i.e. no random noise or random harmonic generation.

2. The switching fundamental can be synchronized to a known frequency, e.g. 812.5 kHz which is $^1/_{16}$-th of the GSM/DCS system clock, 1.23 MHz which is the channel spacing frequency for CDMA, etc.



CH1: Output Ripple (50 mV/DIV)
CH2: P- & N-Channel Drain Voltage (2 V/DIV)

Figure 7. Output noise of the Si9160 demo board

Figures 7 through 9 show the output noise and output spectrum analysis.

Output Noise Spectrum

Note there is no random noise, only switching frequency harmonics. This is very good news for the RF stages, where an unknown, or random noise spectrum will cause problems.

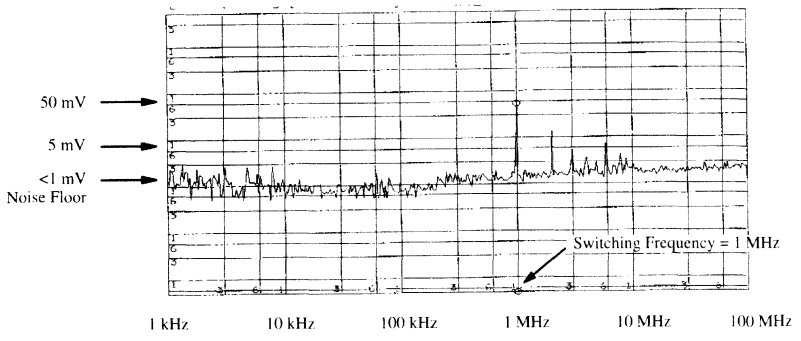


Figure 8. Spectrum response for the Si9160 demo board output voltage

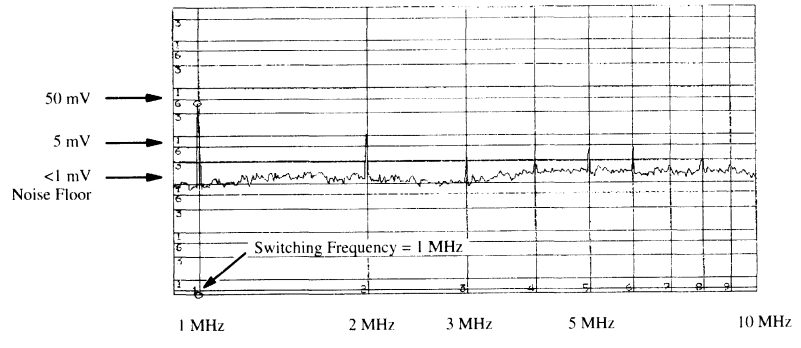


Figure 9. Higher resolution of noise spectrum

Conclusion

Switching at high, known frequencies results in a smaller footprint while maintaining high efficiency. Efficiencies at high switching frequencies can be improved by using Si6801 optimized low gate charge and low gate resistance MOSFET. Additionally, synchronization to an external high frequency clock eliminates or greatly reduces any radio interference concerns and pushes harmonics out beyond signal processing frequencies.

Si786 Demonstration Board

Features

- 5- and 3.3-V Step-Down Synchronous Converters
- Less than 500-µA Quiescent Current
- 25-µA Shutdown Current
- 5.5- to 30-V Input Operating Range

The Si786 Dual-Output Power-Supply Controller for Notebook Computers is a system level integration of two step-down controllers, micropower 5- and 3.3-V linear regulators, and two comparators. The controllers perform high efficiency conversion of the battery pack energy (typically 12 V) or the output of an ac-to-dc wall converter (typically 18- to 24-V_{DC}) to 5- and 3.3-V system supply voltages. The micropower linear regulator can be used to keep power management and back-up circuitry alive during the shutdown of the step-down converters. The comparators can be biased at any voltage, simplifying battery monitoring or providing sufficient voltage to enhance the gate of a low on-resistance n-channel FET used in switching power to different zones in the system.

On the Demo Board, the Si786 is configured as a complete system, ready for operation. It takes 5.5- to 30-V in, and produces regulated 5 V at any current from no load to 3 A, and 3.3 V out at any current from no load to 3 A. Included in this document are the Bill of Materials, Demo Board Schematic, and PCB layout

The demonstration board layout is available in Gerber file format. Please contact your TEMIC sales representative or distributor for a copy.

Ordering Information: Part Number Si786DB

Power-up Check List

1. Start by setting the control switches located in the bottom right corner of the Demo Board. Set the top switch to the left, setting the switching frequency to 200 kHz (to the right is 300 kHz). Set the second switch down to the right, turning the 5-V converter on (to the left is off). Set the third switch down to the right, turning the 3.3-V converter on (to the left is off). Set the bottom switch to the right, allowing the PWM to operate (to the left is shutdown).

2. Attach an electronic load set in resistive mode to the 3.3-V output pins. Set the current to 100 mA. Alternatively, you can use a resistor of value 33 Ω, 1 W.

3. Attach an electronic load set in resistive mode to the 5-V output pins. Set the current to 100 mA. Alternatively, you can use a resistor of value 50 Ω, 1 W.

4. Attach a 10-V supply and ground to the pins on the top side of the board. It is best to use a separate wire from the supply's ground to each of the Demo Board's ground pins, because of the high currents at low input voltages.

5. Take an oscilloscope probe, and place the ground on the 5-V GND pin, and the probe on the 5-V pin. Set the vertical scale for this channel at ac coupled at 50 mV/div. Take a second probe, and place the ground on the 5-V GND pin, and the probe on pin 17 (LX_5) of the Si786. Set this channel at dc coupled 2 V/div. Set the time base at 200 µsec/div.

6. Leave the probes in place. Change the scale on the second probe (the one attached to pin 17) to 10 V/div, and the time base to 500 nsec/div. Set the 5-V output current on the electronic load to 1 A. Set the input power supply to 16 V. Alternatively, *first turn off the input power supply*, and replace the 50-W resistor with a 5-Ω, 10-W resistor, and then turn the input power supply back on, setting it to 16 V.

7. This step should be performed only if an electronic load is being used. Set the input voltage to 15 V. Remove the second probe (the one attached to pin 17 of the Si786), or turn off the channel displaying it. Place a current probe around the wire leading from the 5-V output to the electronic load, and set the oscilloscope and amplifier so that it will display approximately 2 A/div. Set the oscilloscope time base back to 200 µsec/div. Set the 3.3-V electronic load to have a constant 1-A load. Now set up the 5-V electronic load so that it cycles between 100 mA and 3 A at approximately 1 kHz (1 msec period).

8. This step should be performed only if an electronic load is being used. Set the 5-V electronic load back to a constant 1-A current. Remove the voltage probe from the 5-V output. Move the ground of the probe onto the GND pin of the 3.3-V output, and the probe onto the 3.3-V output pin. Remove the current probe from the 5-V output wire, and place it around the wire leading from the 3.3-V output to the electronic load. Now set up the 3.3-V electronic load so that it cycles between 100 mA and 3 A at approximately 1 kHz (1 msec period).

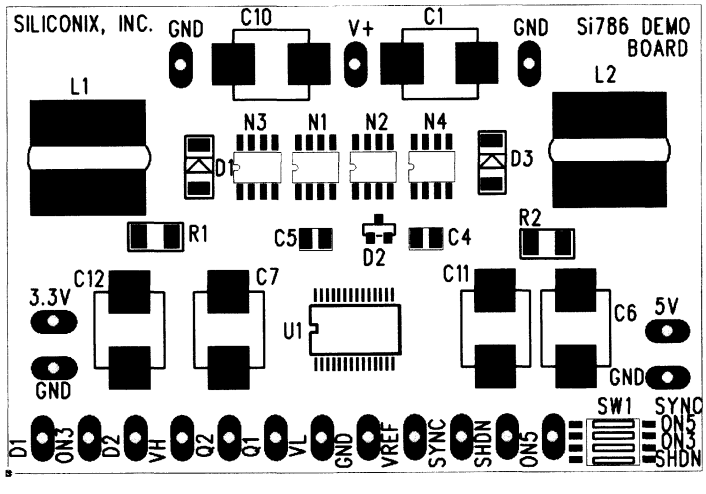


Figure 1. Top Silkscreen

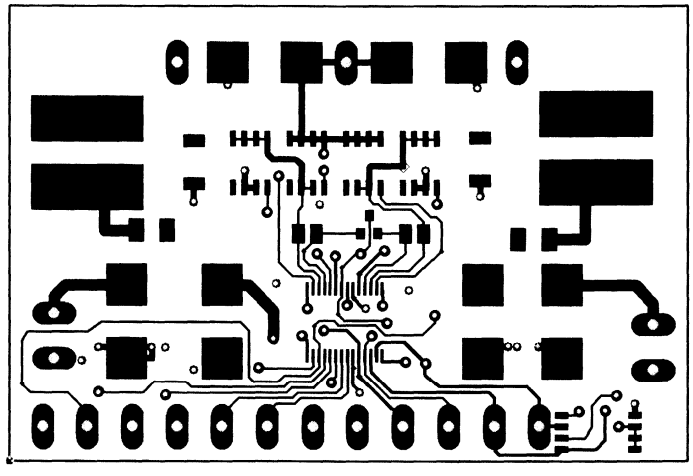


Figure 2. Top Layer

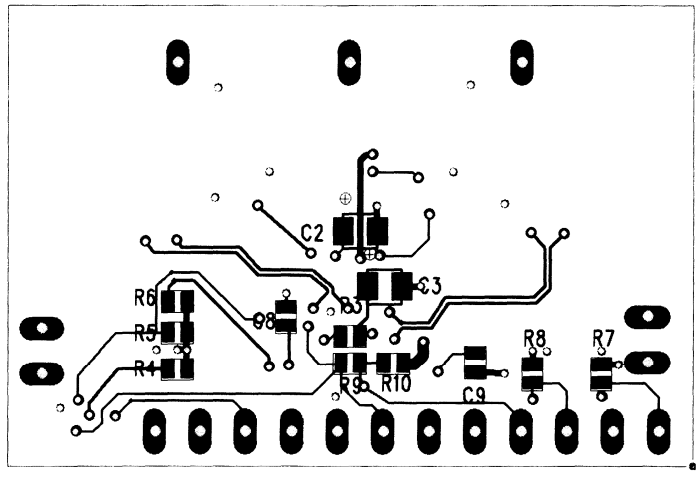
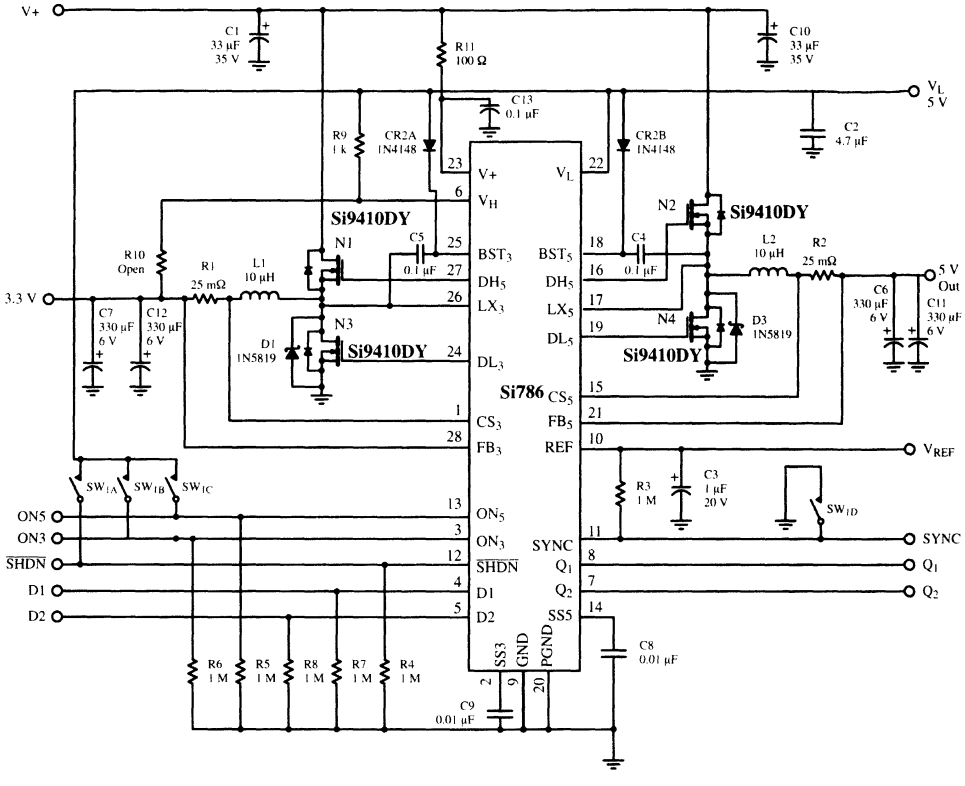


Figure 3. Bottom Layer

Si786DB Application Circuit



Bill of Material for Si786 Dual-Output Power Supply

Part	Used	Reference Designators	Part Type	Description/Part Number	Pattern	Manufacturer
1	1	U1	Si786	D-O PWR Supply, Si786	SSOP-28	Siliconix
2	2	L1, L2	10 µH	Inductor, 10 µH	CDR125-100	Sumida
3	4	N1-N4	Si9410DY	N-Channel MOSFET	SO-8	Siliconix
4	1	SW1	SPST	SW-SPST	DIP-4	Multi-Source
5	2	D1, D3	1N5819	Diode, 1N5819	SOD-87	Nikon
6	1	CR2	CMPD2836	Diode, Dual 1N4148	SOT-23	Central Semiconductor
7	2	R1, R2	0.025 Ω, 1%	Resistor, LR2010-01-R025F	2010	IRC
8	6	R3–R8	1 MΩ	Resistor, 1 MΩ	0805	Multi-Source
9	1	R9	1 kΩ	Resistor, 1 kΩ	0805	Multi-Source
10	1	R10	Open	Resistor, (Open)	0805	Multi-Source
11	1	R11	100 Ω	Resistor	0805	Multi-Source
12	2	C1, C10	33 µF, 35 V	Capacitor, Tantalum, 595D336X0035SR	R	Sprague
13	1	C2	4.7 µF, 6 V	Capacitor, Ceramic, 1206YG475ZAT	1206	AVX
14	2	C3	1 µF, 20 V	Capacitor, Tantalum, TAJA105M025	A	AVX
15	2	C4, C5	0.1 µF, 16 V	Capacitor, Ceramic	0805	Multi-Source
16	1	C6, C7, C11, C12	330 µF, 6 V	Capacitor, Tantalum, TPSE337M006R0100	E	AVX
17	2	C8, C9	0.01 µF, 16 V	Capacitor, Ceramic	0805	Multi-Source
18	1	C13	0.1 µF, 35 V	Capacitor, Cermaic	0805	Multi-Source

Si9130 Demonstration Board

Features

- 5- and 3.3-V Step-Down Synchronous Converters
- Less than 500-µA Quiescent Current
- 25-µA Shutdown Current
- 5.5- to 30-V Input Operating Range

Description

The Si9130 Dual-Output Power-Supply Controller for Notebook Computers is a system level integration of two step-down controllers with micropower 5- and 3.3-V linear regulators. The controllers perform high efficiency conversion of the battery pack energy (typically 12 V) or the output of an ac-to-dc wall converter (typically 18 V to 24 V_{DC}) to 5- and 3.3-V system supply voltages. The micropower linear regulator can be used to keep power management and back-up circuitry alive during the shutdown of the step-down converters. The 3.3-V output is adjustable to 3.3 V, 3.45 V or 3.6 V by programming control pins 3.45 ADJ and 3.6 ADJ. Leaving both pins open results in 3.3-V nominal output. Grounding pin 3.45 ADJ while leaving 3.6 ADJ open delivers 3.45-V nominal output. Grounding pin 3.6 ADJ while leaving 3.45 ADJ open delivers 3.6-V nominal ouput.

On the Demo Board, the Si9130 is configured as a complete system, ready for operation. It takes 5.5- to 30-V in, and produces regulated 5 V at any current from no load to 3 A, and 3.3 V out at any current from no load to 3 A. Included in this document are the Bill of Materials, Demo Board Schematic, and PCB layout.

The demonstration board layout is available in Gerber file format. Please contact your TEMIC sales representative or distributor for a copy.

Ordering Information: Part Number Si9130DB

Power-up Check List–Installed in VRM Mother Board Socket

1. Start by setting the control switches located in the bottom right corner of the Demo Board. Set the top switch to the left, setting the switching frequency to 200 kHz (to the right is 300 kHz). Set the second switch down to the right, turning the 5-V converter on (to the left is off). Set the third switch down to the right, turning the 3.3-V converter on (to the left is off). Set the bottom switch to the right, allowing the PWM to operate (to the left is shutdown).

2. Attach an electronic load set in resistive mode to the 3.3-V output pins. Set the current to 100 mA. Alternatively, you can use a resistor of value 33 Ω, 1 W.

3. Attach an electronic load set in resistive mode to the 5-V output pins. Set the current to 100 mA. Alternatively, you can use a resistor of value 50 Ω, 1 W.

4. Attach a 10-V supply and ground to the pins on the top side of the board. It is best to use a separate wire from the supply's ground to each of the Demo Board's ground pins, because of the high currents at low input voltages.

5. Take an oscilloscope probe, and place the ground on the 5-V GND pin, and the probe on the 5-V pin. Set the vertical scale for this channel at ac coupled at 50 mV/div. Take a second probe, and place the ground on the 5-V GND pin, and the probe on pin 17 (LX_5) of the Si9130. Set this channel at dc coupled 2 V/div. Set the time base at 200 µsec/div.

6. Leave the probes in place. Change the scale on the second probe (the one attached to pin 17) to 10 V/div, and the time base to 500 nsec/div. Set the 5-V output current on the electronic load to 1 A. Set the input power supply to 16 V. Alternatively, *first turn off the input power supply*, and replace the 50-W resistor with a 5-Ω, 10-W resistor, and then turn the input power supply back on, setting it to 16 V.

7. This step should be performed only if an electronic load is being used. Set the input voltage to 15 V. Remove the second probe (the one attached to pin 17 of the Si9130), or turn off the channel displaying it. Place a current probe around the wire leading from the 5-V output to the electronic load, and set the oscilloscope and amplifier so that it will display approximately 2 A/div. Set the oscilloscope time base back to 200 µsec/div. Set the 3.3-V electronic load to have a constant 1-A load. Now set up the 5-V electronic load so that it cycles between 100 mA and 3 A at approximately 1 kHz (1 msec period).

8. This step should be performed only if an electronic load is being used. Set the 5-V electronic load back to a constant 1-A current. Remove the voltage probe from the 5-V output. Move the ground of the probe onto the GND pin of the 3.3-V output, and the probe onto the 3.3-V output pin. Remove the current probe from the 5-V output wire, and place it around the wire leading from the 3.3-V output to the electronic load. Now set up the 3.3-V electronic load so that it cycles between 100 mA and 3 A at approximately 1 kHz (1 msec period).

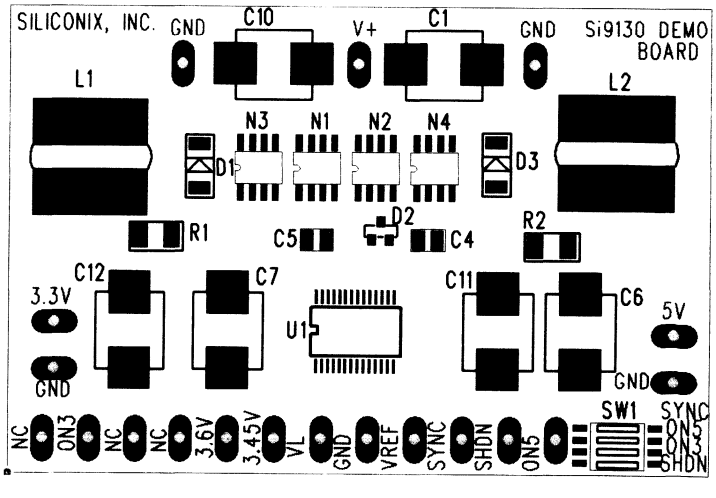


Figure 1. Top Silkscreen

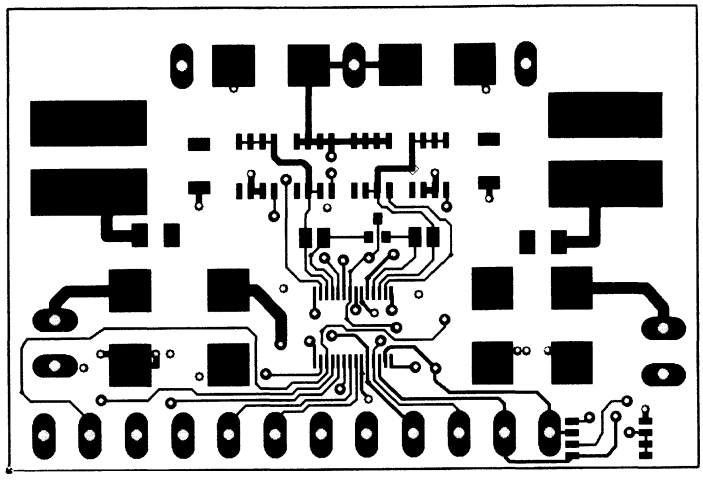


Figure 2. Top Layer

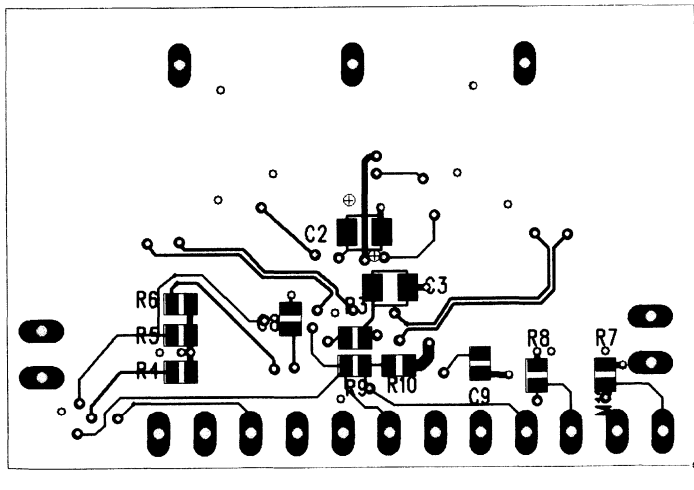
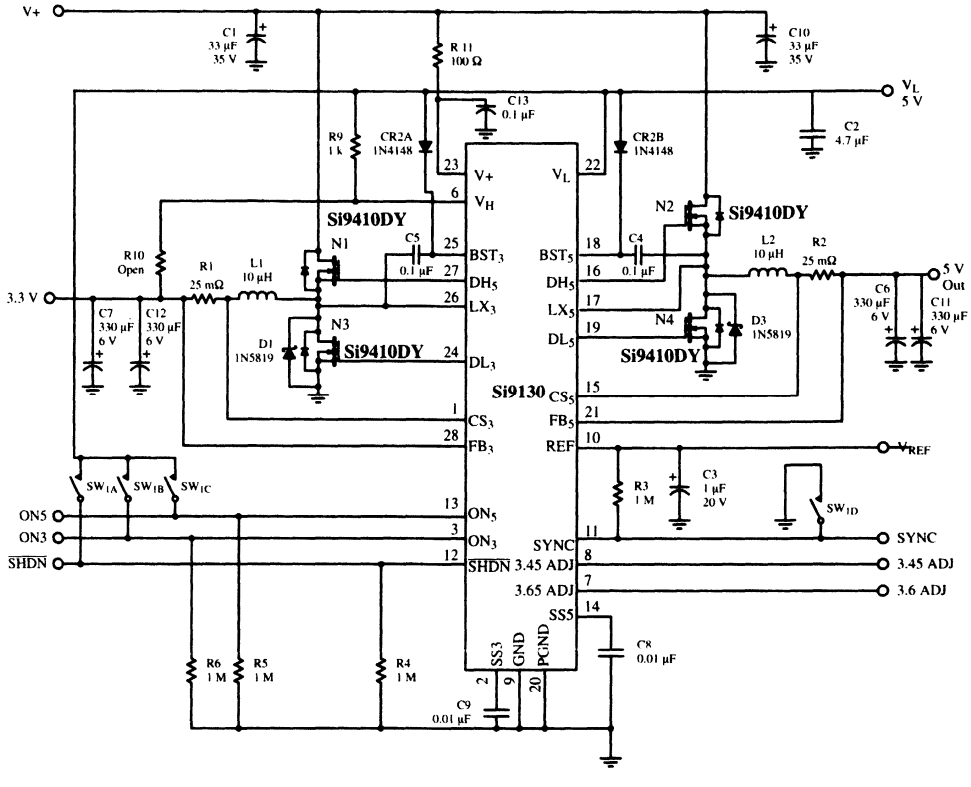


Figure 3. Bottom Layer

Si9130DB Application Circuit



Bill of Material for Si9130 Dual-Output Power Supply

Part	Used	Reference Designators	Part Type	Description/Part Number	Pattern	Manufacturer
1	1	U1	Si9130	D-O PWR Supply, Si9130	SSOP-28	Siliconix
2	2	L1, L2	10 µH	Inductor, 10 µH	CDR125-100	Sumida
3	4	N1-N4	Si9410DY	N-Channel MOSFET	SO-8	Siliconix
4	1	SW1	SPST	SW-SPST	DIP-4	Multi-Source
5	2	D1, D3	1N5819	Diode, 1N5819	SOD-87	Nikon
6	1	CR2	CMPD2836	Diode, Dual 1N4148	SOT-23	Central Semiconductor
7	2	R1, R2	0.025 Ω, 1%	Resistor, LR2010-01-R025F	2010	IRC
8	6	R3–R6	1 MΩ	Resistor, 1 MΩ	0805	Multi-Source
9	1	R9	1 kΩ	Resistor, 1 kΩ	0805	Multi-Source
10	1	R10	Open	Resistor, (Open)	0805	Multi-Source
11	1	R11	100 Ω	Resistor	0805	Multi-Source
12	2	C1, C10	33 µF, 35 V	Capacitor, Tantalum, 595D336X0035SR	R	Sprague
13	1	C2	4.7 µF, 6 V	Capacitor, Ceramic, 1206YG475ZAT	1206	AVX
14	2	C3	1 µF, 20 V	Capacitor, Tantalum, TAJA105M025	A	AVX
15	2	C4, C5	0.1 µF, 16 V	Capacitor, Ceramic	0805	Multi-Source
16	1	C6, C7, C11, C12	330 µF, 6 V	Capacitor, Tantalum, TPSE337M006R0100	E	AVX
17	2	C8, C9	0.01 µF, 16 V	Capacitor, Ceramic	0805	Multi-Source
18	1	C13	0.1 µF, 35 V	Capacitor, Cermaic	0805	Multi-Source

Si9140 Demonstration Board

Features

- V_{IN} = 5 V
- V_{OUT} = 2.0 to 3.5 V in 0.1 V Increments
- 5-µs Transient Response Time
- $I_O \leq 10$ A
- Switching Frequency ≈ 400 kHz
- 100-kHz Closed-Loop Converter Bandwidth

Description

The Si9140 demonstration board has been developed to assist designers to meet the full static and transient load regulation requirements of high performance microprocessors. The demonstration board is designed to regulate the output voltage within ±0.07 V for a 10-A step load. The converter output voltage can easily be set to the desired voltage (2.0 to 3.5 V in 0.1-V increments) by adjusting the four sets of binary switches (S1). The switch in the up position represents 0 = GND and in the down position represents 1 = open. (See layout diagram on page 1-282 for switch orientation.) Table 1 shows the switch setting for various output voltages. The demonstration board is capable of handling up to 10 A of continuous output current. An additional MOSFET, input capacitor, and larger inductor are required to handle currents beyond 10 A. The schematic of the demonstration board is shown in Figure 1. The Bill of Material and Component Vendor List are also provided to minimize the designer's effort.

The demonstration board layout is available in Gerber file format. Please contact your TEMIC sales representative or distributor for a copy.

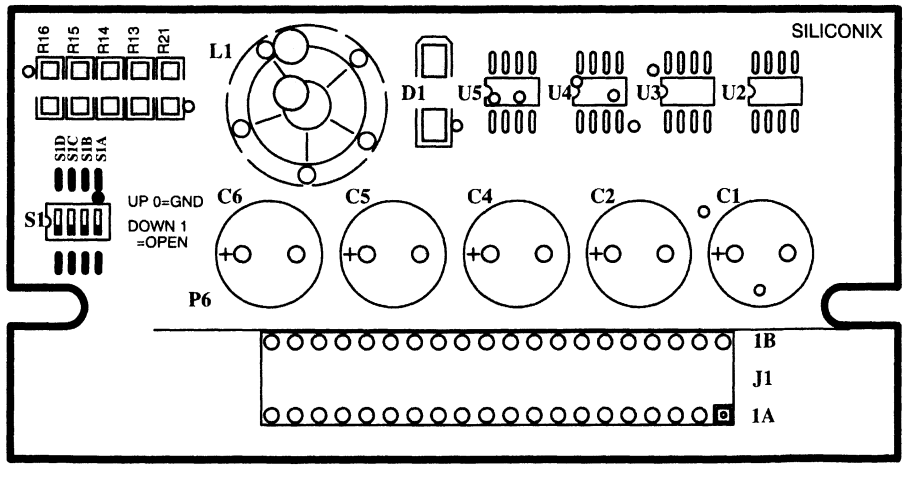
Ordering Information: Part Number Si9140DB

Power-up Check List–Installed in VRM Mother Board Socket

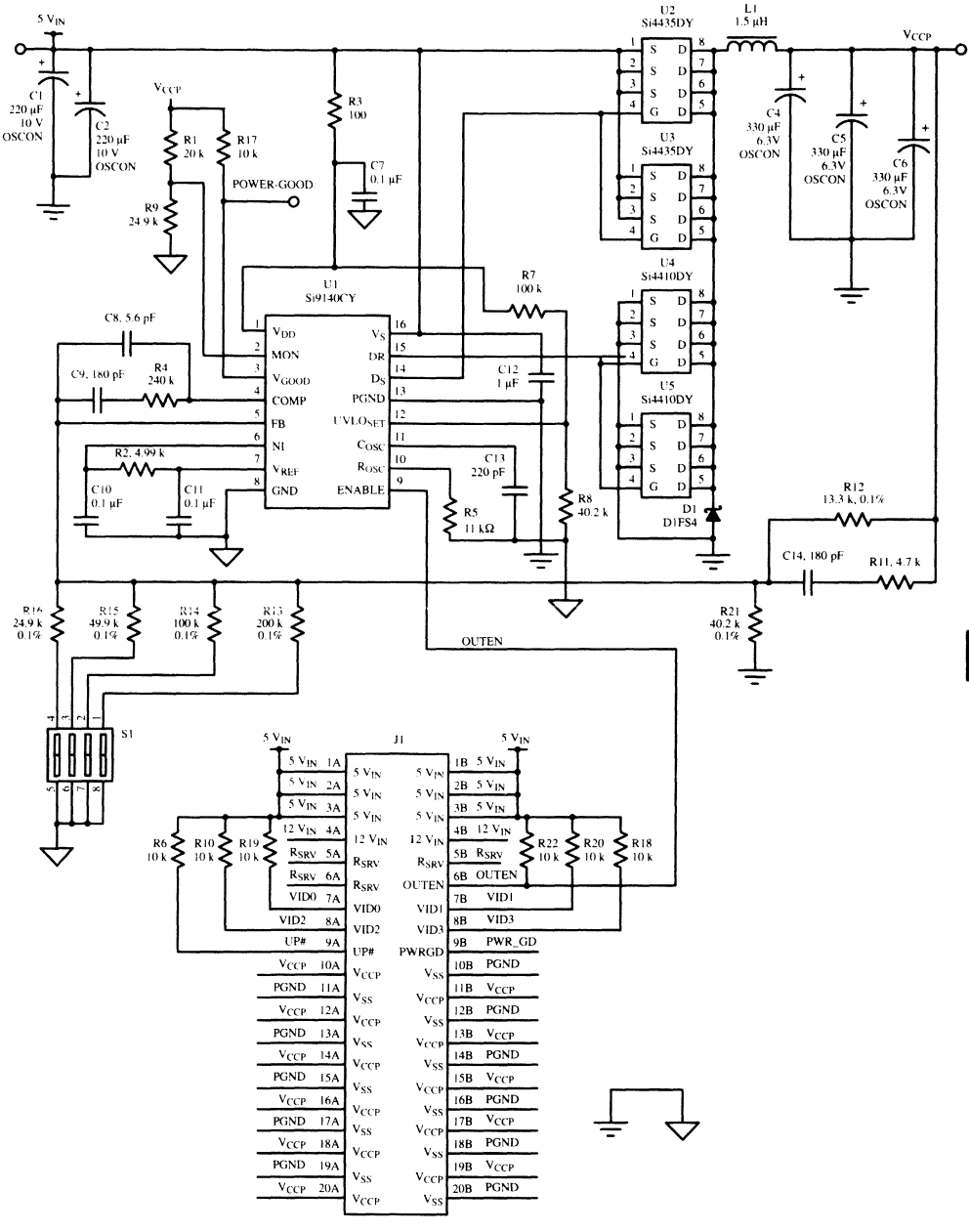
1. Verify that the microprocessor is decoupled with at least 400 µF of capacitance.
2. Adjust the dip switch positions to set the proper processor voltage as described in Table 1.
3. Turn on the main ac/dc converter to verify that +5-V input voltage is within the regulation tolerance before connecting the power supply module.
4. Turn off the main ac/dc converter and connect the power supply module to the mother board.
5. Unplug the CPU and turn on the power to the main ac/dc converter.
6. Verify that the Si9140 converter output voltage is regulating within the set voltage.
7. Power off the main ac/dc converter.
8. Insert the CPU and re-power the main ac/dc converter.

Table 1: S1 Switch Setting for Various Output Voltages

S1 Switch Setting				
S1D (R16)	S1C (R15)	S1B (R14)	S1A (R13)	V_{OUT}
1	1	1	1	2.0
1	1	1	0	2.1
1	1	0	1	2.2
1	1	0	0	2.3
1	0	1	1	2.4
1	0	1	0	2.5
1	0	0	1	2.6
1	0	0	0	2.7
0	1	1	1	2.8
0	1	1	0	2.9
0	1	0	1	3.0
0	1	0	0	3.1
0	0	1	1	3.2
0	0	1	0	3.3
0	0	0	1	3.4
0	0	0	0	3.5



Si9140CY Demo Board



Bill of Material

Part	Used	Part Type	Designators	Case Size
1	3	0.1 µF	C7, C10, C11	0805
2	1	1.5 µH	L1	Inductor
3	1	1 µF/25 V Ceramic	C12	1206
4	1	4.7 k	R11	0805
5	1	4.99 k, 1%	R2	0805
6	1	5.6 pF	C8	0805
7	7	10 k	R6, R10, R17, R18, R19, R20, R22	0805
8	1	11 k, 1%	R5	0805
9	1	13.3 k, 0.1%	R12	1206
10	1	20 k, 1%	R1	0805
11	1	24.9 k, 1%	R9	0805
12	1	24.9 k, 0.1%	R16	1206
13	1	40.2 k, 1%	R21	1206
14	1	49.9 k, 0.1%	R15	1206
15	1	100	R3	0805
16	1	100 k, 0.1%	R14	1206
17	2	180 pF	C9, C14	0805
18	1	200 k, 0.1%	R13	1206
19	1	220 pF	C13	0805
20	2	220 µF/10 V OS-CON	C1, C2	F
21	1	240 k	R4	0805
22	3	330 µF/6.3 V OS-CON	C4, C5, C6	F
23	1	D1FS4	D1	D-64
24	1	40-Pin Connector	J1	AMPMOD2
25	2	Si4410DY	U4, U5	SO-8
26	2	Si4435DY	U2, U3	SO-8
27	1	Si9140CY	U1	SO-16
28	1	SW DIP-4	S1	SO-SW
29	1	100 k, 1%	R7	0805
30	1	40.2 k, 1%	R8	0805
31	5	Spacers	302–200 BIVAR for OS-CON Caps	

Component Supplier List

Ref. Designator	Part Number	Description	Pattern	Vendor	Phone #
C1, C2	10SA220K	Os-con Capacitors	F	Sanyo	(619) 661-6835
C4, C5, C6	6.3SA330K				
D1	D1FS4	1.1 A, 40 V	IF	Shindegen	(800) 543-6525
L1	CTX07-12877-X1	1.5 µH, 10 A	OD = 0.63" HT = 0.32"	Coiltronics	(407) 241-7876
U1	Si9140CY	PWM IC	SO-16	Siliconix	(800) 554-5565
U2, U3	Si4435DY	P-Ch MOSFET	SO-8		
U4, U5	Si4410DY	N-Ch MOSFET	SO-8		
J1	2-535512-5	40-Pin Connector	AMPMOD2	AMP	(800) 522-6252
S1	GDH04S	Pole Switch	SMT-8 0.05 Pitch	Alco Switch	(508) 685-4371
	TPSE227M010R0100	220 µF	E	AVX	(207) 782-5111
	TPSE337M006R0100	330 µF			

Si9160 Demonstration Board

Features

- Synchronous Boost Converter with Efficiency up to 93%
- 1-MHz Switching Frequency
- Operates with Input Voltages of 3.0 V to 5 V
- 5-V Output at 0 A to 1.0 A

Description

The Si9160 Synchronous Boost Controller combined with high frequency Si6801 MOSFET provides efficiency up to 93% at 1-MHz switching frequency. In the past, switching frequency beyond 300 kHz was not realizable due to high switching loss in the MOSFET. The Si6801 high frequency MOSFET has been specifically designed to minimize gate charge and turn on/off delay time in order to optimize converter efficiency at 1 MHz. This high switching frequency reduces the output inductor and capacitor size without increasing the output voltage ripple. The combination of small component size and high efficiency makes Si9160 synchronous boost converter ideal for RF power amplifiers in cellular or Personal Communications Systems (PCS).

The Si9160 demo board has been configured to generate 5-V output with input voltage range of 3.0 V to 5 V. The converter efficiency is greatly enhanced by using the synchronous rectification instead of a free-wheeling Schottky diode. The Si6801 is a complementary MOSFET pair with p- and n-channel devices in a TSSOP package. The n-channel MOSFET is used as the low-side switch and p-channel is used as the high-side rectifier. The converter efficiency is further enhanced by using the 5-V output to power the Si9160 and the gate drives when the output voltage exceeds the input voltage by a diode drop.

The output voltage on the demo board can be easily changed to generate various output voltages by changing resistor value R11 as described by the equation below. Do not change resistor value R10 to generate different output voltages. This might cause instability, if the other feedback components are not adjusted to stabilize the loop. If higher current is required, inductor and MOSFET should be properly adjusted to prevent damaging the board. See the Si9160 data sheet for detailed product information.

$$R11 = 5.4k/(V_{OUT} - 1.5)$$

Included in this document are the Bill of Materials, Demo Board Schematic, and PCB layout.

The demonstration board layout is available in Gerber file format. Please contact your TEMIC sales representative or distributor for a copy.

Ordering Information: Part Number Si9160DB

Power-Up Check List–Installed in VRM Mother Board Socket

1. Attach an electronic load set to either resistive or current mode to the output pins. Set the current to any level between 0 and 1.0 A. Alternatively, you can use a resistor of value between 5 Ω and 1 MΩ.
2. Attach a 2.7- to 5-V supply and ground to the pins on the left side of the board. This can be done with a grabber to one each of the two pins; it is not necessary to use all four pins.
3. Put an oscilloscope ground on the input ground, and the Ch1 probe on pin 1 of the Si6801 (the MOSFET drain). Connect the Ch2 probe on pin 14 of Si9160 and Ch3 probe on pin 15 of Si9160. Set the oscilloscope at 5 V/div and 500 nsec/div; the result will appear approximately as shown in Figure 1.
4. To synchronization to external clock frequency, connect square wave clock to pin 3 to ground on connect pin marked with "S". External clock frequency should be faster than the free running converter frequency. The converter frequency is synchronized during high to low transition.

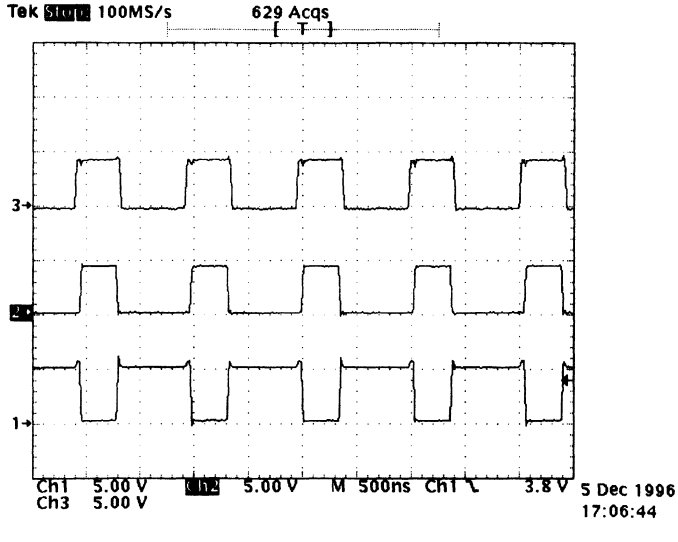


Figure 1. Ch1 – Drain to ground voltage on pin 1 of Si6801.
Ch2 – Low side switch gate drive voltage on pin 14 of Si9160.
Ch3 – High-side rectifier gate drive voltage on pin 15 of Si9160.

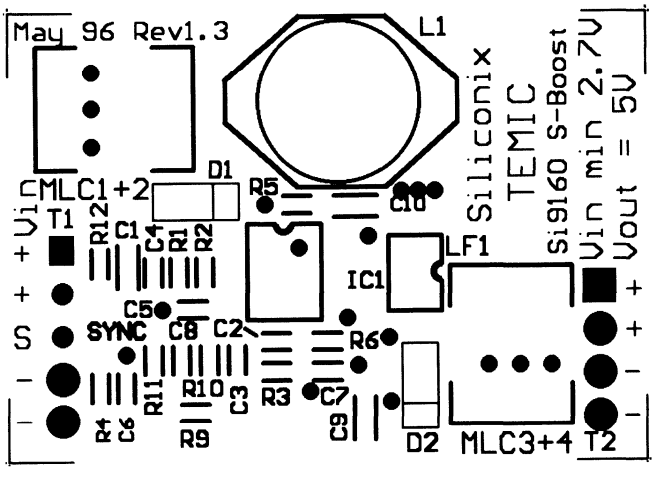


Figure 2. Silk Screen

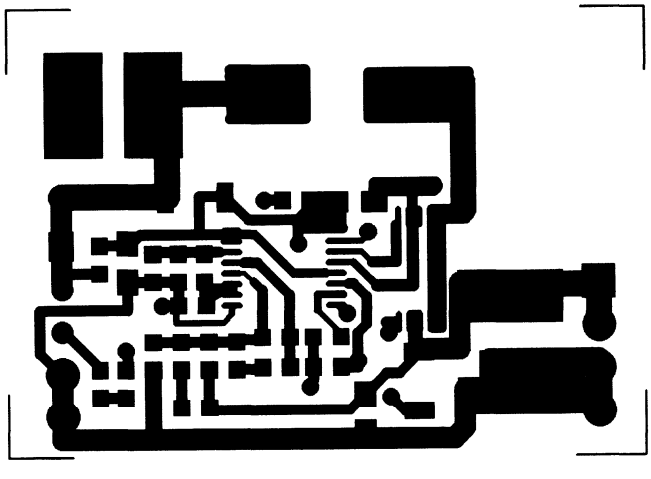


Figure 3. Top Layer

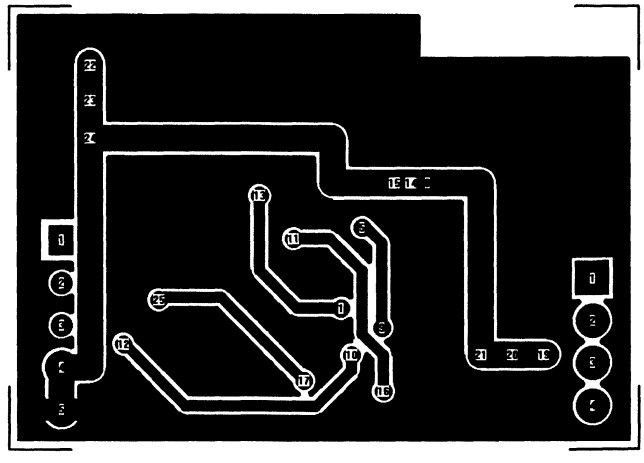


Figure 4. Bottom Layer

Si9160DB Application Circuit

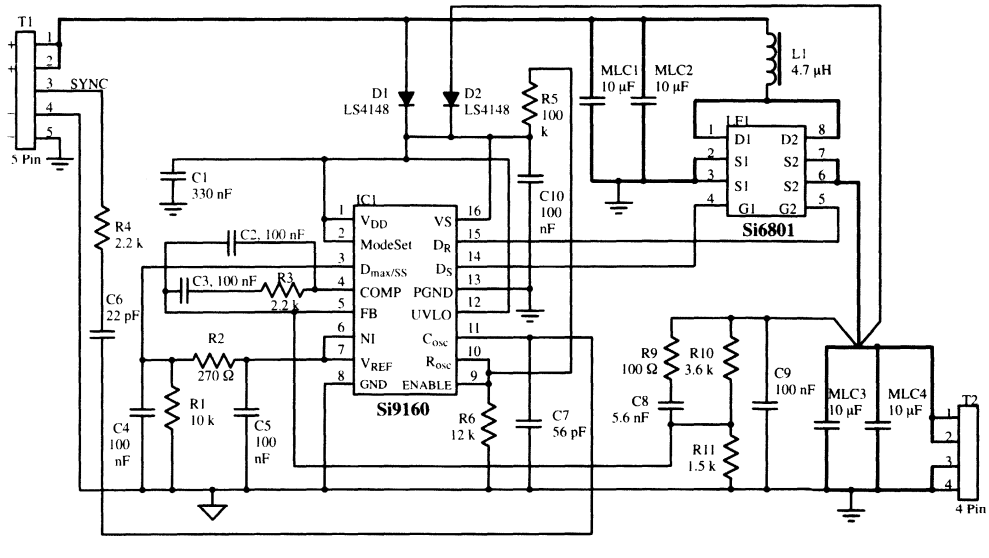


Figure 5. Si9160 Synchronous Boost converter for Mobile/Cellular Commication

Specification

2.7 to V_{OUT}-0.1 V (7 V max)
5 V_{OUT} at 1A (can be pulsed to a higher current such as GSM PA 5 V at approx. 1.6 A at 1/7 duty cycle)
f=1 MHz (can be set up to 1.8 MHz with RC change)

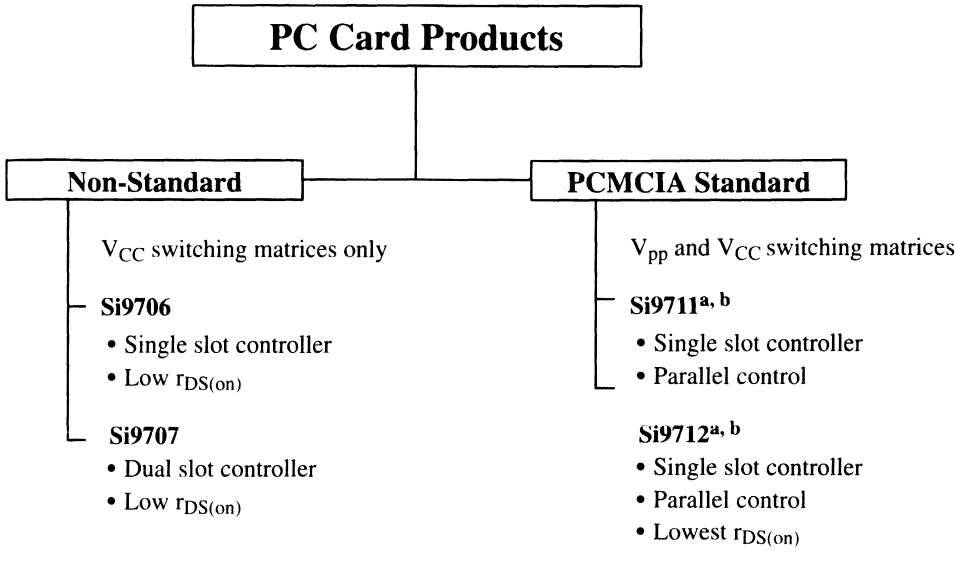
Bill of Material for Si9160 Synchrounous Boost Converter

Part	Used	Reference Designators	Part Type	Description/ Part Number	Pattern	Manufacturer
1	1	C1	330 nF	Capacitor, 330 nF	0805	Multi-Source
2	5	C2-C5, C10	100 nF	Capacitor, 100 nF	0805	Multi-Source
3	1	C6	22 pF	Capacitor, 22 pF	0603	Multi-Source
4	1	C7	56 pF	Capacitor, 56 pF	0603	Multi-Source
5	1	C8	5.6 nF	Capacitor, 5.6 nF	0603	Multi-Source
6	1	C9	100 nF	Capacitor, 100 nF	0805	Multi-Source
7	2	D1, D2	LS4148	Diode, LS4148	LS4148	Multi-Source
8	1	IC1	Si9160	Sync Boost	TSSOP-16	Siliconix
9	1	L1	DO3316P-472	Inductor, 4.7 µH	SMDL	Coilcraft
10	1	LF1	Si6801	High-Frequency MOSFET	TSSOP-8	Siliconix
11	4	MLC1-MLC4	10 µF, 16 V	Capacitor 1210YG106ZAT	2225	AVX
12	1	R1	10 kΩ	Resistor, 10 kΩ	0603	Multi-Source
13	1	R10	3.6 kΩ	Resistor, 3.6 kΩ	0603	Multi-Source
14	1	R11	1.5 kΩ	Resistor, 1.5 kΩ	0603	Multi-Source
15	1	R2	270 Ω	Resistor, 270 Ω	0603	Multi-Source
16	1	R3	2.2 kΩ	Resistor, 2.2 kΩ	0603	Multi-Source
17	1	R4	2.2 kΩ	Resistor, 2.2 kΩ	0603	Multi-Source
18	1	R5	100 kΩ	Resistor, 100 kΩ	0603	Multi-Source
19	1	R6	12 kΩ	Resistor, 12 kΩ	0603	Multi-Source
20	1	R9	100 Ω	Resistor, 100 Ω	0603	Multi-Source
21	1	T1	5 Pin	5-Pin Header	SIP5	Multi-Source
22	1	T2	4 Pin	4-Pin Header	SIP4	Multi-Source

Power Management Selector Guide

Part Number	Package	Description	Switching		12-V Suspend Capability	V_{CC} Rise TIme	Mamimum On-Resistance (T_A = 25°C)		Page Number
			V_{CC}	V_{P-P}			V_{CC} (I = 500 mA)	V_{P-P} (I = 120 mA)	
PC Card									
Si9706DY	SO-8	PCMCIA Interface Switch	X			Programmable	70 mΩ	n/a	2-22
Si9707DY	SO-16	PCMCIA Dual Interface Switch	X			Programmable	70 mΩ	n/a	2-26
Si9712DY	SO-16	PCMCIA Interface Switch	X	X	X	Programmable	70 mΩ	150 mΩ	2-36
Si9711CY	SO-16	PCMCIA Interface Switch	X	X		200 µs (min)	200 mΩ	300 mΩ	2-30

Product Family Tree



Notes

a. Demo board available
b. New product

Dual-Cell Lithium Ion Battery Control IC

Features

- Over-Charge Protection
- Over-Discharge Protection
- Short Circuit Current Limiting
- Battery Open-Circuit Center Tap Protection
- Cell Voltage Balancing
- Undervoltage Lockout
- Individual Cell Voltage Monitoring
- Low Operating Current (30 µA) and Shutdown Current (1 µA)
- Internal N-Channel MOSFET Driver
- High Noise Immunity
- Accurate (± 1.19%) Over-Charge Voltage Detection
- Three different cell types covered

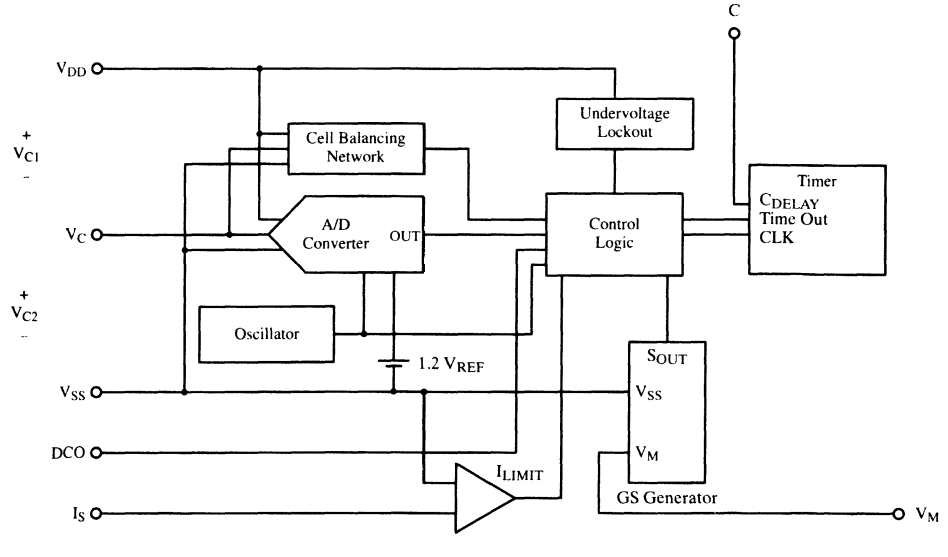
Description

The Si9730 monitors the charging and discharging of dual-cell lithium-ion battery packs ensuring that battery capacity is fully utilized while ensuring safe operation. The Si9730 provides protection against overcharge, over-discharge, and short circuit conditions which are hazardous to the battery and the environment.

Battery voltages of each individual cell are monitored at the center-tap connection by an internal A/D converter through the V_C pin. If one or both of the cells is determined to be overcharged, an internal cell balancing network "bleeds" off current at 15 µA until both cells are charged to the same maximum level. Depending on the condition of each cell, the Si9730 will switch two external source-connected n-channel MOSFETs on or off to allow the cells to be charged or to provide current to the load.

The Si9730 is available in an 8-pin SOIC package with an operating temperature range of –25 to 85°C.

Functional Block Diagram



Absolute Maximum Ratings

V_M ..... V_{DD} –15 V to V_{DD} +15 V
V_{DD} ..... V_{SS} –0.3 V to V_{SS} +12 V
V_C ..... V_{SS} –0.3 V to V_{DD} +0.3 V
I_S ($V_{SS} \geq V_M$) ..... V_M –0.3 V to V_{DD} +0.3 V
($V_M \geq V_{SS}$) ..... V_{SS} –0.3 V to V_{DD} +0.3 V

Maximum Operating Junction Temperature ..... 125°C
Power Dissipation ..... 200 mW
Thermal Impedance ($P_{\Theta JA}$) ..... 80°C/W
Storage Temperature ..... –55 to 150°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Range

C_{VC} < 10 pF from V_C to V_{DD} and V_{SS}, Total
C_D ..... Open to 1.0 µF
R_{IS} series resistance to sense resistor ..... < 27 kΩ
DCO Load Capacitance ..... 0 to 2000 pF

V_{DD} to V_{SS} ..... 9 V
V_{DD} to V_M ..... 12 V
Operating Temperature Range ..... –25 to 85°C

Specifications

Parameter	Symbol	Test Conditions Unless Otherwise Specified		Limits T_A = –25 to 85°C Min[a]	Typ[b]	Max[a]	Unit
Power Supply							
Supply Current, Charging Operation	I_{DD_C}	$V_{C1} = V_{C2}$ = 2.6 V, $V_{DD} - V_M$ = 8.4 V				60	µA
Supply Current, Normal Operation	I_{DD}	$V_{C1} = V_{C2}$ = 4.05 V, $V_M = V_{SS}$				30	µA
	I_{DD_UVL}	$V_M = V_{DD}$, $V_{C1} = V_{C2}$ = 1.7 V				1	µA
Undervoltage Lockout Threshold	V_{UVL}	Measured at $V_{DD} - V_{SS}$ (Falling) $V_{C1} = V_{C2}$, $V_{DD} - V_M$ = 5.5 V		3.5	3.7	4.0	V
V_M Leakage Current	I_{VM_UVL}	$V_{C1} = V_{C2}$ = 1.7 V, $V_{DD} = V_M$				1	µA
V_M Operating Current	I_{VM}	$V_{C1} = V_{C2}$ = 2.6 V, $V_{DD} - V_M$ = 8.4 V				30	µA
Control Logic							
DCO Output High Voltage	V_{OH}	I_{OH} = –10 µA, $V_{C1} = V_{C2}$ = 3.3 V $V_{DD} - V_M$ = 6.6 V		V_{DD} – 0.1			V
DCO Rise Time (10% to 80%)	t_r	V_{C1} = 2 V, V_{C2} = 2.4 V $V_{DD} - V_M$ = 8.4 V C_L = 500 pF DCO to V_{SS}				7.5	µs
DCO Fall Time (80% to 10%)	t_f					1	µs
DCO Output Low Voltage	V_{OL}	I_{OL} = 10 µA	$V_M = V_{DD}$ V_{C1} = 2 V V_{C2} = 2.4 V			V_{SS} +0.4	V
			$V_M = V_{SS}$ $V_{C1} = V_{C2}$ = 4.4 V $I_S = V_{DD}$			V_M +0.52	V
Analog Section							
Current-Limit Comparator Trip Point	V_{ILIMIT}	$V_{C1} = V_{C2}$ = 4.05 V, $V_M = V_{SS}$ + 0.25 V I_S Rising, T_A = 25°C		25.5	28	32	mV
Current Limit Comparator Temperature Coefficient	dV_{ILIMIT}/dT				0.18		%/°C
Current-Limit Comparator Response Time	t_{ILIMIT}	$V_{C1} = V_{C2}$ = 3.3 V, $V_M = V_{SS}$ + 0.25 V C_L = 50 pF, DCO to V_{SS}, See Figure 2				25	µs
Current Limit Comparator Input Bias Current	I_{IS}	$V_{C1} = V_{C2}$ = 3.3 V, $V_{DD} = V_M$, $V_{IS} = V_{SS}$		–125			nA

Specifications

Parameter		Symbol	Test Conditions Unless Otherwise Specified		Limits T_A = −25 to 85°C Min[a]	Typ[b]	Max[a]	Unit
Analog Section (cont'd)								
Over-Charge Detect Threshold (Rising)	A Suffix	V_{OC1} Cell 1	V_{C2} = 4.05 V, $V_{DD} - V_M$ = 8.6 V	T_A = 25°C	4.15	4.20	4.25	V
				T_A = −25°C	4.1		4.27	
				T_A = 85°C	4.1		4.27	
		V_{OC2} Cell 2	V_{C1} = 4.05 V, $V_{DD} - V_M$ = 8.6 V	T_A = 25°C	4.15	4.20	4.25	
				T_A = −25°C	4.1		4.27	
				T_A = 85°C	4.1		4.27	
	B Suffix	V_{OC1} Cell 1	V_{C2} = 4.05 V, $V_{DD} - V_M$ = 8.6 V	T_A = 25°C	4.2	4.25	4.3	
				T_A = −25°C	4.15		4.32	
				T_A = 85°C	4.15		4.32	
		V_{OC2} Cell 2	V_{C1} = 4.05 V, $V_{DD} - V_M$ = 8.6 V	T_A = 25°C	4.2	4.25	4.3	
				T_A = −25°C	4.15		4.32	
				T_A = 85°C	4.15		4.32	
	C Suffix	V_{OC1} Cell 1	V_{C2} = 4.05 V, $V_{DD} - V_M$ = 8.6 V	T_A = 25°C	4.18	4.22	4.25	
				T_A = −25°C	4.12		4.3	
				T_A = 85°C	4.12		4.25	
		V_{OC2} Cell 2	V_{C1} = 4.05 V, $V_{DD} - V_M$ = 8.6 V	T_A = 25°C	4.18	4.22	4.25	
				T_A = −25°C	4.12		4.3	
				T_A = 85°C	4.12		4.25	
Over-Charge Threshold Difference		$\lvert V_{OC1} - V_{OC2} \rvert$					20	mV
Over-Charge Detect Threshold Hysteresis[c]	Cell 1	V_{OC_H1}	$V_{DD} - V_M$ = 8.6 V	V_{C2} = 4.05 V			10	
	Cell 2	V_{OC_H2}		V_{C1} = 4.05 V			10	
Over-Discharge Detect Threshold (Falling)	Cell 1	V_{ODC1}	$V_M = V_{SS}$	V_{C2} = 2.6 V	2.1	2.2	2.3	V
	Cell 2	V_{ODC2}		V_{C1} = 2.6 V	2.1	2.2	2.3	
Cell Balancing Current	Cell 1	I_{BAL1}		V_{C1} = 4.4 V, V_{C2} = 4.05 V	9	15	30	µA
	Cell 2	I_{BAL2}		V_{C2} = 4.4 V, V_{C1} = 4.05 V	9	15	30	
Timer Charge Current		$I_{TIMER(C)}$	V_{C2} = 3.3 V, $V_M = V_{SS}$, $V_C = V_{SS}$, T_A = 25°C			−0.5		µA
Timer Discharge Current		$I_{TIMER(D)}$	$V_{C1} = V_{C2}$ = 3.3 V, $V_{DD} = V_M$, $V_{DD} - V_C$ = 6.1 V, T_A = 25°C			1.0		mA
DL2 Time (Over-Charge)		t_{DL2OC}	V_{C1} = 4.05 V, $V_{DD} - V_M$ = 10 V, C_D = 500 pF, T_A = 25°C, See Figure 4		27	40	60	ms
DL2 Time (Over-Discharge)		t_{DL2ODC}	V_{C1} = 2.6 V, $V_M = V_{SS}$, C_D = 500 pF, T_A = 25°C, See Figure 5		27	40	60	
External Short Circuit Sense Current		$I_{VMSHORT}$	$V_{C1} = V_{C2}$ = 4.4 V, $V_M = V_{DD}$		30		300	µA
Reset Threshold		V_{RTH}	$V_{C1} = V_{C2}$ = 4.05 V, See Figure 3		42	60	100	mV
Center Tap, Average Bias Current		I_{VC}	$V_{C1} = V_{C2}$ = 4.05 V, $V_M = V_{DD}$		−2		2	µA
Overcharge Load Detect		t_{OCC}	$V_{C1} = V_{C2}$ = 4.4 V, C_D = 500 pF, C_L = 500 pF, DCO to V_{SS}, See Figure 1				40	µs
Power-Down Charger Detect Threshold		V_{CHPD}	V_{C1} = 2 V, V_{C2} = 2.4 V, See Figure 6				1.1	V
DCO Pulse Width		t_{PW}	C_L = 500 pF, DCO to V_{SS}, See Figure 7			520		µs

Notes
a. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum.
b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
c. Guaranteed by design, not subject to production test.

Timing Diagrams (Cont'd)

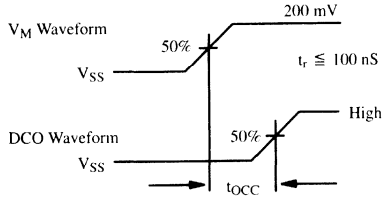


Figure 1. OC Load Detect

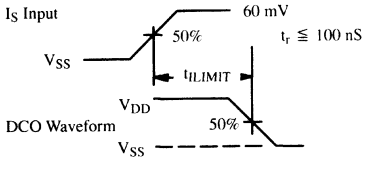
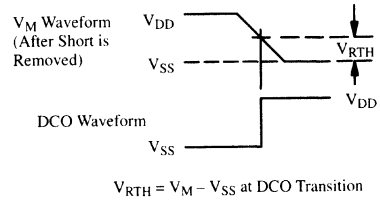
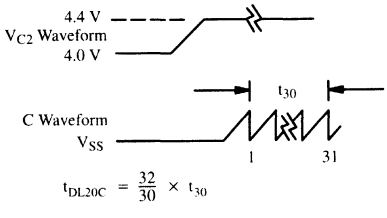


Figure 2. Current-Limit Comparator Response Time



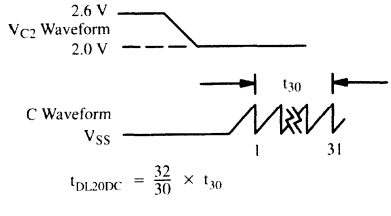
$V_{RTH} = V_M - V_{SS}$ at DCO Transition

Figure 3. Reset Threshold



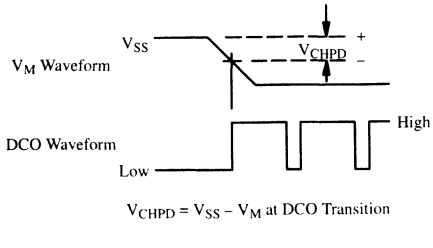
$t_{DL20C} = \frac{32}{30} \times t_{30}$

Figure 4. DL2 Time (Over-Charge)



$t_{DL20DC} = \frac{32}{30} \times t_{30}$

Figure 5. DL2 Time (Over-Discharge)



$V_{CHPD} = V_{SS} - V_M$ at DCO Transition

Figure 6. Power-Down Charger Detect Threshold

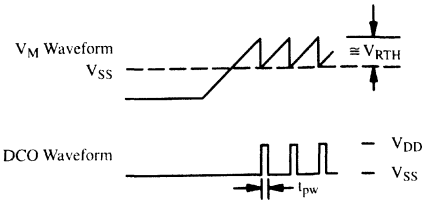
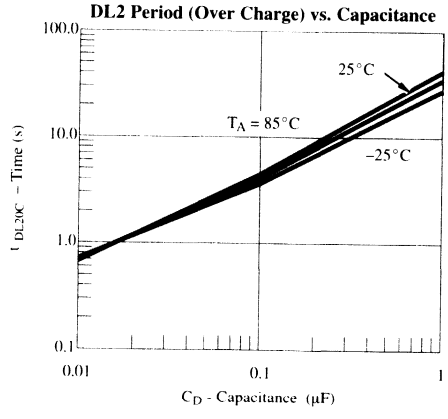


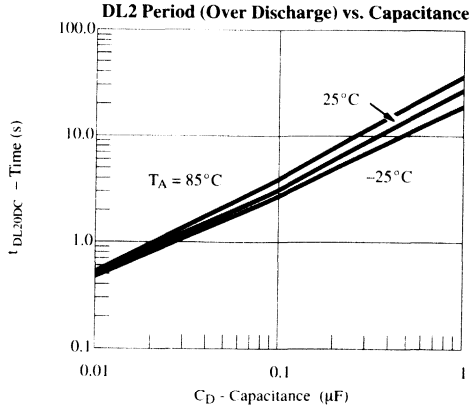
Figure 7. Load Detection in Overcharge Mode

Typical Characteristics (25°C Unless Noted)

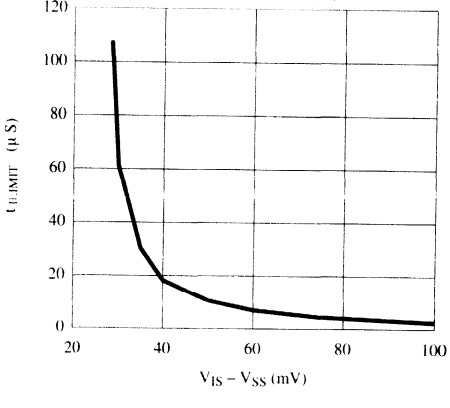
DL2 Period (Over Charge) vs. Capacitance



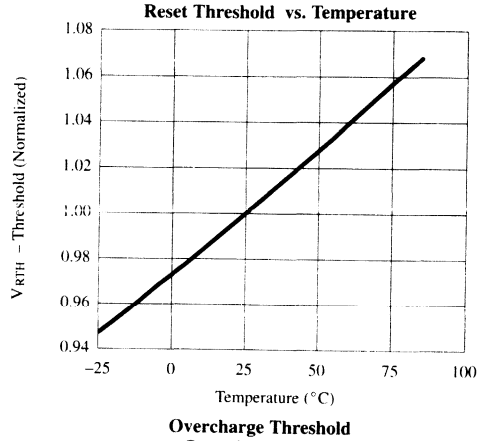
DL2 Period (Over Discharge) vs. Capacitance



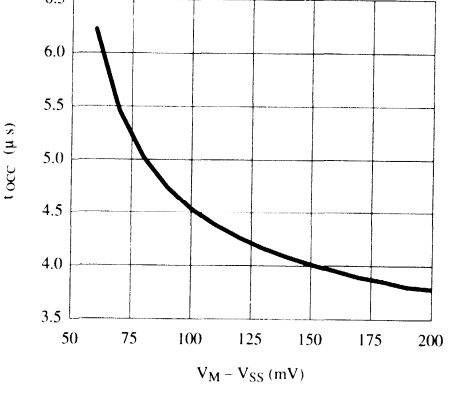
Over Current Sense Voltage vs. Current Sense Time



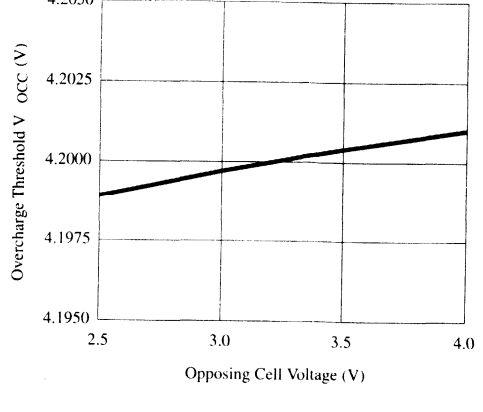
Reset Threshold vs. Temperature



Load Detect Time vs. $V_M - V_{SS}$

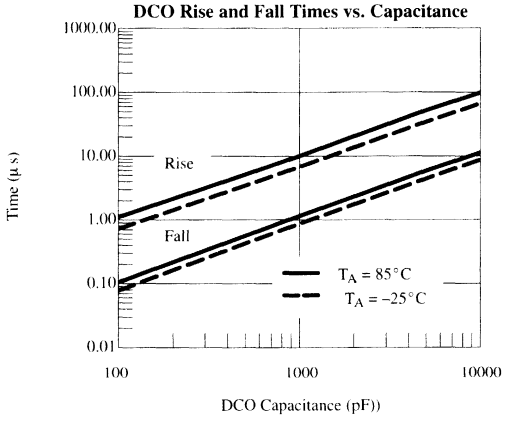


Overcharge Threshold vs. Opposing Cell Voltage

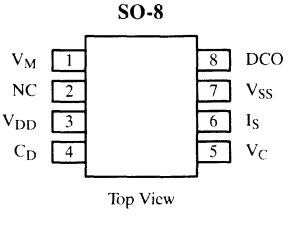


2 Power Management

Typical Characteristics (25°C Unless Noted) (Cont'd)



Pin Configuration



Pin Number	Symbol	Description
1	V_M	Negative Battery Pack Terminal - connection for external negative terminal of the battery pack.
2	NC	No Connection, do not connect this pin.
3	V_{DD}	Dual Cell Positive Terminal - connection for positive terminal of dual series connected LiI+ cells.
4	C_D	Delay Capacitor Connection - an external capactior connected across C_D and Vss allows additional charge time (DL2, see Detailed Description) after a charge error has occured. Suggested capacitor values are shown in DL2 Period vs. Capacitance Curves.
5	V_C	Dual Cell Center Tap Connection - monitors individual battery voltages for overcharge and overdischarge errors.
6	I_S	Current Sense Comparator Input - monitors load current for short circuit conditions . If V_{ILIMIT} is exceeded, then DCO opens the low-side switch, disconnecting the cells.
7	V_{SS}	Dual Cell Negative Terminal - connection for negative terminal of dual series connected LiI+ cells.
8	DCO	Low-side Switch Gate Driver Output - drives the gate of two external source connected n-channel MOSFETs. DCO swings from V_{OL} to V_{DD}.

Detailed Description

Overview

The purpose of the Si9730 is to safely and reliably control the charging and discharging of a two-cell lithium-ion battery. It provides protection against all possible fault conditions, including:

- external short circuits
- reversed charger
- overcharged cell or cells
- undervoltage
- battery open center-tap

General Concepts

The Si9730 operates by connecting or disconnecting the negative terminal of the battery to the negative side of the load and/or charger (see Figure 8); that is, it does ground side switching. It is important to bear the distinction between these two "grounds" in mind in order to understand the operation of the Si9730. The switching is accomplished by controlling two "back-to-back" MOSFETs: having the two MOSFETs in this arrangement is mandatory to ensure that current cannot flow in either direction when the MOSFETs are off. To turn the switch on, the Si9730 applies a gate-source voltage to both MOSFETs (from the DCO pin) that is high with respect to the sources. The Si9730 DCO signal is referenced to the V_M pin while the battery is being charged, and to the Vss pin while the battery is being discharged. The Si9730 causes the DCO to be referenced to the lower of the two voltages. This prevents the switch from turning on or off unintentionally.

The Si9730 is designed to operate only with a current-limited lithium-ion battery charger. Specifically, the battery charger must have an open-circuit voltage that does not exceed the absolute maximum IC voltage, and it must have a limited short-circuit current that does not exceed the allowed charging current of the battery.

The following descriptions cover all the common operational scenarios; additional information on unusual battery conditions can be found in the state transition table.

Normal Charging

The cells are in normal charging conditions if a) both cells are above the Over-Discharge Detect Threshold (V_{ODC} ~ 2.2 V); b) both cells are under the Over-Charge Detect Threshold (V_{OC} ~ 4.2 V); and c) the center tap is connected to the V_C pin. When a charger is present in these conditions, the switch will be on, charging the cells at the current limit of the charger.

Normal Discharging

The cells are in normal discharging conditions if a, b, and c above are satisfied, and if in addition d) the load current is less than the discharge current limit. With no charger present, the switch will be on, discharging the cells and powering the load.

Overcharged Cell(s) Charging

The most destructive condition that a LiI+ cell can experience is overcharging. If the cell becomes overcharged beyond its recommended limits, it can become permanently disabled.

If one or both cells rise above the over-charge detect threshold (V_{OC1} and V_{OC2}), and a charger is present, the Si9730 will open the switch (to prevent further charging) and begin bleeding off charge (15-µA typical) from the overcharged cell or cells.

The details of this operation depend on the fact that the voltage level of lithium-ion batteries drops for a short time after charging ceases (due to momentary changes in battery chemistry, ESR, etc.). Because of this recovery, the Si9730 allows the battery to continue charging for a short time (the overcharge time, t_{DL2OC}). This additional charge time only occurs if the overcharge condition persists for more than 8 msec (two periods of an internal 4msec oscillator). T_{DL2OC} is determined by the capacitor attached to the C_D pin, see Figure 8.

Once the overcharge time has ended, the switch is opened, preventing the battery from further overcharging. Now, the Si9730 begins bleeding current off the overcharged cell or cells (I_{BAL1} and I_{BAL2}), as long as a charger is present. Eventually, the cell(s) will return into their normal range, and charging will begin, starting the whole cycle over again.

Overcharged Cell(s) Discharging

If one or more cells is overcharged, and a load is connected, the switch is turned on, permitting the battery to power the load.

Over-Discharged Cell(s) Discharging

Repeated over-discharging of LiI+ cells can cause irreversible reactions in the cells which lead to decreased cycle life.

To avoid this, if one or both cells becomes over-discharged ($V_{CELL} < V_{ODC}$) and no charger is present, the Si9730 opens the switch to prevent further discharging, and goes into a shutdown mode in which it draws minute power from the battery ($I_{DD\_UVL} < 1$ µA).

Over-Discharged Cell(s) Charging

If one or both cells is over-discharged, and a charger is present, charging can begin, and so the Si9730 closes the switch. However, removal of the charger in this condition could potentially damage the battery if the removal is not recognized and the cells are discharged. Since the voltage drop across the switch is small, the Si9730 actually cycles the switch at a 7/8 duty cycle; during the 1/8 time when the switch is open, the IC checks that the charger is still present.

Once both cells are back into the normal operating range, normal charging resumes.

Undervoltage Charging

If for some reason the battery drops below about 3.7 V (V_{UVL}), there is insufficient voltage for the Si9730 to properly monitor fault conditions. Of course, the switch is already open, since $V_{UVL} < V_{ODC} \times 2$. However, when a charger is detected, the Si9730 recovers and goes into an undervoltage mode. (A charger is detected if the V_S pin is higher than the V_M pin by at least $V_{CHPD} = 1.1$ V, see Figure 6). In this undervoltage mode, the switch is on at a 1/8 duty cycle, to limit the power dissipation across the switch, and, again, to detect the continuing presence of the charger.

Once the battery voltage is above V_{UVL}, the charging continues in the over-discharged state.

Output Short

If too much current is drawn from the battery due to a load short, the switch must be opened quickly to prevent damage to the battery. The Si9730 monitors the load current by looking at the voltage across an external sense resistor (see Figure 8). If the voltage across the sense resistor exceeds $V_{ILIMIT} \sim 28$ mV, the switch is opened. The Si9730 leaves the switch open until the load is *completely* removed.

Of course, the IC must have some way of detecting that the load *has* been removed. For this purpose, a small current ($I_{VMSHORT}$) passes through the Si9730, from pin V_M to pin V_{SS} once the short is detected and the switch is turned off. The $I_{VMSHORT}$ current causes the voltage on the V_M pin to equal the voltage on the V_{DD} pin while the short is present, or the voltage on the V_M pin to equal the voltage on the V_{SS} pin if the short is removed. If the short is not removed, $I_{VMSHORT}$ current will continue to flow until the battery voltage becomes overdischarged. Once the short is removed, the IC is allowed to turn the switch back on.

The current limit threshold has a temperature coefficient of 0.18%/°C. This can partially compensate for a copper circuit board trace being used as the sense resistor.

Open Center Tap

An open center tap is a mechanical failure of the battery pack such that the Si9730's V_C pin is disconnected from the center point of the two-cell battery. If this connection is open, the IC opens the switch, as it cannot measure the cell voltages in this condition. The switch is left open until connection is re-established. If the battery is under-voltaged and the charger is present in this case, the battery is allowed to charge even with the center tap open. In this state, batteries are almost impossible to damage by 1/8 duty cycle charging. Once the battery voltage reaches the over-discharged voltage, the switch is turned off.

State Transition Table

The number of different states of the Si9730 can seem overwhelming at first. This state transition table will help to organize thinking about the different operational conditions of the IC, by listing each possible transition from one condition to another.

Reading the table is straightforward. There are two cells constituting the battery, one with its positive terminal connected to V_{DD} and its negative terminal connected to V_C, referred to as the high cell (see Figure 8); and one cell with its positive terminal connected to V_C and its negative terminal connected to V_{SS}, referred to as the low cell. Each cell can be in one of three voltages:

- Over-discharge (ODC), where $V_{CELL} < V_{ODC}$;
- Normal Operation (NO), where $V_{ODC} < V_{CELL} < V_{OC}$;

or

- Overcharge (OC), where $V_{OC} < V_{CELL}$.

Additionally, the battery as a whole can be undervoltage (UV), where $V_{BATTERY} < V_{UVL}$. Note that this final condition is not *necessarily* (though normally) mutually exclusive with the other cell conditions: if one cell were at 0V, the other cell could be in NO, and the battery could still be in UV.

The charger can be either present (ON) or not present (OFF); the "X" in the table means the condition is true regardless of the state of the charger. The load current can be either 0, normal ($0 < I_{LOAD} < I_{ILIMIT}$) or a short ($I_{ILIMIT} < I_{LOAD}$) where I_{ILIMIT} is set by V_{ILIMIT}/R_{SENSE}; the "X" in the table refers to a load current that can be either 0 or normal. Finally, the switch can be either ON, OFF, or cycling at either 1/8 or 7/8 duty cycle, where the duty cycle refers to the portion of the period when the switch is on; the notation On–>On simply means that the switch does not change state, it remains on; the notation –>Off means that the switch turns off regardless of its previous state.

State Transition Table

High-Cell Voltage	Low-Cell Voltage	Charger On/Off	Load Current	Switch State
NO	NO	Off>On	X	On–>On
NO–>OC	NO	Off	0	On–>Off
NO	NO–>OC	Off	0	On–>Off
NO–>OC	NO	Off	Normal	Cycles at very high duty cycle
NO	NO–>OC	Off	Normal	Cycles at very high duty cycle
OC	NO	Off–>On	X	Off–>Off
NO	OC	Off–>On	X	Off–>Off
OC	OC	Off–>On	X	Off–>Off
NO	NO	Off	Normal–>Short	On–>Off
OC	NO	Off	Normal–>Short	On–>Off
NO	OC	Off	Normal–>Short	On–>Off
NO–>ODC	NO	Off	0	On–>Off
NO	NO–>ODC	Off	0	On–>Off
NO–>ODC	NO	Off	Normal	On–>Off
NO	NO–>ODC	Off	Normal	On–>Off
ODC	NO	Off–>On	X	Off–>Cycle at 7/8 duty cycle
NO	ODC	Off–>On	X	Off–>Cycle at 7/8 duty cycle
ODC	ODC	Off–>On	X	Off–>Cycle at 7/8 duty cycle
UV		Off–>On	X	Off–>Cycle at 1/8 duty cycle
NO–>ODC	OC	Off	0	Cycle–>Off
OC	NO–>OC	Off	0	Off
NO	NO	V<0	X	Off
UV		On	Center Tap–>Open	Cycle at 1/8 duty cycle
ODC	ODC	X	Center Tap–>Open	–.>Off
NO	ODC	X	Center Tap–>Open	–.>Off
ODC	NO	X	Center Tap–>Open	–.>Off
NO	NO	X	Center Tap–>Open	–.>Off
OC	OC	X	Center Tap–>Open	–.>Off

Application Notes

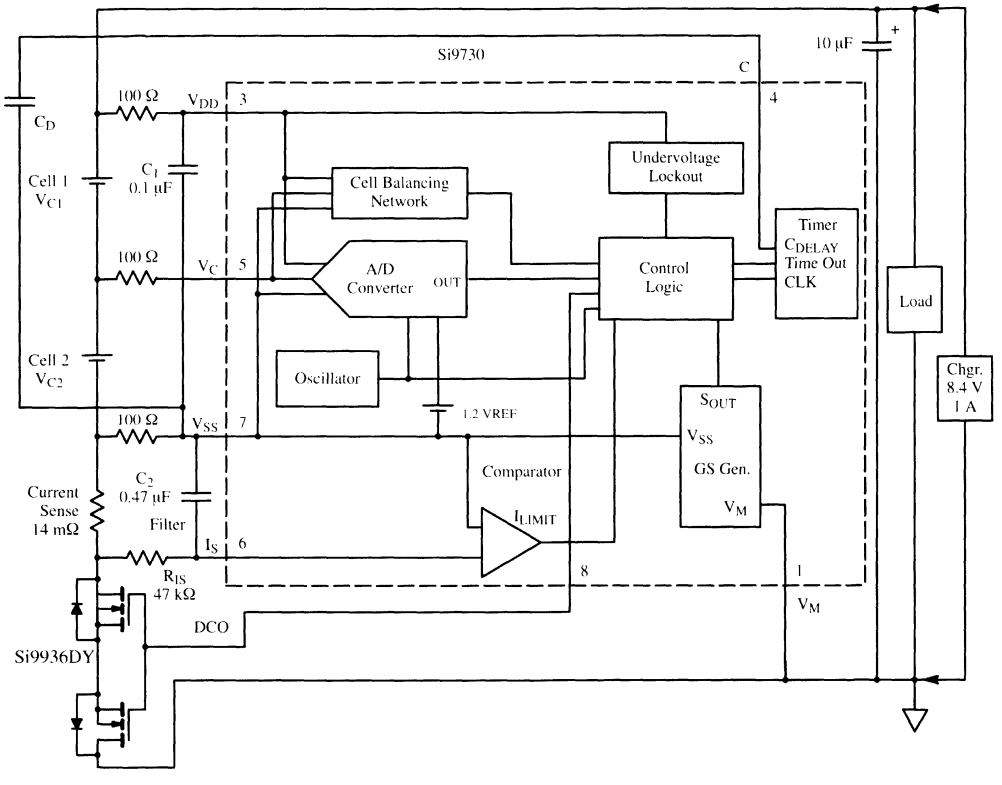


Figure 8. Typical 2 -Cell Circuit

General Considerations

Figure 8 shows a typical application of the Si9730, controlling a 2-cell lithium-ion battery. Specifics of the selection of MOSFETs, current sensing resistor, and output capacitor are detailed below. In addition, there are several typical features of this circuit to be observed.

First, each connection from a cell to the IC has a 100-Ω resistor in series with it. The purpose of the resistor is to ensure that in the unlikely event of the IC shorting, the cells themselves will not see a short. The maximum size of this resistance is set by the current drain of the IC; for example, the V_{DD} pin draws a maximum of 60 µA, which will drop V = 60 µA * 100 Ω = 6 mV across the resistor. This drop constitutes an error in the measured cell voltage, and so the resistor must be small enough that the error voltage is acceptable.

A second typical feature demonstrated in Figure 8 is the current sense filter formed by RIS and C2. This provides a noise filter, to prevent the Si9730 from opening the connection to the battery if there is noise on its current sense pin. It also causes a delay in the response of the IC to a genuine overcurrent, the amount of the delay being inversely proportional to the amount of overcurrent, since the Is pin senses a voltage. Increasing this filter's time constant could be used to allow short-time surges of current out of the battery without compromising its ability to protect the battery.

Output Capacitor

Depending on the MOSFET selected, the Si9730 can open the switch quite rapidly, in a matter of a few microseconds. However, the various monitoring operations take 10–100 times longer than this, and the basic period of the Si9730's oscillator is 4 msec. In order to prevent false readings by the Si9730, it is necessary to attach a capacitor across the output of the battery charger/load (this is *not* in parallel with the battery, because of the switch). A 10-µF capacitor is recommended for this purpose; see Figure 8.

Selecting a Current Sense Resistor

The current sense resistor should be selected based on the maximum current the battery can source or charge at; above this current, the Si9730 will open the switch, disconnecting the battery from its load or charger.

$R_{sense} = V_{ILIMIT}/I_{ILIMIT} \approx 28\ mV/I_{ILIMIT}$

Of course, the resistor must be rated to take the power dissipated in it as well:

$P_{RSENSE} = I_{ILIMIT} * V_{ILIMIT} \approx 28\ mV * I_{ILIMIT}$

For example, suppose that the maximum current the battery will see is 1.8 A. Then, I_{LIMIT} might be chosen to be 2 A. We would then select a resistor of

$R_{SENSE} = 28\ mV/2\ A = 14\ m\Omega$.

The power dissipation in this resistor is

$P_{RSENSE} = 28\ mV * 2\ A = 56\ mW$

and so a 100mW surface mount resistor would be suitable.

Another possibility is to use a thin copper trace as the sense resistor. The copper has a temperature coefficient of 0.39%/°C, but this is partially compensated for by the temperature coefficient of the current limit comparator in the Si9730, which is 0.18%/°C. A simple formula for selecting a trace to act as a current sensor is:

$$R = 0.5\ m\Omega \times \frac{\text{length}}{\text{width}}\ (1\ \text{oz. Copper})$$

For example, to get a 14-mΩ resistor, we need length/width = 28; with a trace width of 0.01", the length of the trace should be 0.28".

MOSFET Selection

Two MOSFETs in series, with their sources and gates connected together, are used as the switch. This prevents current from flowing in either direction when the gate is low; if only one MOSFET were used, the body diode could conduct current in the opposing direction.

LITTLE FOOT MOSFETs are recommended for this application, because of their size, performance and cost benefits. SO-8 and TSSOP-8 MOSFETs allow for space efficient designs with performance equal to or better than their DPAK and TO-220 predecessors. Further, their availability from multiple sources permits a cost effective solution.

There are two important parameters to consider in MOSFET selection: gate threshold voltage; and on-resistance, which determines power dissipation.

Even when the DCO pin of the Si9730 is low, the specification allows its value to be as high as 0.4 V. If this voltage were close to the gate threshold voltage, leakage current through the MOSFETs could be hundreds of microamps, which would result in the battery quickly becoming discharged. To ensure that leakage is minimized, n-channel MOSFETs with a minimum gate threshold voltage of 0.8 V should be chosen.

On resistance of the MOSFETs needs to be selected to limit power dissipation into the MOSFETs' package. For example, a dual MOSFET SO-8 package is rated at 2 W, and a dual MOSFET TSSOP-8 package is rated at 1 W (both at 25°C; if the ambient temperature is higher, the allowable power dissipation in these packages is less). For example, if the maximum current is 2 A, and a dual MOSFET SO-8 package is being used, the maximum on-resistance of the two MOSFETs in series must not exceed

$1\ W = (2\ A)^2 * R_{ON}$

or $R_{ON} = 0.25\ \Omega$; each MOSFET can be allotted half of this, $R_{ON} = 125\ m\Omega$. Account must also be taken of the fact that MOSFETs' on-resistance is a function of temperature; a conservative approach would give a discount of 1/3, $R_{ON} = 125\ m\Omega * (2/3) = 80\ m\Omega$ per MOSFET.

A list of recommended MOSFETs, which TEMIC Semiconductors supplies, can be found on page 2-14.

N-Channel MOSFET Selection Guide

Part Number	$r_{DS\ (on)}(\Omega)$ @ V_{GS} = 10 V	$r_{DS(on)}(\Omega)$ @ V_{GS} = 4.5 V	I_D(A)	$V_{GS(th)}$ (V)	Config.	Package	Recommended Application Current (A) @ 25°C
Si4410DY	0.0135	0.020	10	1.0	Single	SO-8	9
Si4412DY	0.028	0.042	7	1.0	Single	SO-8	6.3
Si6434DQ	0.028	0.042	5.6	1.0	Single	TSSOP-8	4.9
Si4936DY	0.037	0.055	5.8	1.0	Dual	SO-8	3.5
Si9936DY	0.050	0.080	5	1.0	Dual	SO-8	2.9
Si6954DQ	0.065	0.095	3.9	1.0	Dual	TSSOP-8	1.9

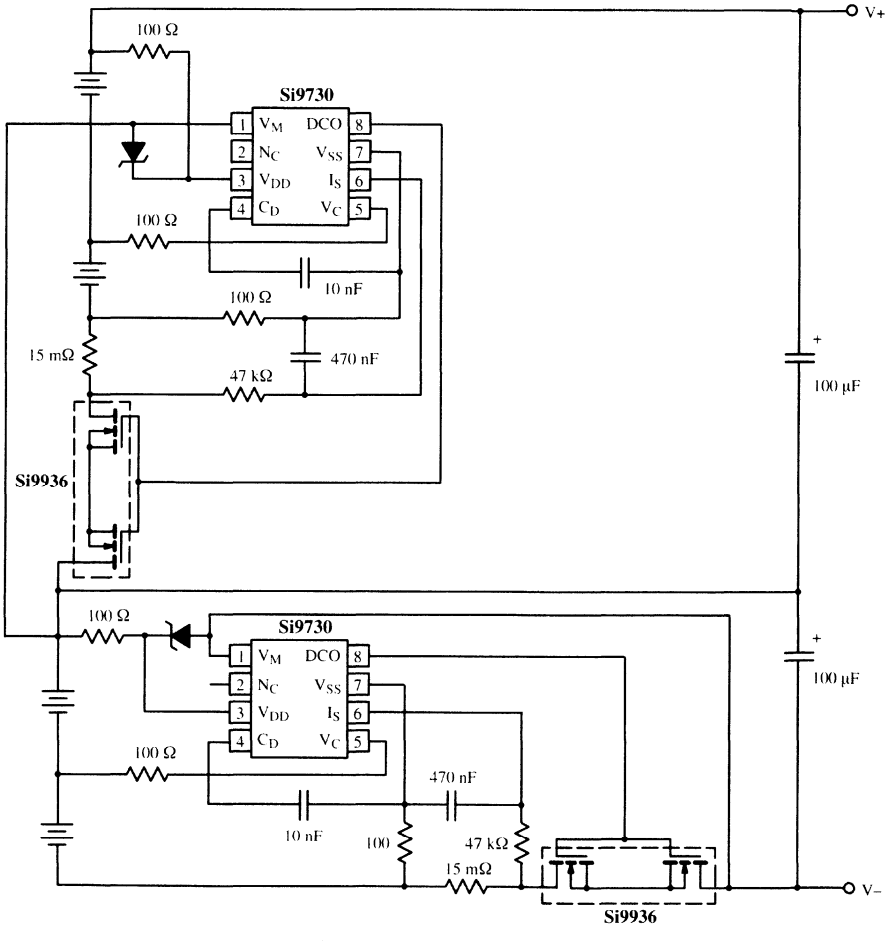


Figure 9. 4-Cell Battery Circuit

Four Cell Application

Figure 9 shows a method for using the Si9730 in a 4-cell application. Basically, this is two complete 2-cell circuits stacked in series. Each half of the complete circuit monitors its own 2-cell portion of the battery, and opens its own MOSFET switch under any of the appropriate conditions. Observe that the total percent power loss in this circuit is identical to that in the 2-cell application; although there are now two sets of MOSFETs in series, there is also double the battery voltage, and so total efficiency is the same.

One novel feature of this 4-cell circuit is the increase in the size of the bypass capacitors. Each half of the circuit retains its own output cap, to reduce noise seen by the circuit. Since the two halves interact with each other (when one opens its switch, the other one is also opened), there can be additional noise, which must be rejected for proper operation. The capacitors have been increased to 100 µF for this reason; remember that they must be rated to take the full maximum voltage rating of the charger, not half of it, since if one switch is closed and the other open, the charger (minus two cells' voltage drop, which might be zero) is applied across the other capacitor.

A second addition on this circuit is the (optional) two zeners, one each for each Si9730, placed from V_{DD} to V_M. These are necessary only if the charger voltage is higher than the 15-V absolute maximum of the IC plus two cells' voltage drop. Just as with the capacitor, if one switch is open and the other closed, the IC will see this charger voltage, and must be protected. The power rating of the zener can be inferred by observing that the current through it is limited by the 100-Ω resistor. A tradeoff can be made here between the power rating of the zener, which can be decreased by increasing the resistor value, and the accuracy of the voltage measurement by the Si9730, which can be increased by decreasing the resistor value.

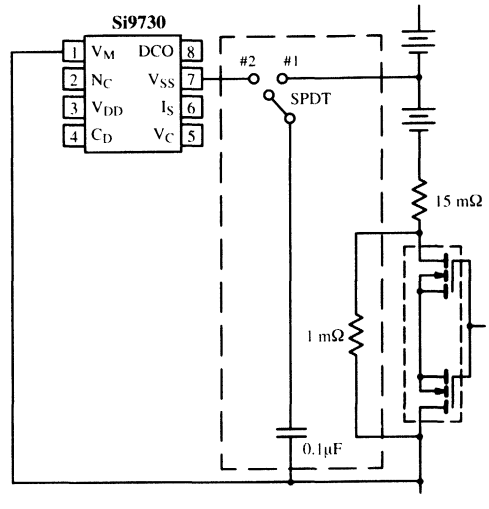


Figure 10. Factory Startup Circuit

Reset from Shutdown

There are two specialized conditions that can place the Si9730 in shutdown mode. The first condition can occur when the circuit is first attached to a battery in the factory. When the IC comes up, it will be in the undervoltage shutdown mode. The Si9730 may also enter this mode when the ambient temperature drops and the battery is nearly in UV. When the temperature drops, the battery pack voltage will drop and the IC may enter the shutdown mode. In either case, the Si9730 must be reset by raising the V_{SS} pin higher than the V_M pin by V_{CPHD}. Figure 10 shows a circuit that resets the circuit once it has entered the shutdown mode.

The circuit works by initially connecting the 0.1-µF capacitor to the battery's center tap and placing the switch in position #1. Although the MOSFETs are open, the 1-mΩ resistor is sufficient to allow the capacitor to charge up in about 300–400 msec. Once the capacitor is charged, the switch is placed in position #2, momentarily making V_{SS} higher than V_M, thus placing the Si9730 in the normal operating mode. The entire circuit provides a leakage of only a few microamps, which is much lower than the self discharge current of the LiIon battery.

Battery Disconnect Switch

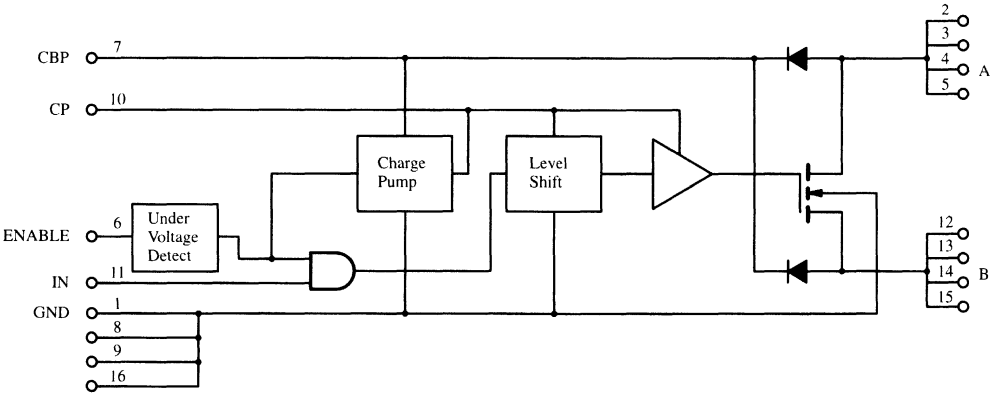
Features

- 6- to 18-V Operation
- Separate Logic Voltage Input
- Undervoltage Lockout (UVL) @ V_L = 3 V
- Shutdown Control Capability
- Safe Power Down

Description

The Si9717CY is a reverse blocking switch for battery disconnect applications. It is an integrated solution for multiple battery technology designs or designs that require isolation from the power bus during charging. The Si9717CY is available in a 16-pin SOIC package and is rated for the commercial temperature range of 0 to 70°C.

Functional Block Diagram



Absolute Maximum Ratings

Voltage Referenced to GND

V_A, V_B ..... –0.3 to 20 V

V_{IN} ..... –0.3 to 10 V

V_{ENABLE} ..... –0.3 to 10 V

Storage Temperature ..... –65 to 125°C

Power Dissipation ..... 2 W

Notes: Device mounted with all leads soldered to PC board.

Recommended Operating Range

V_A, V_B (see note) ..... 6 to 18 V

V_{IN} ..... 0 to 5 V

I_{AB} (continuous) ..... 0 to 4 A

I_{AB} x V_A (continuous) ..... 0 to 40 W

Minimum Cycle Time (turn-on to turn-on) ..... 10 ms

V_{ENABLE} ..... 0 to 5 V

Operating Temperature ..... 0 to 70°C

Junction Temperature ..... 0 to 150°C

Notes:

a. Si9717CY is functional at V_A, V_B = 5 to 6 V with higher supply current. See $I_{A(on)}$ specification.

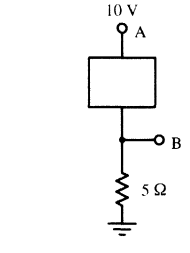
Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70023.

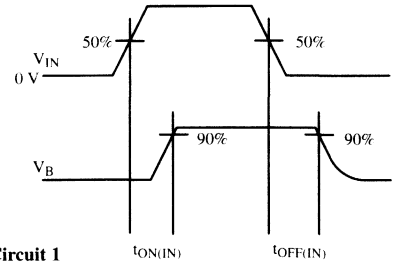
Specifications

Parameter	Symbol	Test Conditions Unless Otherwise Specified 6 V ≦ V_A ≦ 18 V C_{VDD} = 0.1 µF, CP = 0.02 µF	Temp[a]	Limits[d] Min[b]	Typ[c]	Max[b]	Unit
On-Resistance	R_{AB}	V_A = 10 V, I_A = 1 A	Room			0.06	Ω
Leakage Current	$I_{AB(off)}$	V_A = 16 V, V_B = 0 V	Room			10	µA
IN Low Threshold	$V_{IN(L)}$		Full			1	V
IN High Threshold	$V_{IN(H)}$		Full	4.0			
IN Input Current	$I_{IN(H)}$	V_{IN} = 5.0 V	Full			1	µA
Turn-On Delay IN to A or B	$t_{ON(IN)}$	ENABLE = 5 V, V_A = 10 V, R_L = 5 Ω Test Circuit 1	Full			10	µs
Turn-Off Delay IN to A or B	$t_{OFF(IN)}$		Full			10	
ENABLE Low Threshold	$V_{ENABLE(L)}$		Full			3.0	V
ENABLE High Threshold	$V_{ENABLE(H)}$		Full	4.4			
ENABLE Input Current	$I_{ENABLE(H)}$	V_{ENABLE} = 5 V	Full			50	µA
Setup Time from ENABLE to Switch	$t_{ENABLE(H)}$	V_A = 10 V, V_{IN} = 0 V, Test Circuit 2	Room			2.0	ms
		V_A = 6 V, V_{IN} = 0 V, Test Circuit 2	Full			10	
On-State Drain	$I_{A(on)}$	AB Shorted, V_A = 10 V, V_{ENABLE} = 5 V	Full			60	µA
		AB Shorted, V_A = 5 V, V_{ENABLE} = 5 V	Full			300	
Off-State Drain	$I_{A(off)}$	AB Shorted, V_A = 10 V, V_{ENABLE} = 0 V	Full			10	

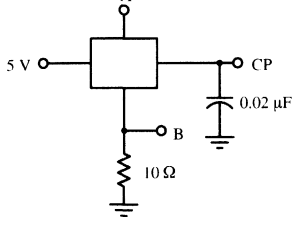
Notes:
a. Room = 25°C, Full = as determined by the operating temperature suffix.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. Tested at room temperature, high temperature guaranteed by statistical data correlation techniques.

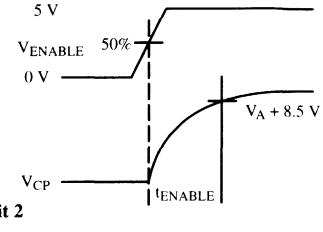
Test Circuits





Test Circuit 1



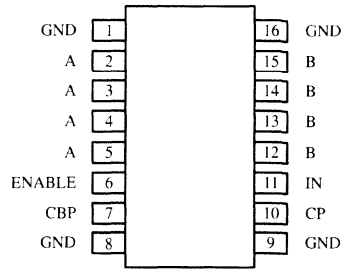


Test Circuit 2

Pin Configuration and Truth Table

ENABLE	IN	Switch Controller State	Switch
0	0	Inactive	X
0	1	Inactive	X
1	0	Set-Up	Off
1	1	Active	On

SO-16



Top View

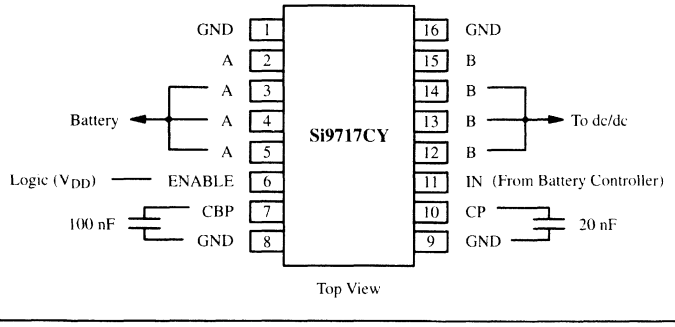
Order Number: Si9717CY

Pin Description

Pin Number	Symbol	Description
1, 8, 9, 16	GND	Common connection for negative battery terminals.
2, 3, 4, 5	A	A-terminal of the battery switch, bidirectional.
6	ENABLE	Logic input, ENABLE. Activates charge pump and switch drive logic.
7	CBP	Internally generated logic power supply, V_{DD}. Requires external bypass capacitor connected to pin 8.
10	CP	Charge pump output terminal. Requires external capacitor connected to pin 9.
11	IN	Logic input, IN. A high level turns on the switch.
12, 13, 14, 15	B	B-terminal of the battery switch, bidirectional.

Applications Diagram

SO-16



Top View

Battery Disconnect Switch

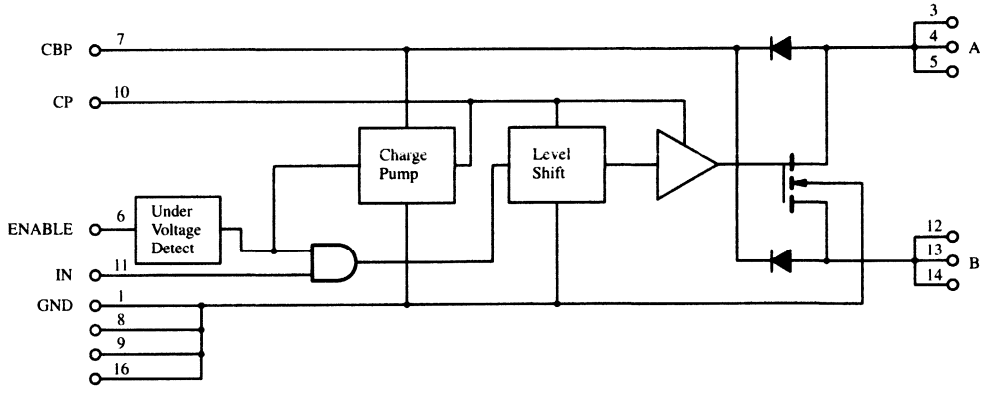
Features

- 6- to 18-V Operation
- Separate Logic Voltage Input
- Undervoltage Lockout (UVL) @ V_L = 3 V
- Shutdown Control Capability
- Safe Power Down

Description

The Si9718CY is a reverse blocking switch for battery disconnect applications. It is an integrated solution for multiple battery technology designs or designs that require isolation from the power bus during charging. The Si9718CY is available in a 16-pin SOIC package and is rated for the commercial temperature range of 0 to 70°C.

Functional Block Diagram



Absolute Maximum Ratings

Voltage Referenced to GND

V_A, V_B ..... –0.3 to 20 V
V_{IN} ..... –0.3 to 10 V
V_{ENABLE} ..... –0.3 to 10 V

Storage Temperature ..... –65 to 125°C
Power Dissipation ..... 2 W

Notes: Device mounted with all leads soldered to PC board.

Recommended Operating Range

V_A, V_B (See note a) ..... 6 to 18 V
V_{IN} ..... 0 to 5 V
I_{AB} (continuous) ..... 0 to 3.5 A
I_{AB} x V_A (continuous) ..... 0 to 35 W
Minimum Cycle Time (turn-on to turn-on) ..... 10 ms
V_{ENABLE} ..... 0 to 5 V

Operating Temperature ..... 0 to 70°C
Junction Temperature ..... 0 to 150°C

Notes:
a. Si9718CY is functional at V_A, V_B = 5 to 6 V with higher supply current. See $I_{A(on)}$ specification.

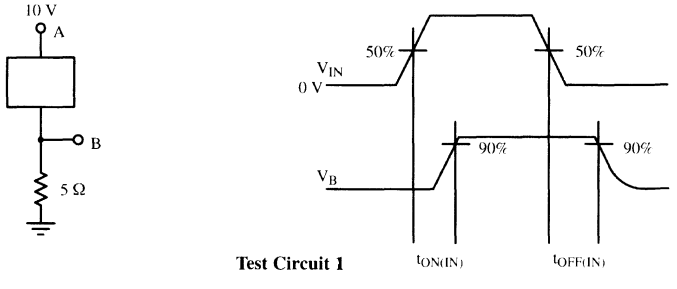
Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70019.

Specifications

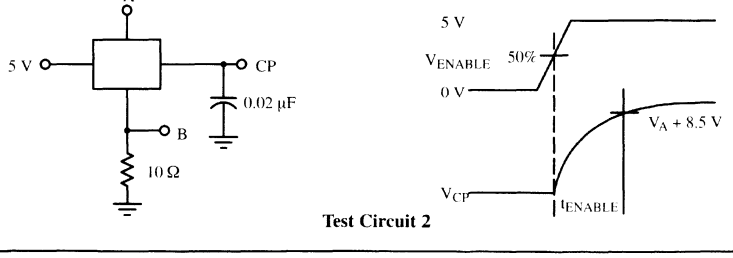
Parameter	Symbol	Test Conditions Unless Otherwise Specified 6 V ≦ V_A ≦ 18 V C_{VDD} = 0.1 µF, CP = 0.02 µF	Temp[a]	Limits[d] Min[b]	Typ[c]	Max[b]	Unit
On-Resistance	R_{AB}	V_A = 10 V, I_A = 1 A	Room			0.08	Ω
Leakage Current	$I_{AB(off)}$	V_A = 16 V, V_B = 0 V	Room			10	µA
IN Low Threshold	$V_{IN(L)}$		Full			1	V
IN High Threshold	$V_{IN(H)}$		Full	4.0			
IN Input Current	$I_{IN(H)}$	V_{IN} = 5.0 V	Full			1	µA
Turn-On Delay IN to A or B	$t_{ON(IN)}$	ENABLE = 5 V, V_A = 10 V, R_L = 5 Ω Test Circuit 1	Full			10	µs
Turn-Off Delay IN to A or B	$t_{OFF(IN)}$		Full			10	
ENABLE Low Threshold	$V_{ENABLE(L)}$		Full			3.0	V
ENABLE High Threshold	$V_{ENABLE(H)}$		Full	4.4			
ENABLE Input Current	$I_{ENABLE(H)}$	V_{ENABLE} = 5 V	Full			50	µA
Setup Time from ENABLE to Switch	$t_{ENABLE(H)}$	V_A = 10 V, V_{IN} = 0 V, Test Circuit 2	Room			2.0	ms
		V_A = 6 V, V_{IN} = 0 V, Test Circuit 2	Full			10	
On-State Drain	$I_{A(on)}$	AB Shorted, V_A = 10 V, V_{ENABLE} = 5 V	Full			60	µA
		AB Shorted, V_A = 5 V, V_{ENABLE} = 5 V	Full			300	
Off-State Drain	$I_{A(off)}$	AB Shorted, V_A = 10 V, V_{ENABLE} = 0 V	Full			10	

Notes:
a. Room = 25°C, Full = as determined by the operating temperature suffix.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. Tested at room temperature, high temperature guaranteed by statistical data correlation techniques.

Test Circuit



Test Circuit 1

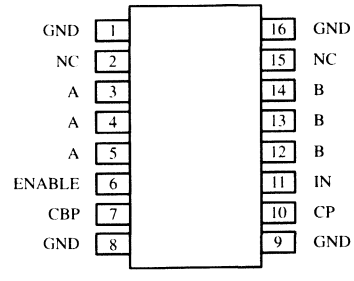


Test Circuit 2

Pin Configuration and Truth Table

ENABLE	IN	Switch Controller State	Switch
0	0	Inactive	X
0	1	Inactive	X
1	0	Set-Up	Off
1	1	Active	On

SO-16



Top View

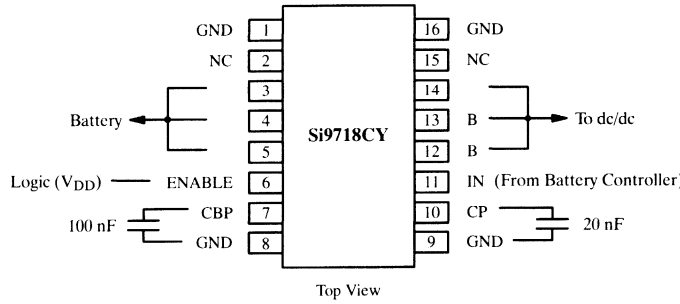
Order Number: Si9718CY

Pin Description

Pin Number	Symbol	Description
1, 8, 9, 16	GND	Common connection for negative battery terminals.
2, 15	NC	No internal connection.
3, 4, 5	A	A-terminal of the battery switch, bidirectional.
6	ENABLE	Logic input, ENABLE. Activates charge pump and switch drive logic.
7	CBP	Internally generated logic power supply, V_{DD}. Requires external bypass capacitor connected to pin 8.
10	CP	Charge pump output terminal. Requires external capacitor connected to pin 9.
11	IN	Logic input, IN. A high level turns on the switch.
12, 13, 14	B	B-terminal of the battery switch, bidirectional.

Applications Diagram

SO-16



Top View

PC Card (PCMCIA) Interface Switch

Features

- Single SO-8 Package
- CMOS-Logic Compatible Inputs
- Slow V_{CC} Ramp Time
- Smart Switching
- Extremely Low R_{ON}
- Reverse Blocking Switches
- Low Power Consumption
- Safe Power Up

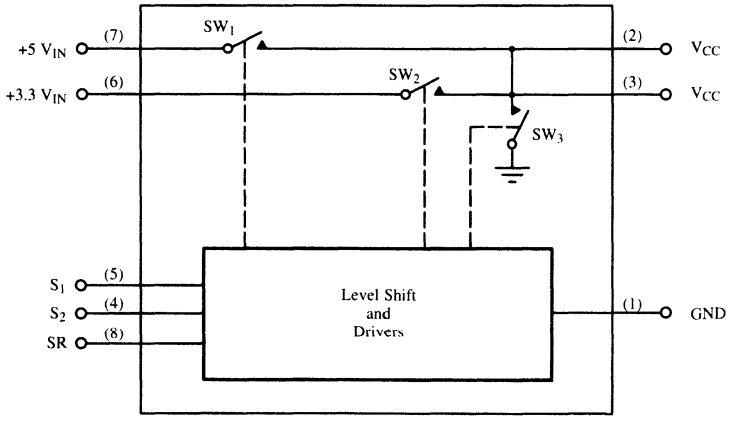
Description

The Si9706DY offers an integrated solution for PC Card power interfaces that only require V_{CC} switching. This part is ideal for systems that operate at 5 V and provide V_{PP} from the main supply or from a dedicated Flash RAM 12-V supply.

The Si9706DY operates off the 5-V supply and has built-in level shifting for gate drive. Internal logic protects against a control logic error that would short 5 V to the 3.3-V supply. This protection logic also allows the Si9706DY to be configured for positive or negative control logic for compatibility with a variety of PC Card controllers. These control inputs are CMOS logic compatible and can be driven to 3.3 V or 5 V.

The Si9706DY PC Card interface switch is packaged in a narrow body SO-8 package and is rated over the industrial temperature range –40 to 85°C.

Functional Block Diagram



Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70010.

Absolute Maximum Ratings

Voltages Referenced to Ground
+5 V_{IN} ..... 7 V
+3.3 V_{IN} ..... 7 V
S_1, S_2 (CMOS Inputs) ..... 7 V
All Pins ..... –0.5 V
I_{OUT} V_{CC}[a] ..... 4 A
PD Max[b]: (T_A = 25°C) ..... 1.59 W
(T_A = 85°C) ..... 0.63 W

Junction Temperature ..... 125°C
Thermal Ratings[b]: $R_{\Theta JA}$ ..... 63 °C/W

Notes
a. Pins 2, 3 connected together externally.
b. Mounted on 1-IN^2, FR4 PC Board.

Recommended Operating Conditions

+5 V_{IN} (must be present) ..... 5 V ± 10%
+3.3 V_{IN} ..... 3.3 V ± 10%
C_{SR} ..... 33 nF
I_{OUT} V_{CC}[a] ..... 2 A

V_{CC} Load Capacitance ..... 150 µF Max

Notes
a. Pins 2, 3 connected together externally.

Specifications

Parameter	Symbol	Test Conditions Unless Otherwise Specified C_{SR} = 33 nF, +5 V_{IN} = 5 V +3.3 V_{IN} = 3.3 V, Low ≤ 0.8 V, High ≥ 2.2 V		Limits –40 to 85°C Min[a]	Typ[b]	Max[a]	Unit
Switch SW_1							
On-Resistance	R_{ON}	I = 500 mA, S_1 = High S_2 = Low	T_A = 25°C		58	70	mΩ
			T_A = 85°C		73	90	
Off Current (V_{CC})	I_{OFF}	+5 V_{IN} = 5.5 V, V_{CC} = 0 V S_1 = S_2 = Low	T_A = 25°C			1	µA
			T_A = 85°C			10	
Rise Time	$t_{S1(on)}$	S_2 = Low, See Figure 1		0.2	1.7	5	ms
Fall Time	$t_{S1(off)}$			10	30	50	
Switch SW_2							
On-Resistance	R_{ON}	I = 500 mA, S_2 = High S_1 = Low	T_A = 25°C		44	55	mΩ
			T_A = 85°C		55	70	
Off Current (+3.3 V_{IN})	I_{OFF}	+3.3 V_{IN} = 3.6 V, V_{CC} = 0 V S_1 = S_2 = Low	T_A = 25°C			1	µA
			T_A = 85°C			10	
Rise Time	$t_{S2(on)}$	S_1 = Low, See Figure 1		0.1	0.9	5	ms
Fall Time	$t_{S2(off)}$			5	20	40	
Switch SW_3							
On-Resistance	R_{ON}	I = 2 mA, S_1 = S_2 = Low	T_A = 25°C		140	400	Ω
			T_A = 85°C		200	500	
Power Supply							
+5 V_{IN} Current Input (on)	$I_{+5VIN(1)}$	S_1 = 0 V, S_2 = 3 V			20	50	µA
	$I_{+5VIN(2)}$	S_1 = 3 V, S_2 = 0V			20	50	
+5 V_{IN} Current Input (off)	$I_{+5VIN(3)}$	S_1 = S_2 = 0 V			< 1	10	

Specifications

Parameter	Symbol	Test Conditions Unless Otherwise Specified C_{SR} = 33 nF, +5 V_{IN} = 5 V +3.3 V_{IN} = 3.3 V, Low ≤ 0.8 V, High ≥ 2.2 V	Limits –40 to 85°C Min[a]	Typ[b]	Max[a]	Unit
Switch Control Inputs S_1, S_2						
Input Voltage High	$V_{I(H)}$	+5 V_{IN} = 5.5 V	2.2	1.8		V
		+5 V_{IN} = 4.5 V	2.2	1.6		
Input Voltage Low	$V_{I(L)}$	+5 V_{IN} = 5.5 V		1.6	0.8	
		+5 V_{IN} = 4.5 V		1.4	0.8	
Input Current High	$I_{I(H)}$	S_1, S_2 = 5 V			1.0	µA
Input Current Low	$I_{I(L)}$	S_1, S_2 = GND	–1.0			

Notes
a. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum.
b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

Timing Waveforms

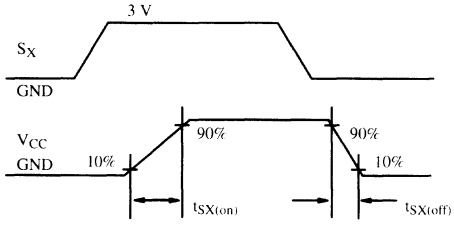


Figure 1. Switch Ramp

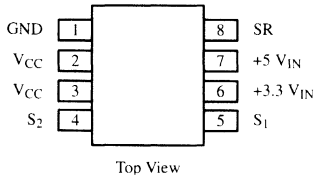
Truth Table

S_1	S_2	Switch 1	Switch 2	Switch 3
0	0	Off	Off	On
0	1	Off	On	Off
1	0	On	Off	Off
1	1	Off	Off	On

Notes
a. Switch 1 and 2 are delayed until after V_{CC} is valid.
b. Shaded line is an error condition for PC Card applications.
c. The smart switching of the Si9706DY avoids potential host damage by defaulting to off during error conditions.

Pin Configuration and Description

SO-8

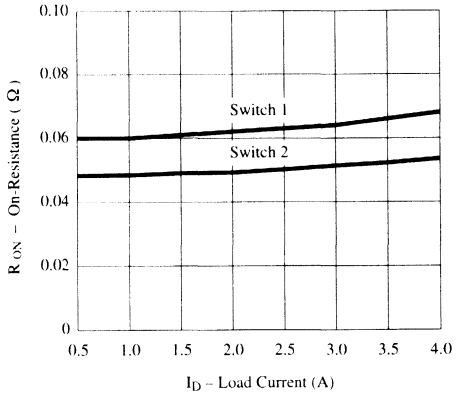


Top View

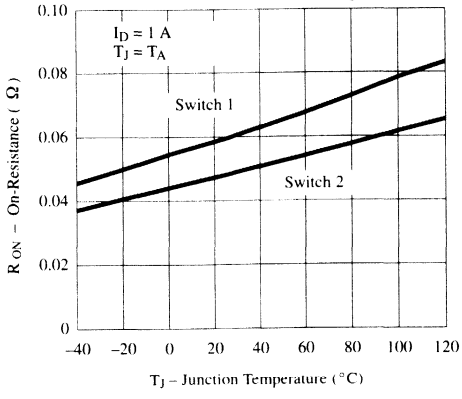
Function	Pin Number	Description
S_1	5	Control input for selecting +5 V_{IN} to V_{CC}.
S_2	4	Control input for selecting +3.3 V_{IN} to V_{CC}.
GND	1	Ground connection.
V_{CC}	2, 3	Supply voltage to slot.
+3.3 V_{IN}	6	+3.3-V supply.
+5 V_{IN}	7	+5-V supply.
SR	8	Slew rate control pin.

Typical Characteristics (25°C Unless Otherwise Noted)

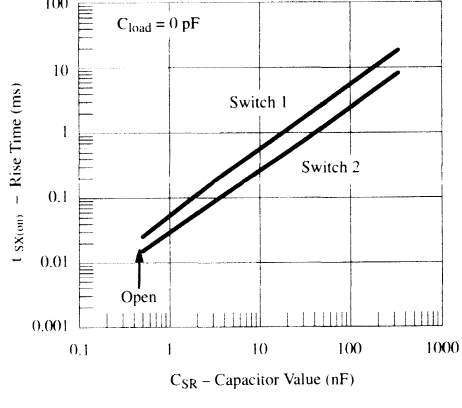
On-Resistance vs. Load Current



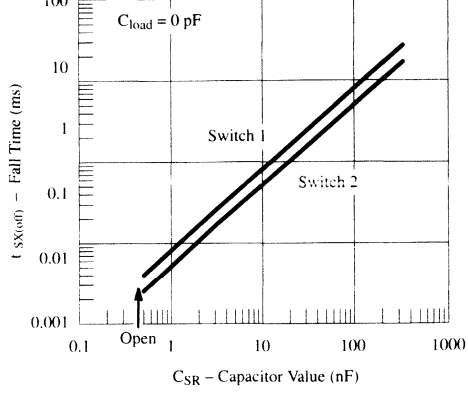
On-Resistance vs. Junction Temperature



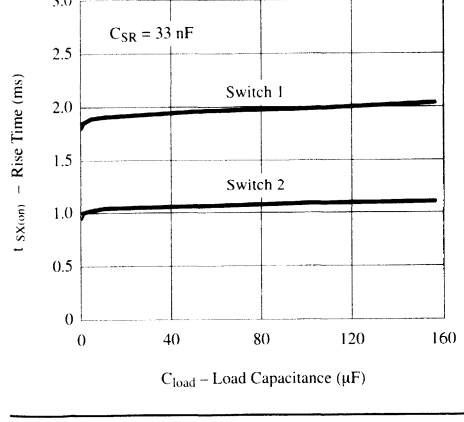
Rise Time vs. SR Capacitor Value



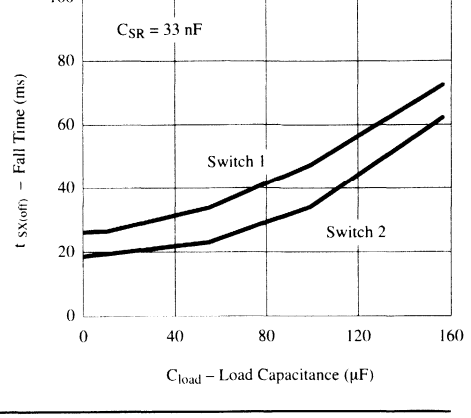
Fall Time vs. SR Capacitor Value



Rise Time vs. Load Capacitance



Fall Time vs. Load Capacitance



PC Card (PCMCIA) Dual Interface Switch

Features

- Single SO-16 Package
- CMOS Logic Compatible Inputs
- Smart Switching
- Slow V_{CC} Ramp Times
- Extremely Low R_{ON}
- Supports Dual PC Card Slots
- Reverse Blocking Switches
- Low Power Consumption
- Safe Power-Up

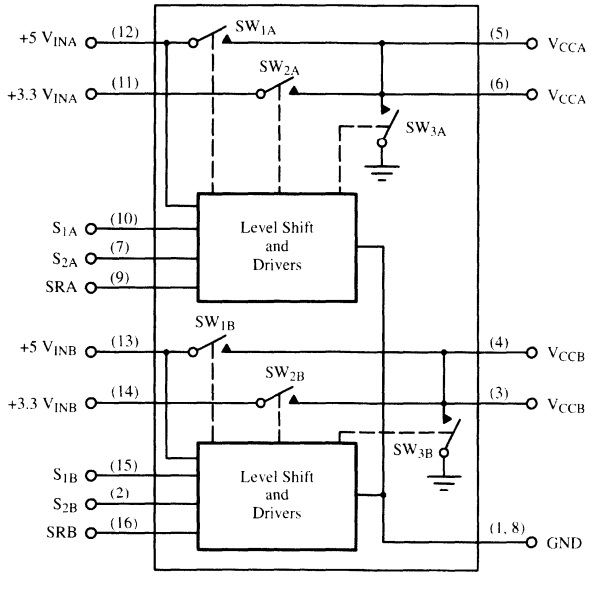
Description

The Si9707DY offers an integrated solution for dual PC Card power interfaces that require only V_{CC} switching. This part is ideal for systems that operate at 5 V and provide V_{PP} from the main supply, or from a dedicated Flash RAM 12-V supply.

The Si9707DY operates off the 5-V supply with built-in level shifting. The V_{CC} outputs function independently and internal logic protects each slot against a control logic error that would short 5 V to the 3.3-V supply. This protection logic also allows the Si9707DY to be configured for positive or negative control logic for compatibility with a variety of PC Card controllers. These control inputs are CMOS logic compatible and can be driven to 3.3 V or 5 V.

The PC Card Dual Interface Switch is available in a SO-16 narrow-body package and is rated over the industrial temperature range of –40 to 85°C.

Functional Block Diagram



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Absolute Maximum Ratings

Voltages Referenced to Ground

+5 V_{INA}, +5 V_{INB} ..... 7 V
+3.3 V_{INA}, +3.3 V_{INB} ..... 7 V
S_{1A} and S_{2A}, S_{1B}, S_{2B} (CMOS Inputs) ..... 7 V
All Pins ..... –0.5 V
I_{OUT} V_{CCA}[a], I_{OUT} V_{CCB}[b] ..... 4 A

PD Max[c]: (T_A = 25°C) ..... 1.65 W
(T_A = 85°C) ..... 0.65 W
Junction Temperature ..... 125°C
Thermal Ratings: $R_{\Theta JA}$[c] ..... 60 °C/W

Notes
a. Pins 5, 6 connected together externally.
b. Pins 3, 4 connected together externally.
c. Mounted on 1-IN^2, FR4 PC Board.

Recommended Operating Conditions

+5 V_{INA}, +5 V_{INB} (must be present) ..... 5 V ± 10%
+3.3 V_{INA}, +3.3 V_{INB} ..... 3.3 V ± 10%
C_{SRA}, C_{SRB} ..... 33 nF
I_{OUT} V_{CCA}[a], I_{OUT} V_{CCB}[b] ..... 2 A

V_{CC} Load Capacitance ..... 150 µF Max

Notes
a. Pins 5, 6 connected together externally.
b. Pins 3, 4 connected together externally.

Specifications

Parameter	Symbol	Test Conditions Unless Otherwise Specified C_{SR} = 33 nF, +5 V_{IN} = 5 V +3.3 V_{IN} = 3.3 V, Low ≤ 0.8 V, High ≥ 2.2 V		Limits –40 to 85°C Min[a]	Typ	Max[a]	Unit
Switch SW_{1A}, SW_{1B}							
On-Resistance	R_{ON}	I = 500 mA, S_1 = High S_2 = Low	T_A = 25°C		58	70	mΩ
			T_A = 85°C		73	90	
Off Current (V_{CC})	I_{OFF}	+5 V_{IN} = 5.5 V, V_{CC} = 0 V S_1 = S_2 = Low	T_A = 25°C			1	µA
			T_A = 85°C			10	
Rise Time	$t_{S1(on)}$	S_2 = Low. See Figure 1		0.2	1.7	5	ms
Fall Time	$t_{S1(off)}$			10	30	50	
Switch SW_{2A}, SW_{2B}							
On-Resistance	R_{ON}	I = 500 mA, S_2 = High S_1 = Low	T_A = 25°C		44	55	mΩ
			T_A = 85°C		55	70	
Off Current (+3.3 V_{IN})	I_{OFF}	+3.3 V_{IN} = 3.6 V, V_{CC} = 0 V S_1 = S_2 = Low	T_A = 25°C			1	µA
			T_A = 85°C			10	
Rise Time	$t_{S2(on)}$	S_1 = Low, See Figure 1		0.1	0.9	5	ms
Fall Time	$t_{S2(off)}$			5	20	40	
Switch SW_{3A}, SW_{3B}							
On-Resistance	R_{ON}	I = 2 mA, S_1 = S_2 = Low	T_A = 25°C		140	400	Ω
			T_A = 85°C		200	500	
Power Supply							
+5 V_{IN} Current Input (on)	$I_{+5VIN(1)}$	S_1 = 0 V, S_2 = 3 V			20	50	µA
	$I_{+5VIN(2)}$	S_1 = 3 V, S_2 = 0V			20	50	
+5 V_{IN} Current Input (off)	$I_{+5VIN(3)}$	S_1 = S_2 = 0 V			<1	10	
Switch Control Inputs S_{1X}, S_{2X}							
Input Voltage High	$V_{I(H)}$	+5 V_{INX} = 5.5 V		2.2	1.8		V
		+5 V_{INX} = 4.5 V		2.2	1.6		
Input Voltage Low	$V_{I(L)}$	+5 V_{INX} = 5.5 V			1.6	0.8	
		+5 V_{INX} = 4.5 V			1.4	0.8	
Input Current High	$I_{I(H)}$	S_{1X}, S_{2X} = 5 V				1.0	µA
Input Current Low	$I_{I(L)}$	S_{1X}, S_{2X} = GND		–1.0			

Notes
a. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum.

Timing Waveforms

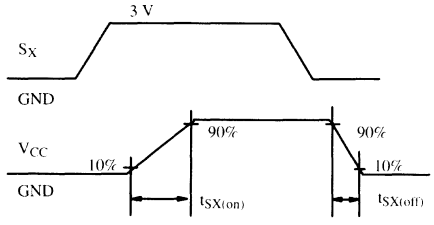
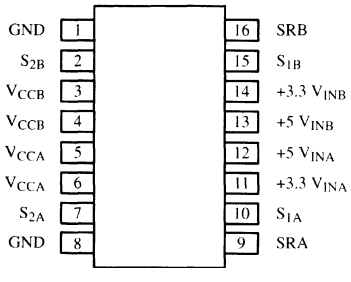


Figure 1. Switch Ramp Time

Pin Configuration and Description

SO-16



Top View

Function	Pin Number	Description
S_{1A}	10	Control input for selecting +5 V_{INA} to V_{CCA}.
S_{1B}	15	Control input for selecting +5 V_{INB} to V_{CCB}.
S_{2A}	7	Control input for selecting +3.3 V_{INA} to V_{CCA}.
S_{2B}	2	Control input for selecting +3.3 V_{INB} to V_{CCB}.
GND	1, 8	Ground connection.
V_{CCA}	5, 6	Supply voltage to slot.
V_{CCB}	3, 4	Supply voltage to slot.
+3.3 V_{INA}	11	+3.3-V supply.
+3.3 V_{INB}	14	+3.3-V supply.
+5 V_{INA}	12	+5-V supply.
+5 V_{INB}	13	+5-V supply.
SRA	9	Slew rate control pin.
SRB	16	Slew rate control pin.

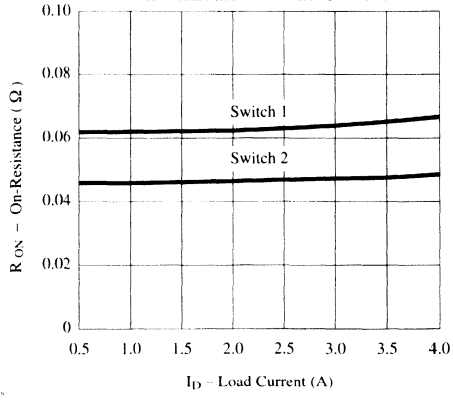
Truth Table

S_1X	S_2X	Switch 1X	Switch 2X	Switch 3X
0	0	Off	Off	On
0	1	Off	On	Off
1	0	On	Off	Off
1	1	Off	Off	On

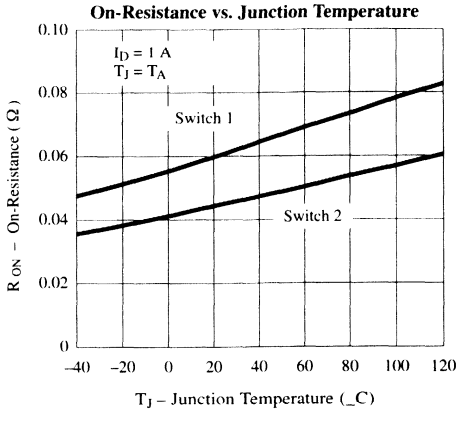
Notes
a. Switch 1 and 2 are delayed until after V_{CC} is valid.
b. Shaded lines are error conditions for PC Card applications.
c. The smart switching of the Si9707 avoids potential host damage by defaulting to off during error conditions.

Typical Characteristics (25°C Unless Otherwise Noted)

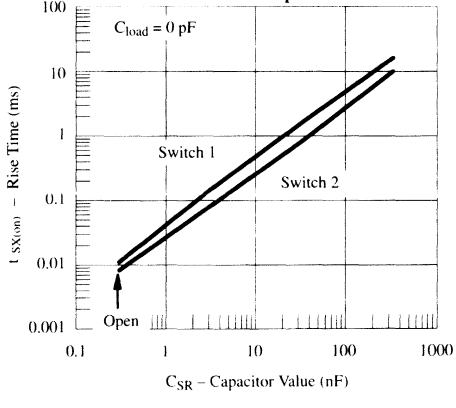
On-Resistance vs. Load Current



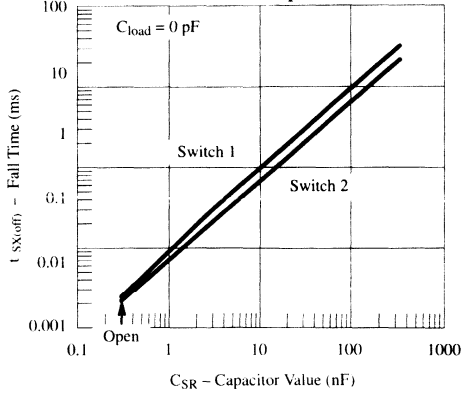
On-Resistance vs. Junction Temperature



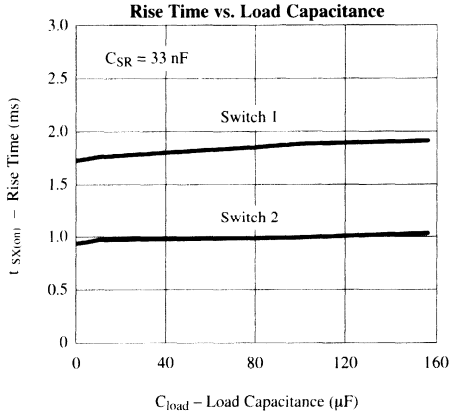
Rise Time vs. SR Capacitor Value



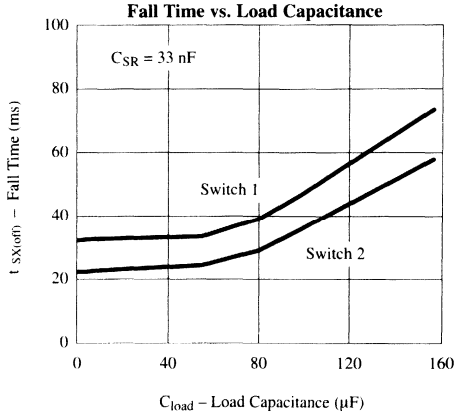
Fall Time vs. SR Capacitor Value



Rise Time vs. Load Capacitance



Fall Time vs. Load Capacitance



PC Card (PCMCIA) Interface Switch

Features

- Single SO-16 Package
- CMOS Inputs with Hysteresis
- Extremely Low R_{ON}
- Reverse Blocking Switches
- HiZ Outputs in the Off-State
- Low Power Consumption
- Safe Power-Up

Description

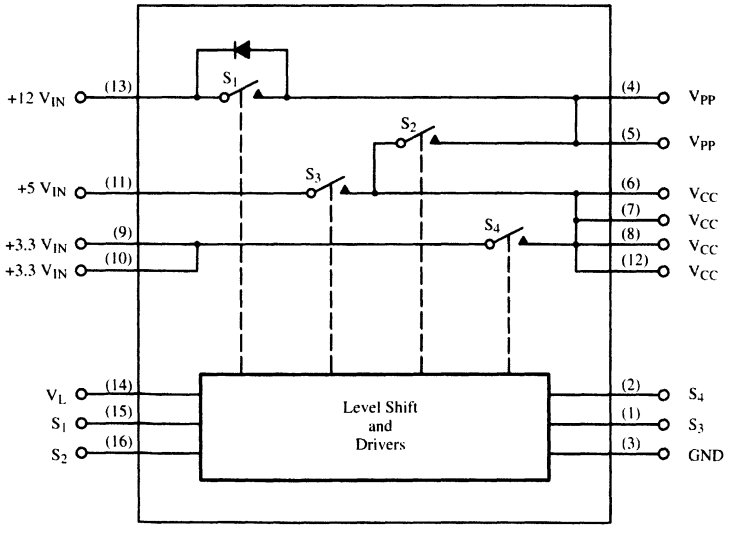
The Si9711CY is a monolithic switch designed to meet the needs of the PC Card interface. The inputs are fully CMOS compatible and incorporate all the level shift and interface required to be driven by any CMOS driver. The external inputs can be driven to 3.3-V or 5-V by setting V_L at the appropriate level. The switches are low R_{ON} and can carry the maximum currents found on the PC Card interface.

The 5-V and 3.3-V switches do not have the parasitic diode found in vertical DMOS power switches.

Low R_{ON} is achieved by using MOSFETs driven off the +12-V_{IN} input. All level shifting is built into the Si9711CY.

The Si9711CY is packaged in an SO-16 package and is rated over the commercial temperature range 0 to 70°C.

Functional Block Diagram



Truth Table – S_1 through S_4

Logic	Switch
0	OFF
1	ON

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70022.

Absolute Maximum Ratings

Voltages Referenced to Ground

V_L ..... 7 V
+12 V_{IN} ..... 15 V
+5 V_{IN} ..... 7 V
+3.3 V_{IN} ..... 7 V
S_1 through S_4 (CMOS Inputs) ..... V_L + 0.5 V
I_{OUT} V_{PP} ..... 300 mA
V_{CC} ..... 7 V
V_{PP} ..... 15 V
All Pins ..... –0.5 V
I_{OUT} V_{CC} ..... 1.5 A
PD Max: (T_A = 25°C) ..... 710 mW
(T_A = 70°C) ..... 390 mW
Junction Temperature ..... 125°C
Thermal Ratings
$R_{\Theta JA}$ ..... 140 °C/W

Recommended Operating Conditions

+12 V_{IN} ..... 12 V ± 10%
+5 V_{IN} ..... 5 V ± 10%
+3.3 V_{IN} ..... 3.3 V ± 10%
I_{OUT} V_{CC} ..... 1 A
I_{OUT} V_{PP} ..... 150 mA
V_L ..... 5.0 V ± 10%

Specifications

Parameter	Symbol	Test Conditions Unless Otherwise Specified +5 V_{IN} = 5 V, +3.3 V_{IN} = 3.3 V +12 V_{IN} = 12 V, V_L = 5.0 V, GND = 0 V		Limits C Suffix, 0 to 70°C Min[a]	Typ	Max[a]	Unit
Switch 1							
On-Resistance	R_{ON}	I = 120 mA, +12 V_{IN} = 10.8 V S_1 = V_L, S_2 = GND	T_A = 25°C			200	mΩ
			T_A = 70°C			250	
Off Current (+12 V_{IN} to V_{PP})	I_{OFF}	+12 V_{IN} = 13.2 V, V_{PP} = 0 V S_1 = GND	T_A = 25°C			1	µA
			T_A = 70°C			10	
Switching Time	$t_{S1(on)}$	C_L = 0.1 µF, S_2 = Low, R_L = 100 Ω, See Figure 1		0.1		1	µs
	$t_{S1(off)}$			0.5		4	
Switch 2							
On-Resistance	R_{ON}	I = 120 mA, +12 V_{IN} = 10.8 V S_2 = S_3 = V_L	T_A = 25°C			300	mΩ
			T_A = 70°C			350	
Off Current	I_{OFF}	V_{PP} = 13.2 V, V_{CC} = 0 V +12 V_{IN} = 13.2 V	T_A = 25°C			1	µA
			T_A = 70°C			10	
Switching Time	$t_{S2(on)}$	C_L = 0.1 µF, R_L = 100 Ω, S_1 = S_4 = GND, S_3 = V_L, See Figure 1		0.1		1	µs
	$t_{S2(off)}$			0.5		4	
Switch 3							
On-Resistance	R_{ON}	I = 500 mA, +12 V_{IN} = 10.8 V S3 = V_L	T_A = 25°C			200	mΩ
			T_A = 70°C			250	
Off Current	I_{OFF}	+5 V_{IN} = 5.5 V, V_{CC} = 0 V	T_A = 25°C			1	µA
			T_A = 70°C			10	
Switching Time	$t_{d(on)}$	+5 V_{IN} = 5 V, C_L = 0.1 µF, V_{CC} to GND R_L = 100 Ω, V_{CC} to GND, See Figure 2		1			µs
	$t_{ramp(on)}$			200			
	$t_{S3(off)}$			0.5		4	

Specifications

Parameter	Symbol	Test Conditions Unless Otherwise Specified +5 V_{IN} = 5 V, +3.3 V_{IN} = 3.3 V +12 V_{IN} = 12 V, V_L = 5.0 V, GND = 0 V		Limits C Suffix, 0 to 70°C Min[a]	Typ	Max[a]	Unit
Switch 4							
On-Resistance	R_{ON}	I = 500 mA, +12 V_{IN} = 10.8 V S_4 = V_L	T_A = 25°C			150	mΩ
			T_A = 70°C			185	
Off Current	I_{OFF}	+3.3 V_{IN} = 3.6 V, V_{CC} = 0 V S_2 = S_3 = S_4 = GND	T_A = 25°C			1	µA
			T_A = 70°C			10	
Switching Time	$t_{d(on)}$	+3.3 V_{IN} = 3.3 V, C_L = 0.1 µF, S_3 = GND R_L = 100 Ω, See Figure 2		1			µs
	$t_{ramp(on)}$			200			
	$t_{S4(off)}$			0.5		4	
Power Supply							
+12 V_{IN} Current	$I_{+12VIN(1)}$	S_1 = S_4 = GND, S_2 = S_3 = V_L				10	µA
	$I_{+12VIN(2)}$	S_1 = S_4 = V_L, S_2 = S_3 = GND				10	
V_L Current	$I_{VL(1)}$	S_1 = S_4 = GND, S_2 = S_3 = V_L				10	
	$I_{VL(2)}$	S_1 = S_4 = V_L, S_2 = S_3 = GND				10	
Switch Control Inputs							
Input Voltage High	$V_{I(H)}$		V_L = 3.3 V	2.8	2.4		V
			V_L = 5 V	4.0	3.3		
Input Voltage Low	$V_{I(L)}$		V_L = 3.3 V		1.1	0.4	
			V_L = 5 V		1.5	0.8	
Input Hysteresis[b]	$V_{I(H)}-V_{I(L)}$		V_L = 3.3 V	0.5	1.3		
			V_L = 5 V	0.8	1.8		
Input Current High	$I_{I(H)}$	S_1 through S_4 = V_L, V_L = 5 V				1.0	µA
Input Current Low	$I_{I(L)}$	S_1 through S_4 = GND, V_L = 5 V		−1.0			

Notes
a. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
b. Guaranteed by design, not subject to production testing.

Timing Waveforms

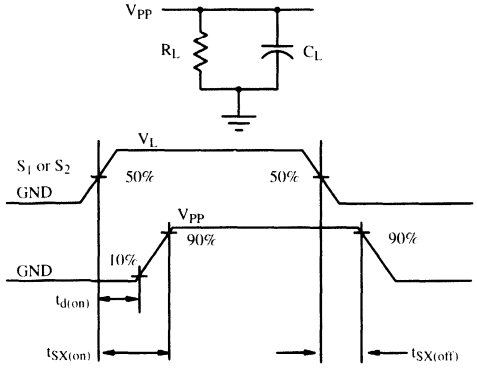


Figure 1. $t_{d(on)}$ and $t_{SX(on)}$

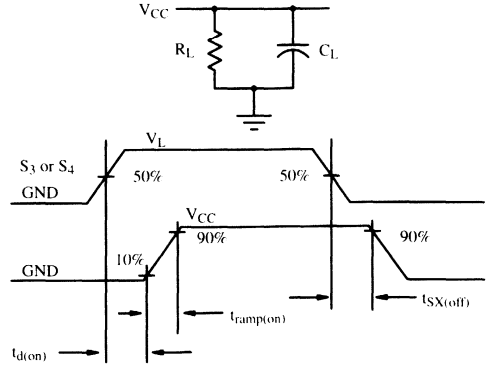
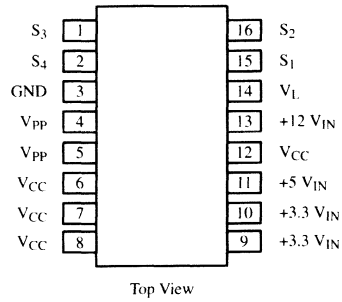


Figure 2. $t_{ramp(on)}$

Pin Configuration

SO-16



Top View

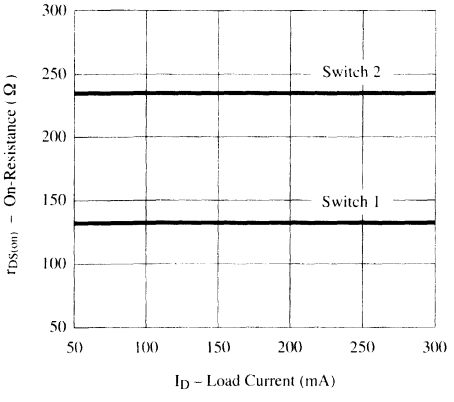
Order Number: Si9711CY

Pin Description

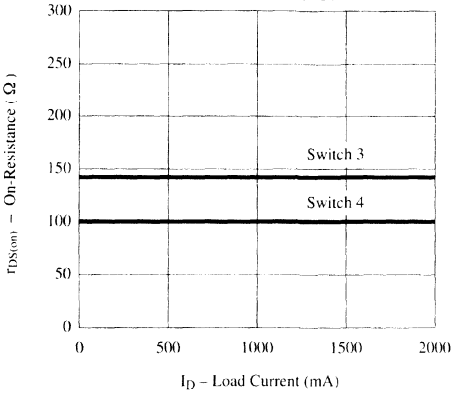
Pin Number	Symbol	Description
1	S_3	Control input for selecting +5 V_{IN} to V_{CC}. The PC Card terminology for this pin is $V_{CC}\_EN_1$.
2	S_4	Control input for selecting +3.3 V_{IN} to V_{CC}. The PC Card terminology for this pin is $V_{CC}\_EN_0$.
3	GND	Ground connection.
4, 5	V_{PP}	Program and peripheral voltage to PC Card slot.
6, 7, 8, 12	V_{CC}	Supply voltage to slot.
9, 10	+3.3 V_{IN}	+3.3-V supply.
11	+5 V_{IN}	+5-V supply.
13	+12 V_{IN}	+12-V supply.
14	V_L	Rail voltage for switch control inputs, selectable to 5-V or 3.3-V.
15	S_1	Control input for selecting +12 V_{IN} to V_{PP}. The PC Card terminology for this pin is $V_{PP}\_EN_1$.
16	S_2	Control input for selecting V_{CC} to V_{PP}. The PC Card terminology for this pin is $V_{PP}\_EN_0$.

Typical Characteristics (25°C Unless Otherwise Noted)

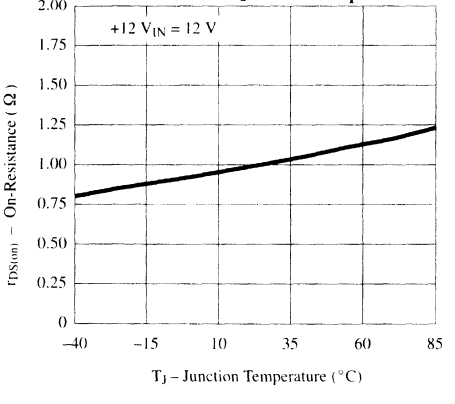
On-Resistance vs. Load Current



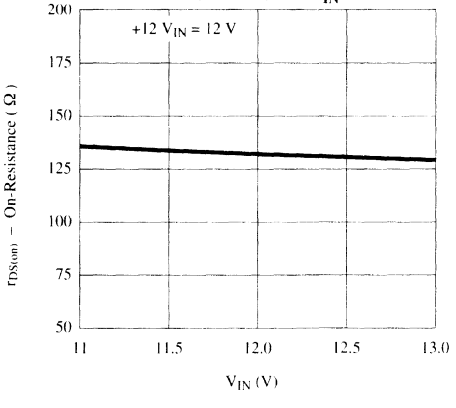
On-Resistance vs. Load Current



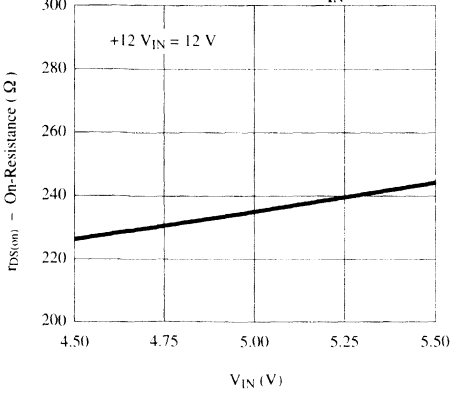
Switch 1 – 4
On-Resistance vs. Junction Temperature



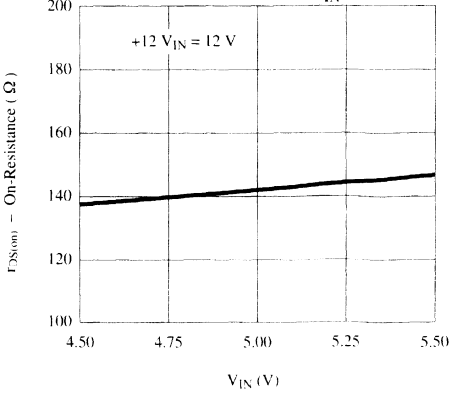
Switch 1
On-Resistance vs. V_{IN}



Switch 2
On-Resistance vs. V_{IN}

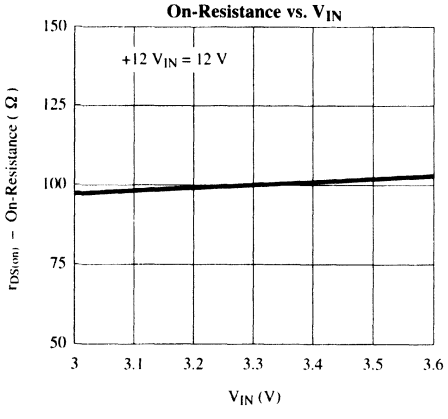


Switch 3
On-Resistance vs. V_{IN}

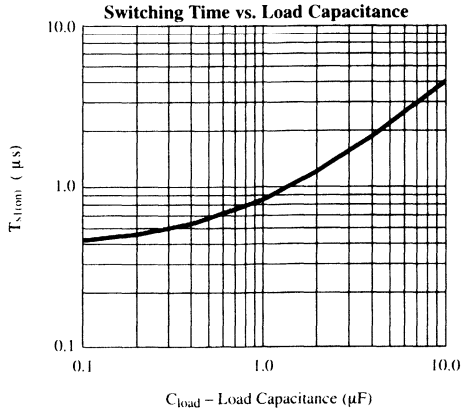


Typical Characteristics (25°C Unless Otherwise Noted)

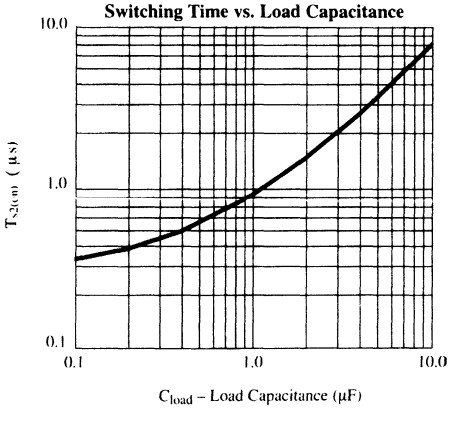
Switch 4
On-Resistance vs. V_{IN}



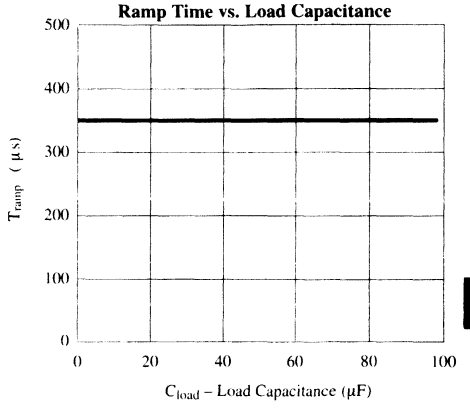
Switch 1
Switching Time vs. Load Capacitance



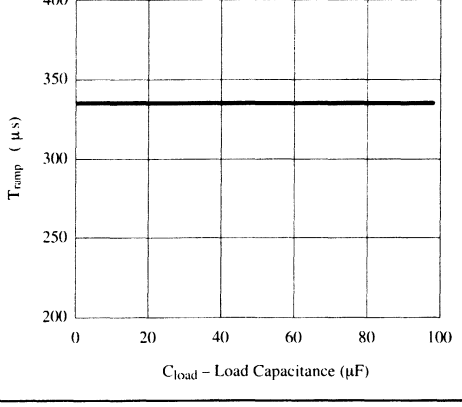
Switch 2
Switching Time vs. Load Capacitance



Switch 3
Ramp Time vs. Load Capacitance



Switch 4
Ramp Time vs. Load Capacitance



PC Card (PCMCIA) Interface Switch–12-V Suspend Capability

Features

- Programmable V_{CC} Ramp
- Smart Switching
- 12-V Sleepmode Compatible
- Extremely Low R_{ON}
- Reverse Blocking Switches
- V_{PP} Programmable to 0, 12-V or V_{CC}
- Safe Power-Up
- Low Power Consumption
- PC Card 3-V/5-V Compatible
- Logic Compatible Inputs
- Single SO-16 Package

Description

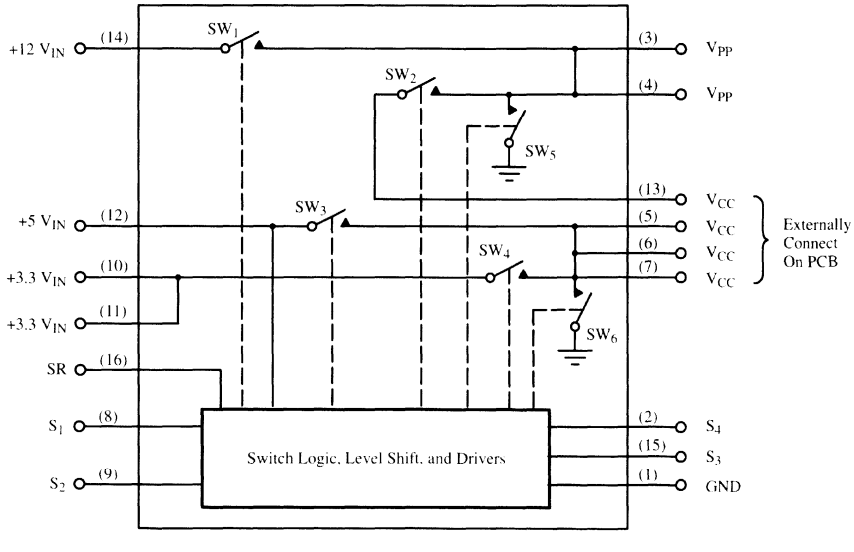
The Si9712DY combines low on-resistance with slow ramp time and smart switching for overall best performance in integrated PC Card interface switches.

The Si9712DY operates off the 5-V supply and has built-in level shifting for gate drive. Internal logic protects against an external control input error that would short 5 V to the 3.3-V supply. This protection logic also allows the Si9712DY to be configured for positive or negative control logic for compatibility with a variety of PC Card controllers. These control inputs are CMOS logic compatible and can be driven to 3.3 V or 5 V.

The Si9712DY complies with the release of the PC Card standard by suppling 0 V, 12 V, and V_{CC} to the V_{pp} output and 0 V, 3.3 V, and 5 V to the V_{CC} output. The V_{CC} ramp time is user programmable with an external capacitor connected to the SR pin.

The PC Card switch is packaged in a narrow body SO-16 package and is rated over the industrial temperature range –40 to 85°C.

Functional Block Diagram



Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70024.

Absolute Maximum Ratings

Voltages Referenced to Ground
+12 V_{IN} ..... 15 V
+5 V_{IN} ..... 7 V
+3.3 V_{IN} [c] ..... 7 V
S_1 through S_4 (CMOS Inputs) ..... 7 V
I_{OUT} V_{PP} [a] ..... 300 mA
All Pins ..... –0.5 V
I_{OUT} V_{CC} [b] ..... 4 A

PD Max: (T_A = 25°C) ..... 2.5 W
(T_A = 85°C) ..... 1.0 W
Junction Temperature ..... 125°C
Thermal Rating—$R_{\Theta JA}$ ..... 40 °C/W

Notes
a. Pins 3, 4 connected together externally.
b. Pins 5, 6, 7, 13 connected together externally.
c. Pins 10, 11 connected together externally.

Recommended Operating Conditions

+12 V_{IN} ..... 0 or 12 V ± 10%
+5 V_{IN} (must be present) ..... 5 V ± 10%
+3.3 V_{IN} [c] ..... 3.3 V ± 10%
C_{SR} ..... 33 nF
I_{OUT} V_{PP} [a] ..... 150 mA
I_{OUT} V_{CC} [b] ..... 2 A

V_{PP} Load Capacitance ..... 10 µF Max
V_{CC} Load Capacitance ..... 150 µF Max

Notes
a. Pins 3, 4 connected together externally.
b. Pins 5, 6, 7, 13 connected together externally.
c. Pins 10, 11 connected together externally.

Specifications

Parameter	Symbol	Test Conditions Unless Otherwise Specified C_{SR} = 33 nF, +12 V_{IN} = 12 V, +5 V_{IN} = 5 V +3.3 V_{IN} = 3.3 V, Low ≤ 0.8 V, High ≥ 2.2 V		Limits –40 to 85°C Min [b]	Typ [c]	Max [b]	Unit
Switch 1							
On-Resistance	R_{ON}	I = 120 mA, +12 V_{IN} = 11.4 V S_3 = S_1 = High S_2 = S_4 = Low	T_A = 25°C			120	mΩ
			T_A = 85°C			145	
Off Current (+12 V_{IN})	I_{OFF}	+12 V_{IN} = 12.6 V S_1 = Low	T_A = 25°C			1	µA
			T_A = 85°C			10	
Switching Time	$t_{SW1(on)}$	S_2 = S_4 = Low. See Figure 1 S_3 = High		50	200	350	µs
	$t_{SW1(off)}$				1.0	10	
Delay Time	$t_{d(on)}$	See Figure 3 S_2 = S_4 = Low		1.0	6	20	ms
	$t_{d(off)}$			0.1	2.9	10	µs
Rise Time	$t_{SW1(on)}$	S_2 = S_4 = Low, S_3 = High See Figure 2		50	150	300	µs
Switch 2							
On-Resistance	R_{ON}	I = 120 mA, S_2 = S_3 = High S_1 = S_4 = Low	T_A = 25°C			150	mΩ
			T_A = 85°C			180	
Switching Time	$t_{SW2(on)}$	S_1 = S_4 = Low, S_3 = High , See Figure 1		50	200	350	µs
	$t_{SW2(off)}$				1.0	10	
Delay Time	$t_{d(on)}$	S_1 = S_4 = Low, See Figure 3		1.0	6	20	ms
	$t_{d(off)}$			0.1	1.7	10	µs
Rise Time	$t_{SW2(on)}$	S_1 = S_4 = Low, S_3 = High See Figure 2		50	150	300	µs

Specifications

Parameter	Symbol	Test Conditions Unless Otherwise Specified C_{SR} = 33 nF, +12 V_{IN} = 12 V, +5 V_{IN} = 5 V +3.3 V_{IN} = 3.3 V, Low ≤ 0.8 V, High ≥ 2.2 V		Limits –40 to 85°C Min[b]	Typ[c]	Max[b]	Unit
Switch 3							
On-Resistance	R_{ON}	I = 500 mA, S_3 = High $S_1 = S_2 = S_4$ = Low	T_A = 25°C			70	mΩ
			T_A = 85°C			95	
Off Current (V_{CC})	I_{OFF}	+5 V_{IN} = 5.5 V, V_{CC} = 0 V $S_1 = S_2 = S_3$ = Low S_4 = High +3.3 V_{IN} = Open Circuit	T_A = 25°C			1	µA
			T_A = 85°C			10	
Rise Time	$t_{SW3(on)}$	$S_1 = S_2 = S_4$ = Low, See Figure 2		0.1	1.7	10	ms
Fall Time	$t_{SW3(off)}$			3	30	50	
Switch 4							
On-Resistance	R_{ON}	I = 500 mA, S_4 = High $S_1 = S_2 = S_3$ = Low	T_A = 25°C			50	mΩ
			T_A = 85°C			70	
Off Current (+3.3 V_{IN})	I_{OFF}	+3.3 V_{IN} = 3.6 V, $S_1 = S_2 = S_3 = S_4$ = Low	T_A = 25°C			1	µA
			T_A = 85°C			10	
Rise Time	$t_{SW4(on)}$	$S_1 = S_2 = S_3$ = Low, See Figure 2		0.1	0.9	10	ms
Fall Time	$t_{SW4(off)}$			3	20	40	
Switch 5							
On-Resistance	R_{ON}	I = 2 mA, $S_1 = S_2$ = Low	T_A = 25°C		235	400	Ω
			T_A = 85°C		325	550	
Switch 6							
On-Resistance	R_{ON}	I = 2 mA, $S_3 = S_4$ = Low	T_A = 25°C		140	400	Ω
			T_A = 85°C		200	500	
Power Supply							
+5 V_{IN} Current Input (on)	$I_{+5VIN(1)}$	$S_1 = S_4$ = 0 V, $S_2 = S_3$ = 3 V			20	50	µA
	$I_{+5VIN(2)}$	$S_1 = S_4$ = 3 V, $S_2 = S_3$ = 0V			20	50	
+5 V_{IN} Current Input (off)	$I_{+5VIN(3)}$	$S_1 = S_2 = S_3 = S_4$ = 0 V			<1	10	
Switch Control Inputs							
Input Voltage High	$V_{I(H)}$	+5 V_{IN} = 5.5 V		2.2	1.8		V
		+5 V_{IN} = 4.5 V		2.2	1.6		
Input Voltage Low	$V_{I(L)}$	+5 V_{IN} = 5.5 V			1.6	0.8	
		+5 V_{IN} = 4.5 V			1.4	0.8	
Input Current High	$I_{I(H)}$	S_1 through S_4 = 5 V				1.0	µA
Input Current Low	$I_{I(L)}$	S_1 through S_4 = GND		–1.0			

Notes
a. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum.
b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

Timing Waveforms

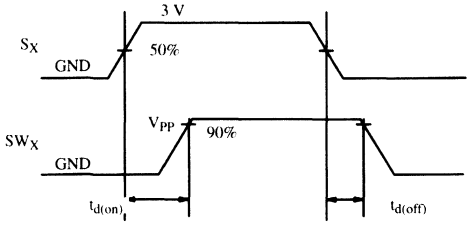


Figure 1. V_{PP} Switch Delay

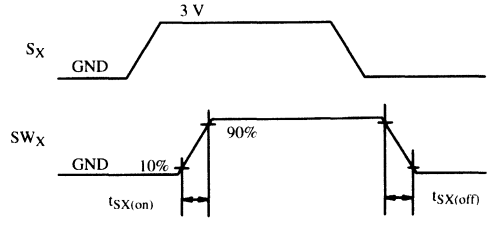


Figure 2. Switch Ramp

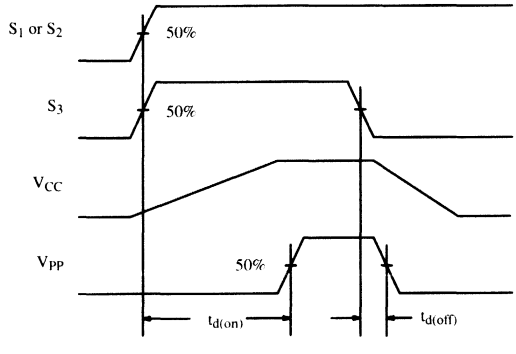
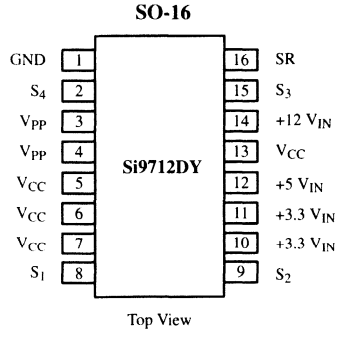


Figure 3. Delay from S_1 or S_2 to V_{PP} Power-up

Pin Configuration/Pin Description



Note: Pins 5, 6, 7, and 13 must be connected in the PCB for correct operation.

Pin Number	Function	Description
1.	GND	Ground connection.
2	S_4	Control input for selecting +3.3 V_{IN} to V_{CC}. The PC Card terminology for this pin is $V_{CC}\_EN_0$.
3, 4	V_{PP}	Program and peripheral voltage to PC Card slot.
5, 6, 7, 13	V_{CC}	Supply voltage to slot.
8	S_1	Control input for selecting +12 V_{IN} to V_{PP}. The PC Card terminology for this pin is $V_{PP}\_EN_1$.
9	S_2	Control input for selecting V_{CC} to V_{PP}. The PC Card terminology for this pin is $V_{PP}\_EN_0$.
10, 11	+3.3 V_{IN}	+3.3-V supply.
12	+5 V_{IN}	+5-V supply.
14	+12 V_{IN}	+12-V supply.
15	S_3	Control input for selecting +5 V_{IN} to V_{CC}. The PC Card terminology for this pin is $V_{CC}\_EN_1$.
16	SR	Slew rate control pin, capacitor to GND defines programmable ramp time.

Truth Table[b]

S_1	S_2	S_3	S_4	Switch 1[a]	Switch 2[a]	Switch 3	Switch 4	Switch 5	Switch 6
0	0	0	0	Off	Off	Off	Off	On	On
0	0	0	1	Off	Off	Off	On	On	Off
0	0	1	0	Off	Off	On	Off	On	Off
0	0	1	1	Off	Off	Off	Off	On	On
0	1	0	0	Off	Off	Off	Off	On	On
0	1	0	1	Off	On	Off	On	Off	Off
0	1	1	0	Off	On	On	Off	Off	Off
0	1	1	1	Off	Off	Off	Off	On	On
1	0	0	0	Off	Off	Off	Off	On	On
1	0	0	1	On	Off	Off	On	Off	Off
1	0	1	0	On	Off	On	Off	Off	Off
1	0	1	1	Off	Off	Off	Off	On	On
1	1	0	0	Off	Off	Off	Off	On	On
1	1	0	1	On	Off	Off	On	Off	Off
1	1	1	0	On	Off	On	Off	Off	Off
1	1	1	1	Off	Off	Off	Off	On	On

Notes
a. Turn on of switch 1 and 2 are internally delayed until after V_{CC} is valid. See Figure 3.
b. Shaded lines are error conditions for PC Card applications, however, switches default to the states shown.

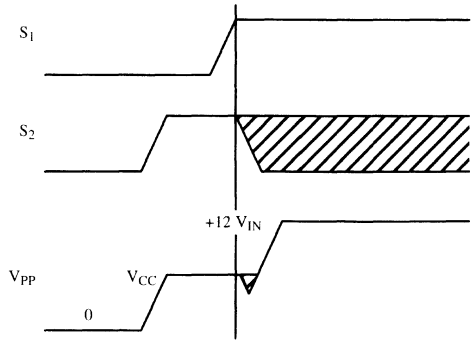
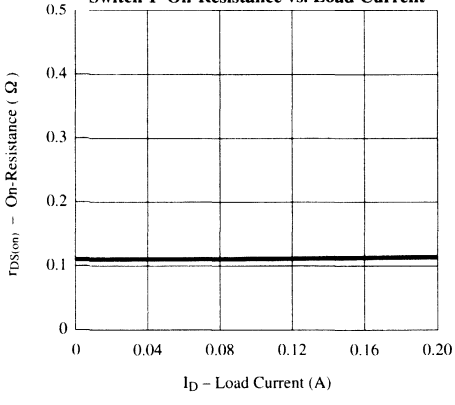


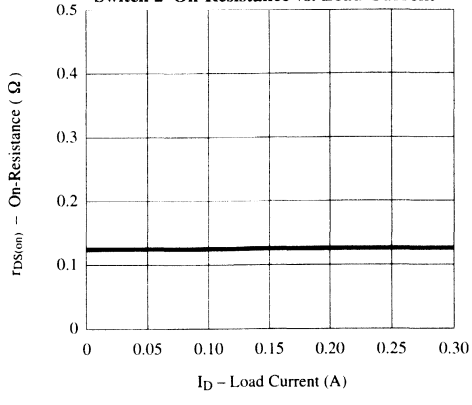
Figure 4. Break-Before-Make of SW_1 and SW_2

Typical Characteristics (25°C Unless Otherwise Noted)

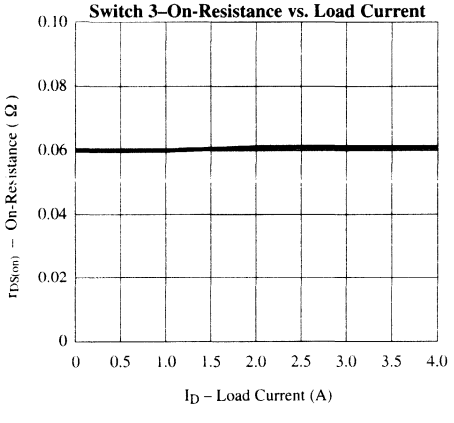
Switch 1–On-Resistance vs. Load Current



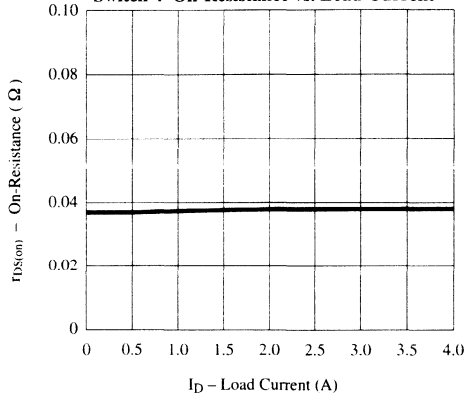
Switch 2–On-Resistance vs. Load Current



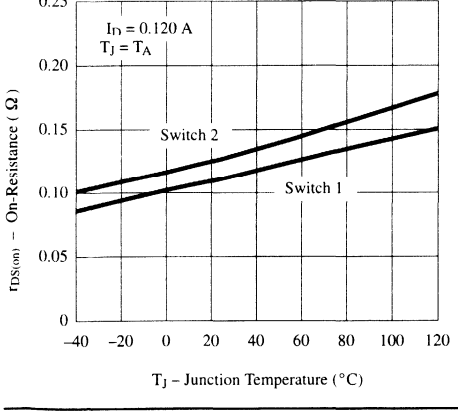
Switch 3–On-Resistance vs. Load Current



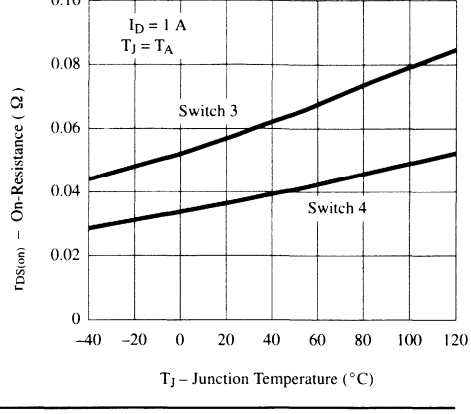
Switch 4–On-Resistance vs. Load Current



On-Resistance vs. Junction Temperature

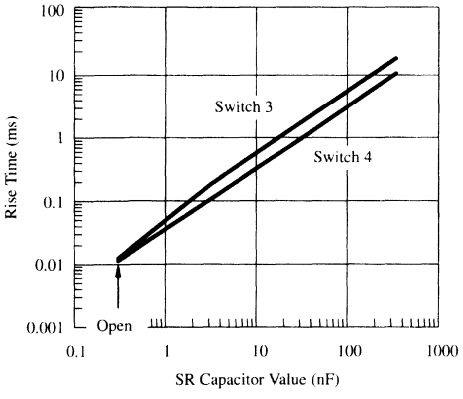


On-Resistance vs. Junction Temperature

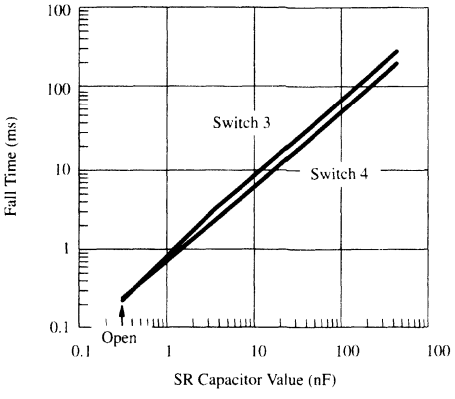


Typical Characteristics (25°C Unless Otherwise Noted)

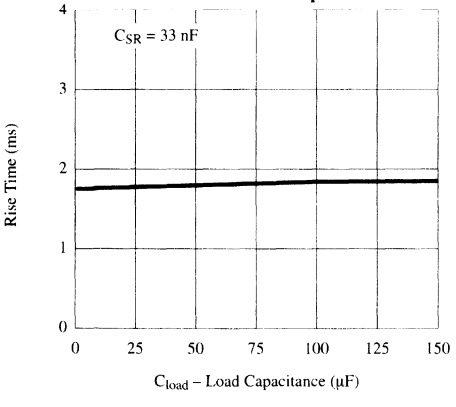
Rise Time vs. SR Capacitor Value



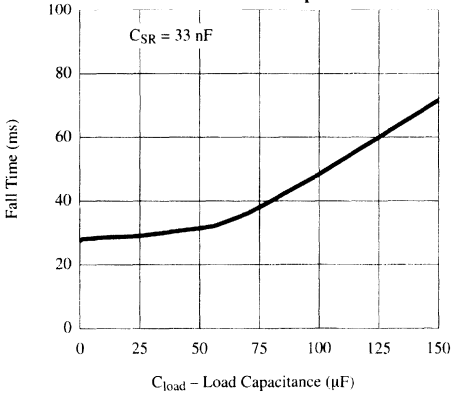
Fall Time vs. SR Capacitor Value



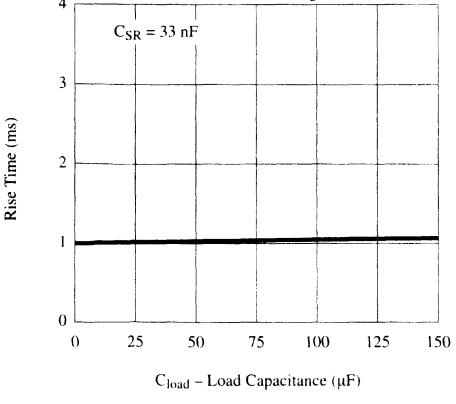
Switch 3
Rise Time vs. Load Capacitance



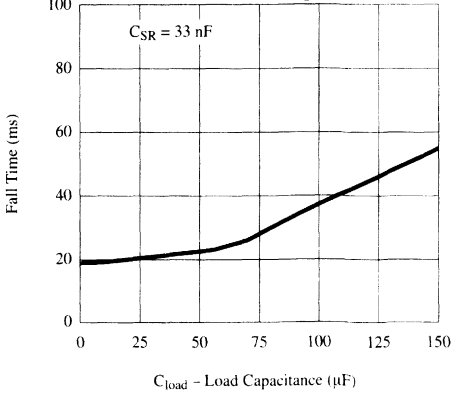
Switch 3
Fall Time vs. Load Capacitance



Switch 4
Rise Time vs. Load Capacitance



Switch 4
Fall Time vs. Load Capacitance



Designing with Siliconix PC Card (PCMCIA) Power Interface Switches

Teresa Hardy

Introduction

Innovation in portable computer design is driven today by the need for smaller, lighter, and more energy-efficient products. This has been the driving force behind the small form-factor I/O cards that have created an emerging market for PC Cards. In the current version of the PC Card standard, a computer or other "host platform" must be able to deliver some combination of 3.3, 5, and 12 V at the slot for a card to operate. These voltages are then supplied to the card on two supply lines called V_{CC} and V_{PP}.

Siliconix offers a series of integrated power MOSFETs specifically designed for the strict demands of the PC Card power interface. The Si9710CY, Si9711CY, and Si9712DY devices switch 3.3 V or 5 V to Vcc and 3 V, 5 V, or 12 V to the flash memory program pin, V_{PP}. The Si9706DY and Si9707DY are a functional subset of the Si9712DY. They support only the Vcc line for systems that use V_{PP} from the main supply or future specialized systems that do not support the V_{PP} function.

The Si97XX series of PC Card power interface switches is intended for battery-operated notebook, sub-notebook, and palmtop computers. These monolithic power ICs provide several options for any host platform power switching application. In a single surface-mount package, they provide tighter output tolerances because of their low on-resistance rating, and longer battery life, with leakage currents of less than 1 µA.

PC Card Power Switching: An Overview

Upon initial card insertion, the PC Card interface must determine its required supply voltages and wake up the card with the proper voltages supplied. The purpose of the PC Card power selector function is therefore that of a power multiplexer, as shown in Figure 1. The switch configuration has been designed for the V_{PP} output to select among all the available voltages (a four-state output), namely 12, 5, and 3.3 V along with ground (0 V). The V_{CC} line is a higher-current three-state output for 5- and 3.3-V circuitry, which also can provide a grounded condition.

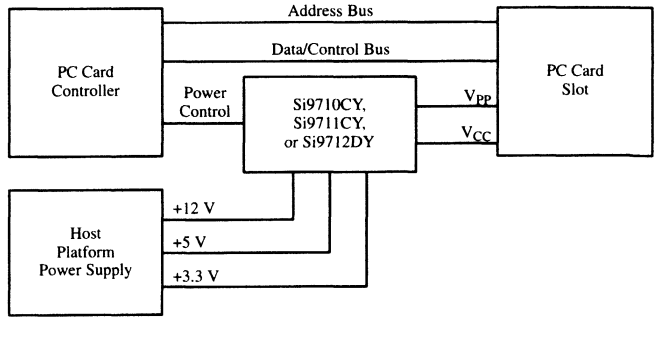


Figure 1. Function of Power Selector for PC Cards

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Voltage Requirements and Reverse-Blocking Capability

The power switch requirements in the PC Card voltage selector are unique for at least four reasons. ***First***, the power selector's control interface must follow the PC Card communication format (and interface conveniently to PC Card controller ICs). While the control signals from the interface chip are 3- or 5-V CMOS logic, the 12-V signals must be controlled from this lower voltage input using level shifting. ***Second***, the switches must be bidirectionally blocking since any one of the supplies may go to sleep and short to ground. If the output is held high by another switch, the input is then at a lower potential than the output. One example of this condition is where S1 is off and S2 (as shown in Figure 3 and Figure 4) is on so that V_{PP} is biased to the same potential as V_{CC}. In the event that the 12-V input drops and the supply sleeps, S1 changes from a state where its input voltage exceeds its output to the opposite polarity. Similar cases can occur with S3 and S4.

Low On-Resistance Issues

The ***third*** unique aspect of the PC Card voltage selector function is the need for low on-resistance switches, generally below 200 mΩ on the V_{PP} = 12 V switch and even as low as 60 mΩ on the 3.3-V switch. The low on-resistance is not necessarily needed for reasons of power dissipation or high current, but rather to prevent significant voltage drops across the switch. In general, the input to the switch from the system supply may be 4% below nominal, leaving only one percent for the switch. The PC Card standard specifies a maximum variation of ±5% on both V_{CC} and V_{PP}. This structure is clearly driven by Flash RAM requirements on V_{PP} and the tight rail voltage on 3.3-V ICs. Therefore, the system designer must consider the allowable voltage drop for a maximum expected current on both V_{CC} and V_{PP}. For a 500-mA load at 5 V on V_{CC}, a 1% voltage drop requires a maximum on-resistance of 100 mΩ. The Si9712DY exceeds this requirement over the full temperature range (-40 to 85°C). Assuming a slightly lower current requirement at 3.3 V, the Si9712DY meets 1% voltage drop over the operating temperature range with a maximum specified on-resistance of 80 mΩ.

Because of Siliconix' pioneering efforts in battery disconnect switches, the PC Card power selector function has been integrated monolithically using the proprietary BCD15 technology. This integrated function actually replaces seven to nine discrete power MOSFETs per slot beyond those involved in the interface and level shifting circuitry.

Controlling the Power-Up

The ***fourth*** unique aspect of the PC Card power selector is its need for controlled slew rates on the 3.3-V and 5-V switches. The requisite switching times range from hundreds-of-microseconds to milliseconds: extremely long intervals for integrated circuit technology. Because of the versatility of our BCD15 technology, however, Siliconix can control the power device behavior over such long intervals.

Designers face a dilemma when dealing with switching ramp times. On the one hand, fast rise times are directly related to the current spikes that can shut down some host platforms. Even the capacitors on PC cards themselves can be damaged by surge currents. Yet some designers correctly wonder whether the ramp time called out by the PC Card Rev. 2.1 standard, as slow as 300 ms, is actually so slow as to latch up and draw excessive current.

The rules in this area are different for different types of host platforms. The small handheld systems that operate off A-cells cannot supply the current to support a fast ramp to a large load. In fact, many of these palmtops attempt to avoid the issue by not offering a Type III slot (although some Type II cards can be categorized as high-power cards). The larger portables have what it takes to supply power to a wider range of cards such as rotating media and the more powerful multimedia or wireless communications cards. For the sake of this discussion, we will group these higher-power systems together as the notebooks.

If a host platform power supply can only handle a certain peak current, then it should control the ramp to support that limit over the range of available cards. Unfortunately, the growing number of card vendors makes the card load a difficult parameter to define without extensive research. According to ongoing surveys of card manufacturers contacted by Siliconix, this capacitance can be as high as 150 µF. Indeed, cards can be grouped in at least two categories: high-power cards that can have as much as 150-µF bypass on V_{CC}, and low-power cards that are well below a 50-µF bypass on V_{CC}. With these parameters in mind, it is clear from Figure 2 that the host platform with a surge current capability in the milliamp range would need to support a ramp in the low millisecond range for the most reliable operation over the full range of cards.

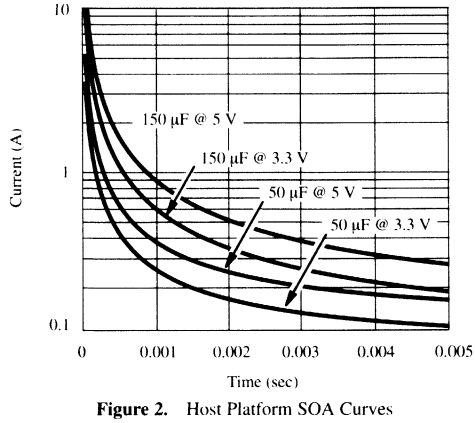


Figure 2. Host Platform SOA Curves

The curves in Figure 2 show the safe operating area based on a worst-case assumption of 150-µF card capacitance on V_{CC}. These curves are based on the following calculation:

$$i = C(dv/dt) + I_{steady\ state}$$

where $I_{steady\ state}$ is estimated at 100 mA for 5 V and 70 mA for 3.3 V during the time before the CIS register is read. A 2 ms ramp time is an ideal ramp for a platform that can support a 500-mA surge over the range of card capacitance values. The notebook category of platforms can tolerate a ramp less than 1 ms.

Si9711CY

A host platform design that can support a surge of close to 4 A can comfortably use the Si9711CY, which ramps at 200 µs. However, those systems that cannot tolerate this kind of peak current will be better off with the Si9712DY, which maintains a ramp closer to 1 ms. The Si9706DY and Si9707DY are modelled after the Si9712DY, and therefore support the slower ramp. The Si9710CY does not support the slow ramp. Therefore, for designs originally intended for the Si9710CY, Siliconix recommends a pin-compatible upgrade to the Si9711CY.

Pin Description for Si9710CY and Si9711CY

S1, S2, S3, S4 (Pins 15, 16, 1, 2)

Control input for selecting appropriate outputs on both V_{CC} and V_{PP}. These four inputs are CMOS compatible and can accommodate 3.3-V and 5-V rails by connecting V_L to the appropriate rail voltage. Each control pin (S1, S2, S3, and S4) individually controls its respective switch (SW1, SW2, SW3, and SW4).

V_L (Pin 14)

This pin is an input to indentify the rail voltage for the control inputs. Connect V_L to the same rail voltage of the PC Card controller for signal voltage compatibility.

+3.3 V_{IN} (Pins 9 and 10)

These pins are the input to provide +3.3 V to the V_{CC} pins of the slot by way of Switch 4, and to V_{PP} by way of Switch 2. Connect these pins to the host platform +3.3-V supply.

+5 V_{IN} (Pin 11)

This pin is the input to provide +5 V to the V_{CC} pins of the slot by way of Switch 3, and to Vpp by way of Switch 2. Connect this pin to the host platform +5-V supply.

+12 V_{IN} (Pin 13)

This pin is the input to provide +12 V to the slot V_{PP} by way of Switch 1. The +12 V_{IN} pin is also used to generate the internal gate drive voltage; therefore, it is important that +12 V is continuous. Connect this pin directly to the host platform +12-V supply. See the section on suspend mode operation for non-continuous 12-V systems.

V_{CC} (Pins 6,7,8,12)

PC Card slot supply voltage. Connect all four pins together and to pins 17 and 51 of the PC Card slot.

Vpp (Pins 4 and 5)

PC Card program and peripheral voltage to slot. Connect both pins together and to pins 18 and 52 of the PC Card slot.

GND (Pin 3)

Ground reference connection. Connect this pin to host platform system ground.

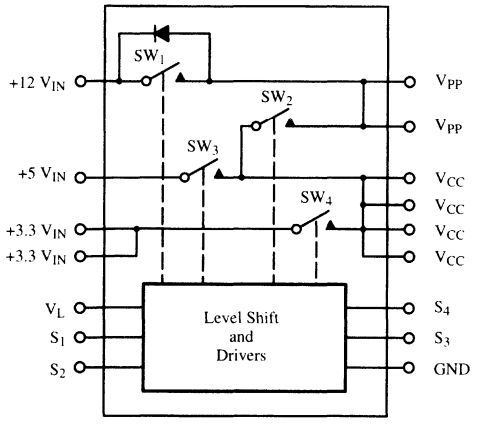


Figure 3. Si9710CY/11CY Functional Block Diagram

Table 1. Si9710CY/11CY Truth Table

S1	S2	S3	S4	V_{PP}	V_{CC}
0	0	0	0	HiZ	HiZ
0	0	0	1	HiZ	3.3 V
0	0	1	0	HiZ	5 V
0	0	1	1	HiZ	Invalid State
0	1	0	0	HiZ	HiZ
0	1	0	1	3.3 V	3.3 V
0	1	1	0	5 V	5 V
0	1	1	1	V_{CC}	Invalid State
1	0	0	0	HiZ	HiZ
1	0	0	1	12 V	3.3 V
1	0	1	0	12 V	5 V
1	0	1	1	12 V	Invalid State
1	1	0	0	Invalid State	HiZ
1	1	0	1	Invalid State	Invalid State
1	1	1	0	Invalid State	Invalid State
1	1	1	1	Invalid State	Invalid State

Si9712DY

The Si9712DY is functionally similar to the Si9710CY and Si9711CY with added features. The upgraded configuration of the Si9712DY provides a zero voltage output on V_{CC} and V_{PP}, programmable ramp time on V_{CC}, and meets the PC Card revision 3 PC Card specification scheduled for release in January 1995. Most importantly, it offers better on-resistance in the same package style.

Portable system designers who are interested in maintaining the V_{CC} ±5% tolerance called out in the PC Card standard will find Si9712DY the best choice. It is designed to support slots intended for "high-power" cards requiring more than an ampere of surge current during normal operation. Some cards that are considered "high-power" cards include rotating media, multimedia, and some wireless communication cards.

The Si9712DY also appeals to the system designer because of the easy interface with the variety of industry-standard controllers. The control inputs for V_{CC} can be configured as active high or active low by simply swapping S3 and S4. Table 2 shows that (1, 1) and (0, 0) on S3, S4 both yield zero out of V_{CC}. Therefore, crossing control lines for SW3 and SW4 will simply change the polarity of the control.

System designers using custom PC Card controllers that are pin constrained may consider tying S2 control high. The Si9712DY truth table (Table 2) shows that S1 will dominate. This limits the operation of the interface by not allowing a state for zero on V_{PP} while V_{CC} is active.

Pin Description for the Si9712DY

S1, S2, S3, S4 (Pins 8, 9, 15, 2)

Control input for selecting appropriate outputs on both V_{CC} and V_{PP}. These four inputs are CMOS compatible and can accommodate 3.3-V and 5-V rails. Each control pin (S1, S2, S3, and S4) individually controls its respective switch (SW1, SW2, SW3, and SW4).

+3.3 V_{IN} (Pins 10 and 11)

These pins are the input to provide +3.3 V to the V_{CC} pins of the slot by way of Switch 4, and to V_{PP} by way of Switch 2. Connect these pins to the host platform +3.3-V supply.

+5 V_{IN} (Pin 12)

This pin is the input to provide +5 V to the V_{CC} pins of the slot by way of Switch 3, and to V_{PP} by way of Switch 2. The +5 V pin is also used to generate the internal gate drive voltage; therefore, it is important that +5 V is continuous. Connect this pin to the host platform +5-V supply. See also the section on advanced sleep modes.

+12 V_{IN} (Pin 14)

This pin is the input to provide +12 V to the V_{PP} of the slot by way of Switch 1. Connect this pin directly to the host platform +12-V supply.

V_{CC} (Pin 5, 6, 7, 13)

PC Card slot supply voltage. Connect all four pins together and to pins 17 and 51.

V_{PP} (Pin 3 and 4)

PC Card program and peripheral voltage to slot. Connect both pins together and to pins 18 and 52.

SR (Pin 16)

Connect a capacitor to the SR pin to adjust the slew rate of the V_{CC} ramp. Recommended capacitance value is identified in the data sheet. This capacitor can be omitted for designs that can tolerate the faster ramp as shown in the Si9712DY data sheet curves.

GND (Pin 1)

Ground reference connection. Connect this pin to the host platform system ground.

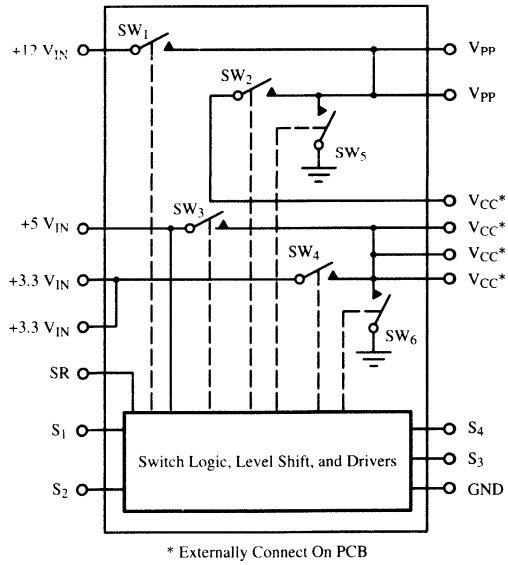


Figure 4. Si9712DY Functional Block Diagram

Table 2. Si9712DY Truth Table

S1	S2	S3	S4	V_{PP} (V)	V_{CC} (V)
0	0	0	0	0	0
0	0	0	1	0	3.3
0	0	1	0	0	5
0	0	1	1	0	0
0	1	0	0	0	0
0	1	0	1	3.3	3.3
0	1	1	0	5	5
0	1	1	1	0	0
1	0	0	0	0	0
1	0	0	1	12	3.3
1	0	1	0	12	5
1	0	1	1	0	0
1	1	0	0	0	0
1	1	0	1	12	3.3
1	1	1	0	12	5
1	1	1	1	0	0

Si9706DY and Si9707DY

The Si9706DY and Si9707DY are interface switches that support only the V_{CC} pins of the PC Card interface. They are intended for systems that support the Vpp programming voltage at the main supply such as the Maxim MAX783 dc-to-dc controller shown in Figure 7.

The Si9706DY is a single V_{CC} power interface switch in an 8-pin SOIC package that switches 3.3 V, 5 V, or 0 V to the V_{CC} pins of the PC Card slot. The Si9707DY is an SO-16 that is equivalent to two Si9706DYs. Both devices have the slow V_{CC} ramptime and smart switching featured in the Si9712DY. The simplified truth table for the Si9706DY and Si9707DY is shown in Table 3.

Table 3. Si9706DY/07DY Truth Table

S1	S2	V_{CC}
0	0	0 V
0	1	3.3 V
1	0	5 V
1	1	0 V

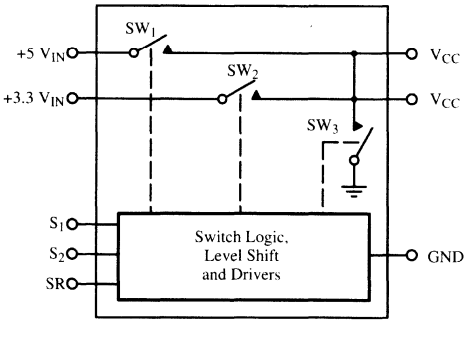


Figure 5. Si9706DY Functional Block Diagram

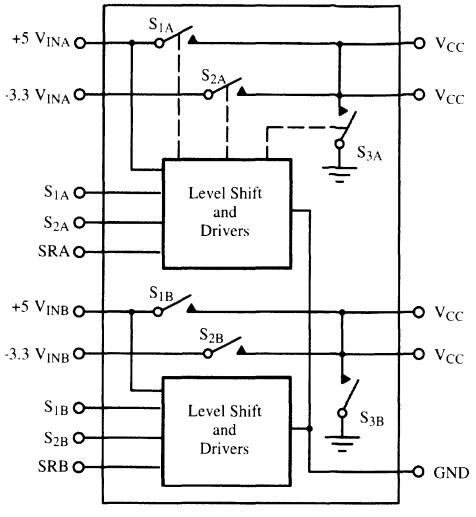


Figure 6. Si9707DY Functional Block Diagram

Pin Description for the Si9706DY/9707DY

S1, S2

(Si9706DY: Pin 4, 5) (Si9707DY: Pin 15, 2, 10, 7)

Control input for selecting appropriate outputs on V_{CC}. These two inputs are CMOS compatible and can accommodate 3.3-V and 5-V rails by setting V_L. Table 3 shows V_{CC} output for all states on S1 and S2. For PC Card controllers with active low control signals, S1 and S2 can be reversed.

+3.3 V_{IN}

(Si9706DY: Pin 6) (Si9707DY: Pin 11, 14)

This pin is the input for +3.3 V to be connected to V_{CC} by way of Switch 4. Connect this pin to the host platform +3.3-V supply.

+5 V_{IN}

(Si9706DY: Pin 7) (Si9707DY: Pin 12, 13)

This pin is the input for +5 V to be connected to Vcc by way of Switch 3. Connect this pin to the host platform +5-V supply.

V_{CC}
(Si9706DY: Pin 2, 3) (Si9707DY: Pin 3, 4, 5, 6)

PC Card slot supply voltage. For the Si9706DY, connect pins 2 and 3 of the IC to pins 17 and 51 of the PC card connector. For the Si9707DY, pins 5 and 6 connect to slot A and pins 3 and 4 connect to the slot B pins 17 and 51.

SR
(Si9706DY: Pin 8) (Si9707DY: Pin 9, 16)

Connect a capacitor to the SR pin to adjust the slew rate of the V_{CC} ramp. Recommended capacitance value is identified in the data sheet.

GND
(Si9706DY: Pin 1) (Si9707DY: Pin 8, 1)

Ground reference connection. Connect this pin to host platform system ground.

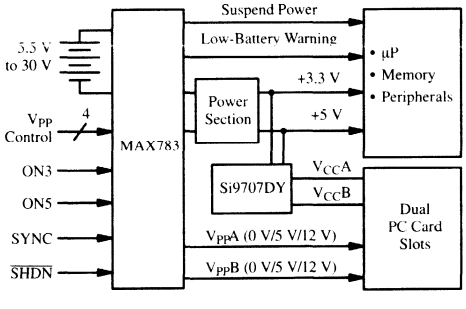


Figure 7. Power System Block Diagram Using MAX783 and Si9707DY for Dual PC Card Slots

Sleep Mode Support

One of the most common ways of extending battery life is to turn off those supplies which are not being used. Designs that support a power management philosophy that causes +12-V to be intermittent would find the Si9712DY a more suitable part. However, host platforms that turn off the +12-V supply can still use the Si9711CY with the simple external circuit shown in Figure 8.

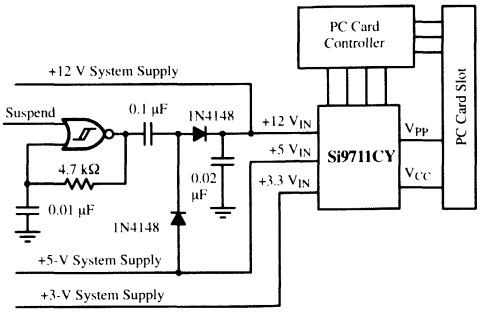


Figure 8. Si9711CY Sleep Mode

Advanced Sleep Mode Support

Today's portable systems have multiple levels of suspend, sleep, or deep-sleep. In certain host platforms, a suspend mode may require maintaining an active slot with the +5-V supply turned off. The best application example for this case is a host platform with a fax/modem card that wakes the system on detecting a ring on the line. This kind of sleep can be done either by using an external circuit similar to the one shown in Figure 8 for suspending +12-V, or by reducing the +5 V_{IN} to 3.3-V. The Si9712DY is functional with no increased on-resistance for card currents below 100 mA (Figure 10).

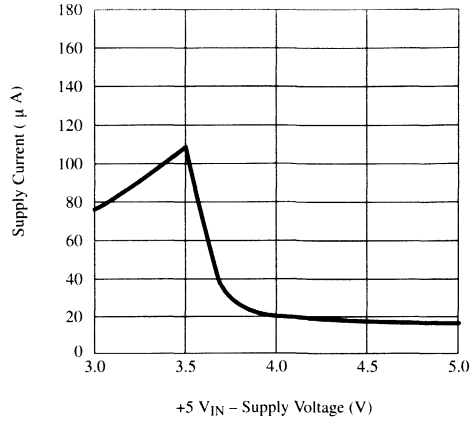


Figure 9. Si9712DY Current Draw During Suspend

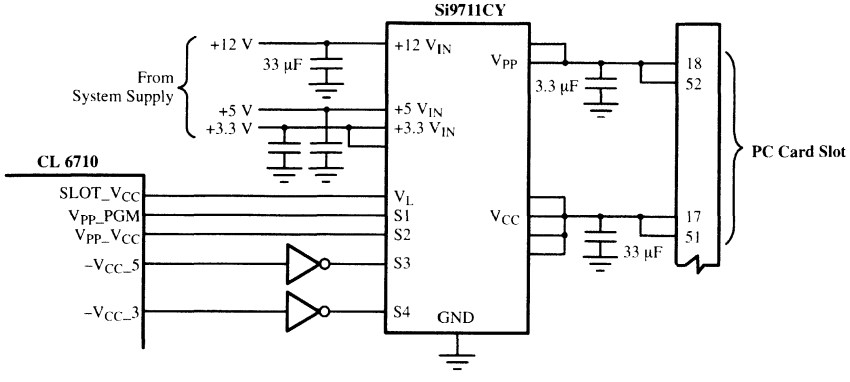


Figure 10. Si9711CY System Implementation

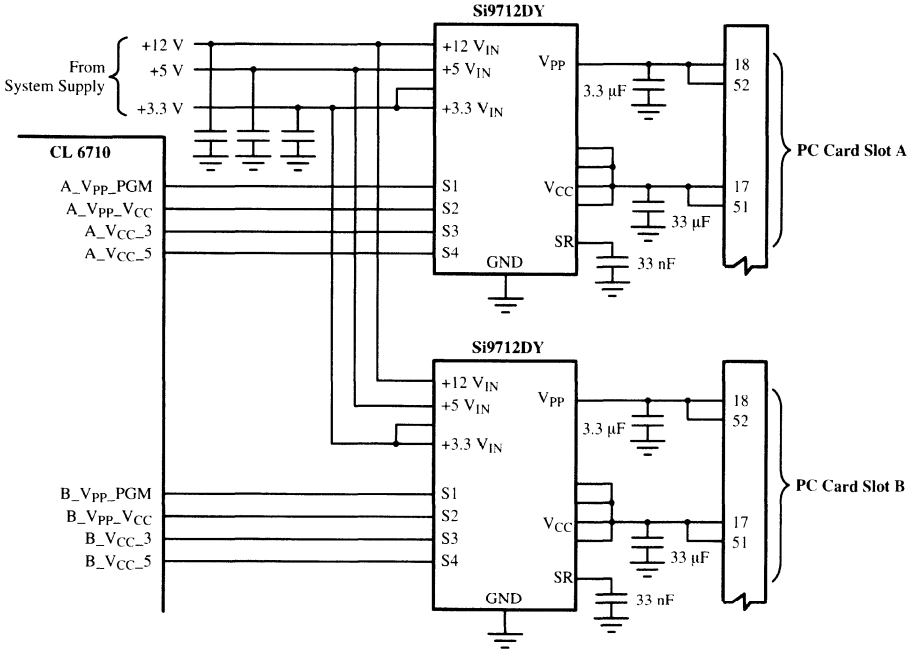


Figure 11. Si9712DY System Implementation

Controller Interface with the Si9711CY

The Si9711CY has individual lines for each switch in the power interface. These control lines can be connected directly to industry-standard controllers that have active high outputs for the switch enables. For controllers that output active low signals for V_{CC} control, such as the Cirrus 6710, the interface would require two inverting buffers as shown in Figure 11. The system power supply, or input side of the switch for 3.3-, 5-, and 12-V should have sufficient bypass capacitance to prohibit switching noise from feeding back into the system supply. For example, the bypass capacitor on +12 V_{in} has been selected as 10 X the bypass on the V_{PP} output pin. Bypass capacitance on the 3.3-V and 5-V inputs will vary based on system implementation and the intended power level that the slot is intended to support. Capacitor values for V_{CC} and V_{PP} are left up to the individual system designer. However V_{CC} should be at least 10 X the capacitance of V_{PP}. They should be selected for optimum ESD protection since these pins interface directly to the PC Card slot.

Controller Interface with the Si9712DY

The Si9712DY interface supports both active-high and active-low V_{CC} control. The smart switching feature allows the designer to swap the 3.3- and 5-V control to produce an active low interface as shown in Figure 11 with the Cirrus 6720 in a dual-slot configuration.

Controller Interface with the Si9706DY/07DY

The Si9706DY and Si9707DY interfaces directly to industry-standard PC Card controllers. The Si9707DY would provide the best system choice with the MAX783 dc/dc controller and the Cirrus 6720 dual slot PC Card controller. The Si9706DY and Cirrus 6710 with the MAX783 provide a complete solution for single slot configurations. The Si9706DY and Si9707DY support active high and active low control signals in the same way as Si9712DY.

In-Rush Current Limit MOSFET Driver

Features

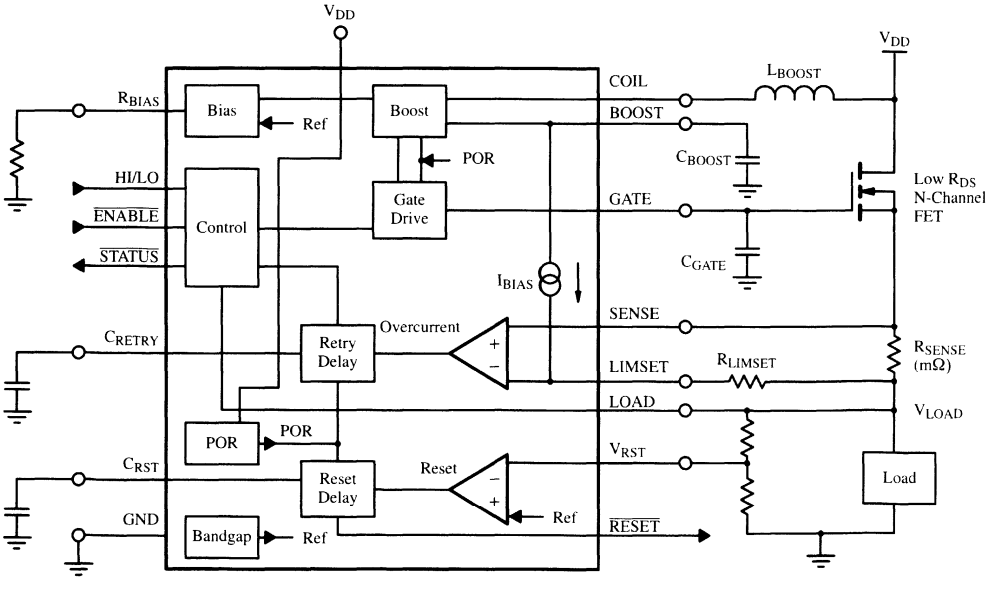
- 2.9- to 13-V Input Operating Range
- Microprocessor $\overline{\text{RESET}}$
- Integrated High-Side Driver for N-Channel MOSFET
- Programmable di/dt Current

Description

The Si9750 current limit MOSFET interface IC is designed to operate between a power source and a load using a low on-resistance power MOSFET with a sense terminal or in conjunction with a low ohmic sense resistor. The Si9750 current limiter prevents source and load transients during hot swap and power-on with programmable dv/dt and di/dt. Both turn-on and steady-state current limits can be individually programmed, providing protection against short circuits. Power on $\overline{\text{RESET}}$ and logic controls allow complete microprocessor interfacing. The $\overline{\text{RESET}}$ function of the Si9750 is industry-standard with full programmability.

The Si9750 is available in a 16-pin SOIC package and is rated over the commercial temperature range (0 to 70°C).

Functional Block Diagram



Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70028.

Absolute Maximum Ratings

Voltages Referenced to Ground
V_{DD} ..... 15 V
Boost Voltage ..... 29 V
Inputs/Outputs
(except Gate, Boost and V_{RST}) ..... –0.3 to V_{DD} + 0.3 V
V_{RST} Input Current (0 < V_{RST} < 15 V) ..... 20 mA
Inputs/Outputs Current ..... 20 mA
$\overline{RESET}$ Current ..... 3 mA
$\overline{STATUS}$ Current ..... 3 mA

Storage Temperature ..... –65 to 125°C
Junction Temperature ..... 150°C
Power Dissipation (package)[a]
16-Pin SOIC[b] ..... 900 mW
Thermal Impedance (Θ_{JA}) ..... 140°C/W

Notes
a. Device mounted with all leads soldered or welded to PC board.
b. Derate 7.2 mW/°C above 25°C.

* *Exposure to Absolute Maximum rating conditions for extended periods may affect device reliability. Stresses above Absolute Maximum rating may cause permanent damage. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum rating should be applied at any one time*

Specifications

Parameter	Symbol	Test Conditions Unless Otherwise Specified 2.9 V ≤ V_{DD} ≤ 13.2 V HI/LO = GND, R_{BIAS} = 12.5 kΩ L_{BOOST} = 100 µH, C_{BOOST} = 100 nF	Limits 0 to 70°C Min[a]	Typ[b]	Max[a]	Unit
Supply						
Quiescent Current	I_Q	$\overline{ENABLE}$ =Logic Low		4	8	mA
Logic						
Enable Turn-On Voltage	$V_{EN(on)}$				0.3 x V_{DD}	V
Enable Turn-Off Voltage	$V_{EN(off)}$		0.7 x V_{DD}			
Enable Source Current	I_{ENSRC}	V_{ENABLE} = 0V	40		120	µA
Turn-On Time	t_{ON}	See Figure 3.			5	µs
Turn-Off Time	t_{OFF}				5	
Turn-On Boost	$t_{ON(BST)}$	See Figure 4.			600	
t_{OFF} Initial Short Circuit	$t_{OFF(ISC)}$	C_{GATE} = 33 nF, See Figure 6.			10	
t_{OFF} Short Circuit	$t_{OFF(SC)}$	C_{GATE} = 33 nF, See Figure 7.			2	
Status Output Voltage	V_{STAT}	I_{SINK} = 200 µA			0.4	V
Status Output Delay Time	t_{STDLY}	See Figure 8.			25	µs
Status Threshold	$V_{STATTHR}$		0.85 x V_{DD}		0.95 x V_{DD}	V
HI/LO Turn-On Voltage	$V_{HILO(on)}$		0.7 x V_{DD}			
HI/LO Turn-Off Voltage	$V_{HILO(off)}$				0.3 x V_{DD}	
Gate Drive						
Enhancement Voltage (V_{GATE} – V_{SENSE})	V_{GS}		8.5	10.5	15	V
Source Current	I_{SOURCE}	V_{CBOOST} = 9 V	1.06	1.30	1.54	mA
Sink Current	I_{SINK}		1.6	2.6	3.7	

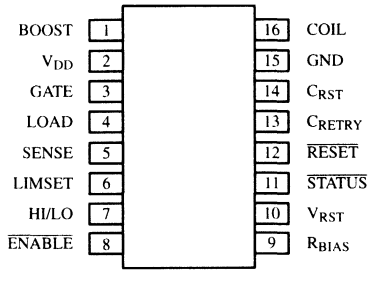
Specifications

Parameter	Symbol	Test Conditions Unless Otherwise Specified 2.9 V ≤ V_{DD} ≤ 13.2 V HI/LO = GND, R_{BIAS} = 12.5 kΩ L_{BOOST} = 100 µH, C_{BOOST} = 100 nF	Limits 0 to 70°C Min[a]	Typ[b]	Max[a]	Unit
Current Sense Circuit						
Current Sense Amplifier Common Mode Range	V_{CMR}		0		V_{DD} + 0.3	V
Current Sense Amplifier Voltage Offset	V_{OS}		–3		3	mV
Current Sense Amplifier Bias Current	I_{SOS}	Normal Operation		–0.2		µA
R_{LIMSET} Reference Current	$I_{RLIMSET}$		18	19.5	21	
Current Sense Amplifier Hysteresis	V_{HYST}			12		mV
Current Sense Amplifier Series Offset	V_{SOS}	HI/LO = V_{DD}, V_{CMR} > 0.5 V		20		
Power On Reset						
$\overline{\text{RESET}}$ Output Voltage	$V_{OP(rst)}$	I_{OUT} = 1 mA, V_{DD} > 2 V			0.4	V
$\overline{\text{RESET}}$ Output Hysteresis[c]	V_{HYST}	See Note c		2		mV
$\overline{\text{RESET}}$ Comparator Input Threshold	V_{RST}		1.223	1.250	1.277	V
$\overline{\text{RESET}}$ Comparator Offset Voltage[d]	V_{RBIAS}			0.5		mV
$\overline{\text{RESET}}$ Comparator Input Bias Current	I_{BIAS}			–0.2		µA
$\overline{\text{RESET}}$ Timer Delay	t_{RSTD}	C_{RST} = 15 nF, See Figure 8.	110	150	190	µs
RETRY	t_{RETRY}	C_{RETRY} = 100 nF	70	130	200	ms

Notes
a. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum.
b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production test.
c. In a practical situation, V_{HYST} is multiplied by ratio of a resistor divider chain. For V_{DD} = 13.2 V, V_{HYST} = 20 mV.
d. The $\overline{\text{RESET}}$ comparator input threshold specification (V_{RST}) includes the $\overline{\text{RESET}}$ comparator offset voltage.

Pin Configuration

SO-16



Top View

Order Number: Si9750CY

Pin Description

Pin Number	Function	Description
1	BOOST	Output of on-chip Boost converter. A 100-nF capacitor should be connected between BOOST and GND
2	V_{DD}	Positive supply pin.
3	GATE	Connection to external power MOSFET gate.
4	LOAD	Connection to positive supply side of LOAD.
5	SENSE	Connects external sense resistor of a sensefet sense pin to SENSE input of overcurrent trip comparator. A standard MOSFET may also be used in conjunction with a low ohmic value shunt resistor.
6	LIMSET	Connects overcurrent limit set resistor R_{LIMSET} to the reference input of overcurrent trip comparator.
7	HI/LO	CMOS logic input to control the overcurrent trip comparator sensitivity at power-on. HI/LO should be connected to GND for low Capacitive loads and to V_{DD} for high capacitive loads.
8	$\overline{ENABLE}$	CMOS logic input to turn IC on or off. GATE voltage remains low when $\overline{ENABLE}$ is high.
9	R_{BIAS}	A resistor connected from this pin to GND programs the reference bias current for the overcurrent trip comparator resistor R_{LIMSET} and the $GATE_{(on)}$ charge current. See Functional Description for equations.
10	V_{RST}	Input to voltage monitor comparator.
11	$\overline{STATUS}$	Open drain NMOS output. This pin is driven low when the current limiter is enabled and the LOAD voltage is greater than 90% of V_{DD}.
12	$\overline{RESET}$	Open drain NMOS output. This pin is driven low during power on reset or when V_{RST} is lower than the internal 1.25-V reference.
13	C_{RETRY}	A capacitor connected from this pin to GND programs the retry timer.
14	C_{RST}	A capacitor connected from this pin to GND programs the reset timer.
15	GND	Negative supply pin.
16	COIL	Connection to Boost converter inductor.

Functional Description

The Si9750 together with an n-channel MOSFET provides the following functions:

- limits di/dt current for hot insertion applications
- provides complete short circuit protection
- high-side drive allows n-channel MOSFET to be used, for lower power dissipation
- industry-standard microprocessor reset function
- logic control input and outputs

Setting the Current Limit (SENSE, HI/LO pins, R_{LIMSET}, R_{SENSE})

The current limit point is determined by the voltage across R_{SENSE}, the value of R_{LIMSET}, and the bias current. The current limit circuit is shown in Figure 1.

The steady state current is set by the equation:

$$I_{LOAD} \times R_{SENSE} > I_{BIAS} \times R_{LIMSET} \quad (1)$$

Due to the highly capacitive nature of some loads, the Si9750 has an option to increase the current limit point to a much higher level at turn-on. In this case, turn-on is defined as $V_{GATE} < V_{DD} + 7.8$ V. This function is implemented with the HI/LO pin. If the HI/LO pin is tied low the current limit is 20% higher during turn-on than the steady state current limit point.

$$I_{LOAD} \times R_{SENSE} > 1.2 \times I_{BIAS} \times R_{LIMSET} \quad (2)$$
(with pin HI/LO=Low)

If a higher current limit is needed at start-up, the HI/LO pin can be tied high. The equation becomes:

$$I_{LOAD} \times R_{SENSE} > 1.2 \times I_{BIAS} \times R_{LIMSET} + I_{BIAS}(1\ k\Omega + R_{HI}) \quad (3)$$
(HI/LO = High)

Notice that any current limit can be set at turn-on using an optional resistor, R_{HI}.

Relaxation Mode Current Limit (C_{RETRY} pin)

In an overload condition, the Si9750 will go into a relaxation mode current limit operation that not only protects the source and load, but also reduces the power dissipated in the MOSFET. When an overload is detected, the circuit quickly turns off, then goes into a retry mode whereby the current is ramped up slowly. If the fault still exists, the current will ramp down again. This sequence will repeat indefinitely at a period defined by $10^6 \times C_{RETRY}$ until the fault is removed. Typically, capacitors in the range of 1 nF to 1 µF can be used on C_{RETRY}, but the period should be >50 ms.

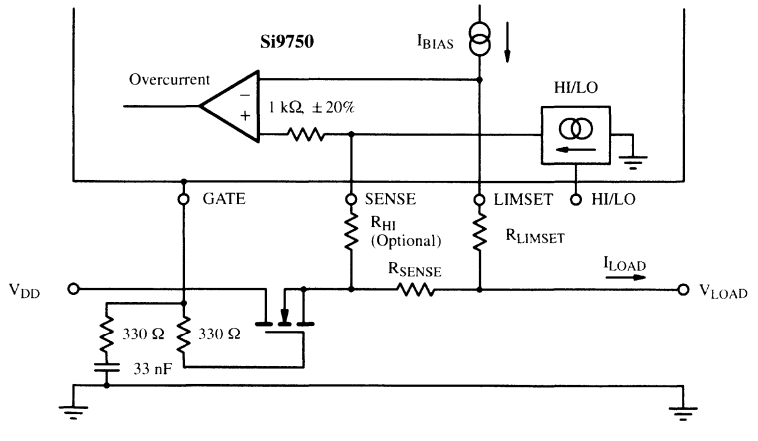


Figure 1.

Functional Description (Cont'd)

di/dt Limiting On Hot and Cold Insertion (GATE pin)

The GATE pin provides a constant current source that is used to control the rate of rise of the gate of the MOSFET, and hence to control the di/dt of the load and source current. The equation that governs the gate current is:

$$I_{SOURCE} = 1.25\ V \times \frac{12}{R_{BIAS}} = 1.2\ mA \quad (4)$$

(for R_{BIAS} = 12.5 kΩ)

Typically, a 33-nF capacitor should be connected from the GATE pin to ground. If a large I_{SOURCE} is needed for high di/dt, a 330-Ω resistor in series with C_{GATE} may be necessary to prevent oscillation. In the case that V_{DD} > 6 V, a resistor of approximately 330 Ω is also recommended in series with the gate. (Figure 1.)

Reference Bias Current (R_{BIAS} pin)

This pin sets the internal current used by R_{LIMSET} to determine all the current limit points. Typically R_{BIAS} = 12.5 kΩ which sets a 20-µA bias current. The equation which relates R_{BIAS} to I_{BIAS} is:

$$I_{BIAS} = \frac{1.25\ V}{5 \times R_{BIAS}} = 20\ \mu A \quad (5)$$

(for R_{BIAS} = 12.5 kΩ)

Power on Reset (POR) (V_{DD} pin)

This function monitors the voltage on the V_{DD} pin and signals the system if all input voltage requirements have been met. At turn-on when V_{DD} > 2.7 V ± 200 mV, a POR signal is generated for a duration of 100 µs. After this point the system is released into operation. If V_{DD} falls below 2.7 V ± 200 mV, a second POR signal will be generated. If two POR signals are detected, this indicates that the source for V_{DD} is not capable of supplying the load current. The IC then turns off the MOSFET and initiates its retry period, hence fully protecting the MOSFET from an over-power condition.

Boost Converter (COIL, BOOST pins)

The boost converter generates the gate drive for the external n-channel MOSFET. This is limited to typically V_{DD} + 11 V. The boost inductor should typically be 100 µH, <3.5 Ω, >180 mA dc, and the boost capacitor should be 100 nF.

Logic Control ($\overline{STATUS}$, $\overline{ENABLE}$, $\overline{RESET}$, V_{RST} and C_{RST} pins)

$\overline{STATUS}$. The status monitor detects when the load voltage is 90% of input voltage, V_{LOAD} > 0.9 x V_{DD}. This pin is an open-drain NMOS output, capable of sinking 200 µA at V_{OL} = 0.4 V. If this pin is used in conjunction with the $\overline{ENABLE}$ of another unit, power supply sequencing (or daisy-chaining) is easily implemented.

$\overline{ENABLE}$. This CMOS logic compatible input serves as the on/off control pin. This pin has 40-µA minimum pull-up to V_{DD}.

$\overline{RESET}$ (V_{RST}, C_{RST}, $\overline{RESET}$ pins). This is a standard implementation of the microprocessor reset function. A comparator looks at the voltage on V_{RST} pin and compares it with 1.25 V. This function is programmable by using an external voltage divider. When V_{RST} is higher than 1.25 V, the reset signal is delayed by the C_{RST} pin, defined by Equation (6) and then goes high. (Figure 8.)

$$\text{Reset delay } t_{RSTD} \approx 10^4 \times C_{RST} \quad (6)$$

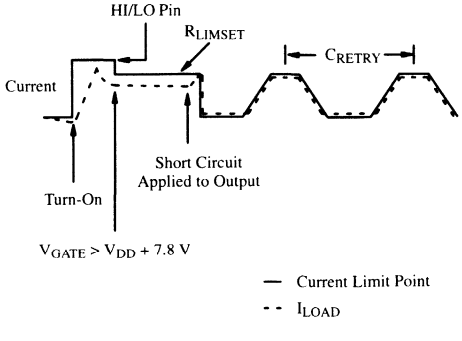
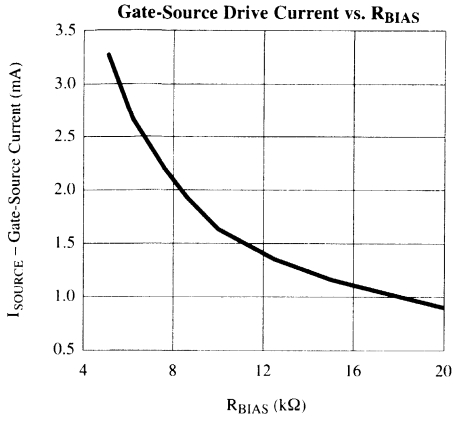


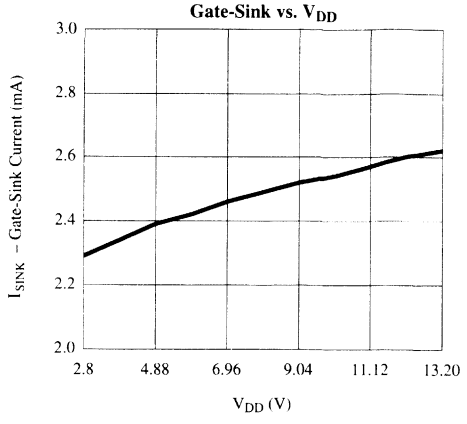
Figure 2. Typical Operation Under Start-up Condition With An Overcurrent Fault Applied to the Output

Typical Characteristics (25°C Unless Noted)

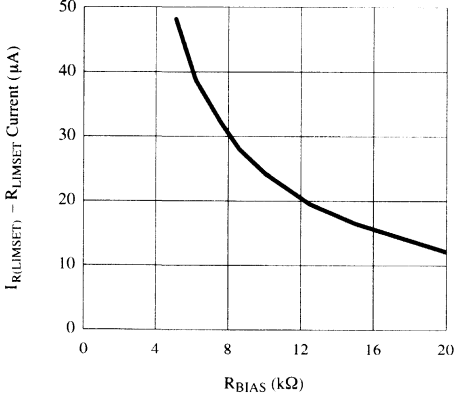
Gate-Source Drive Current vs. R_{BIAS}



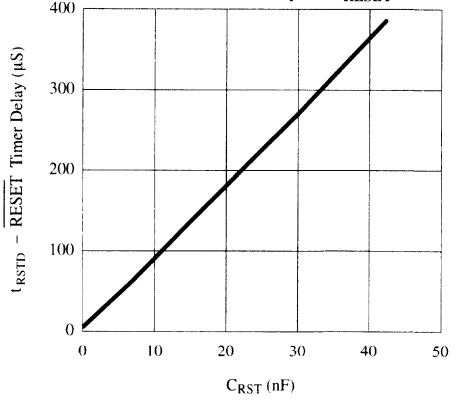
Gate-Sink vs. V_{DD}



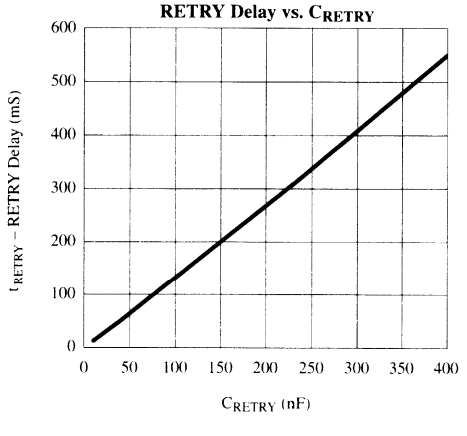
R_{LIMSET} Current vs. R_{BIAS}



$\overline{\text{RESET}}$ Timer Delay vs. C_{RESET}



RETRY Delay vs. C_{RETRY}



Switching Time Test Circuits

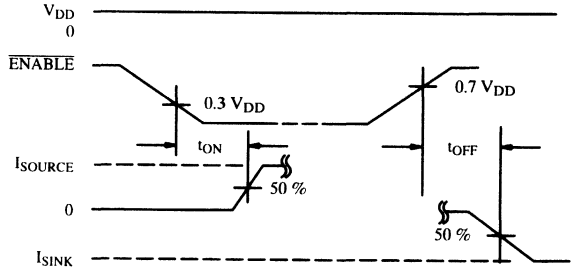


Figure 3. Normal-Mode Operation

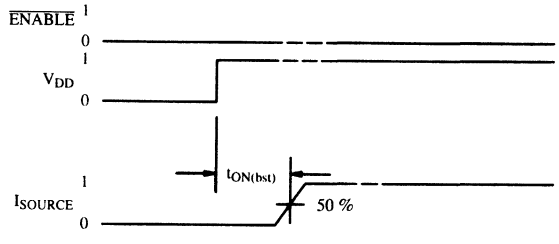


Figure 4. Timing Definition with $\overline{\text{ENABLE}}$ Already On

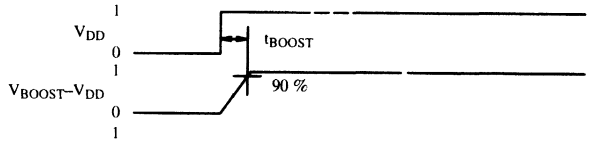


Figure 5. Start of Boost Converter

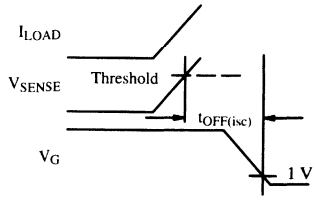


Figure 6. First Short Circuit

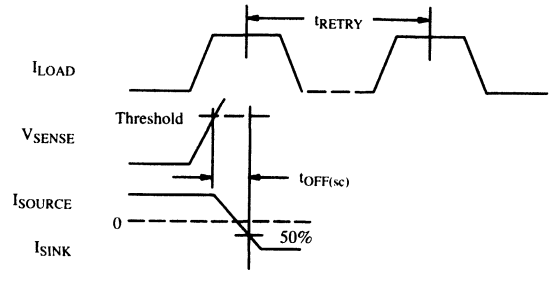
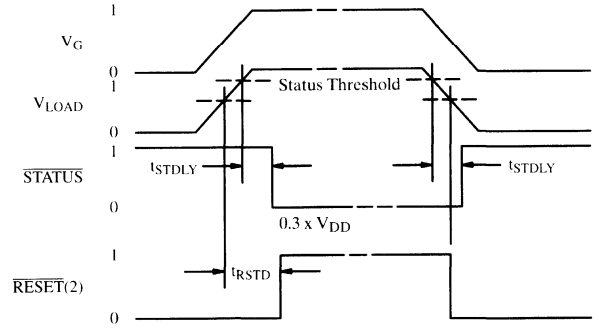


Figure 7. Relaxation-Mode Current Limit

Switching Time Test Circuits



(2) With reset input divider correctly set, monitoring V_{LOAD}

Figure 8. $\overline{\text{STATUS}}$ and $\overline{\text{RESET}}$

Motor Control Selector Guide

Part Number	Function	Supply Voltage	Output Drive Capacity	Input Drive Requirements	Features	Package	Protection	Page Number
Si9600[a]	Dual H-Bridge Controller/ 4 Half-Bridges Controller	7 – 40	Drives 8 N-Ch MOSFETs	TTL/CMOS	Current of Voltage Mode, Serial Bus Control, Diagnostics	SQFP-48	Short Circuit, Under Voltage, Temperature	3-133
Si9910	High Voltage MOSFET Driver	11 – 16 for Driver	Drives 1 N-Ch MOSFET	12-V Logic	dv/dt, di/dt Control	DIP-8, SO-8	Over Current, Under Voltage	3-1
Si9961	Voice Coil Motor Controller	12	1 A	Analog	Linear Current Mode	SOIC-24 Widebody	Under Voltage	3-58
Si9976	Half-Bridge Driver	20 – 40	Drives 2 N-Ch MOSFETs	TTL/CMOS	High-Side Bootstrap	SO-14	Short Circuit, Under Voltage	3-16
Si9978[a]	H-Bridge Driver/Dual $^1/_2$ H-Bridge Driver	20 – 40	Drives 4 N-Ch MOSFETs	TTL/CMOS	PWM, Brake, High-Side Bootstrap	SO-24 Widebody	Over Current, Under Voltage	3-29
Si9979[a]	3-Phase Brushless Motor Controller	20 – 40	Drives 6 N-Ch MOSFETs	TTL/CMOS	PWM 60° and 120° Hall Sensor Commutation, High-Side Bootstrap	SQFP-48	Over Current Under Voltage	3-42
Si9986	Buffered H-Bridge	3.8 – 13.2	1 A	TTL/CMOS	PWM, Saturated	SO-8	Shoot Through	3-67
Si9990	HDD VCM/Spindle Controller	5	1.2-A Spindle, 0.5-A VCM	TTL/CMOS Analog	Current Mode PWM Spindle, Current Mode Analog VCM, Auto Head Retract	SQFP-64	Over Temp, Under Voltage	3-74
Si9993[a]	HDD VCM/Spindle Controller	12	Spindle Drives 3 N- and 3 P-Ch MOSFETS VCM Drives 2 N- and 2 P-Ch MOSFETS	TTL/CMOS Analog	Current Mode PWM Spindle, Current Mode PWM or Analog, VCM, Auto Head Retract	SQFP-64	Over Temp, Under Voltage	3-107

Notes
a. Demo Board Available

Adaptive Power MOSFET Driver[b]

Features

- dv/dt and di/dt Control
- Undervoltage Protection
- Short-Circuit Protection
- t_{rr} Shoot-Through Current Limiting
- Low Quiescent Current
- CMOS Compatible Inputs
- Compatible with Wide Range of MOSFET Devices
- Bootstrap and Charge Pump Compatible (High-Side Drive)

Description

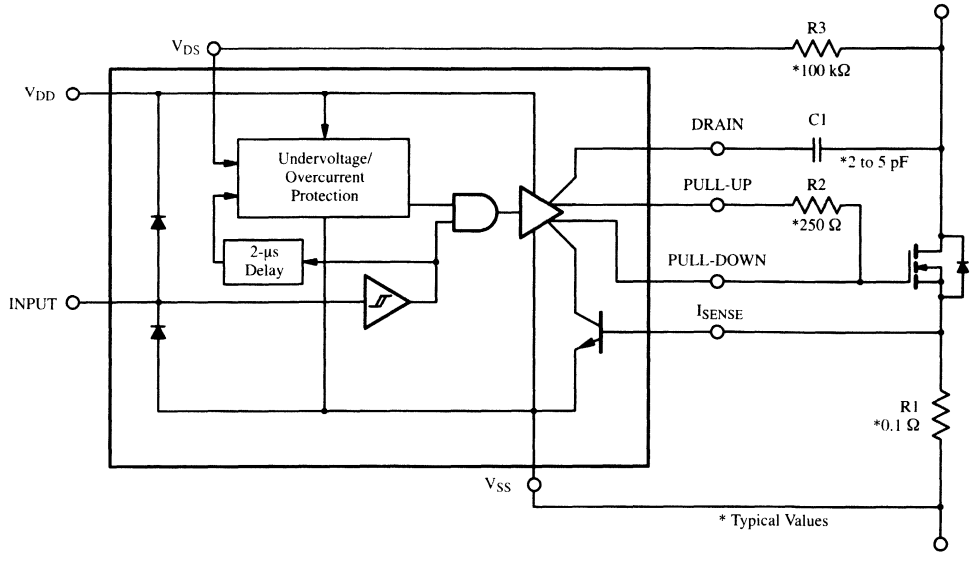
The Si9910 Power MOSFET driver provides optimized gate drive signals, protection circuitry and logic level interface. Very low quiescent current is provided by a CMOS buffer and a high-current emitter-follower output stage. This efficiency allows operation in high-voltage bridge applications with "bootstrap" or "charge-pump" floating power supply techniques.

The non-inverting output configuration minimizes current drain for an n-channel "on" state. The logic input is internally diode clamped to allow simple pull-down in high-side drives.

Fault protection circuitry senses an undervoltage or output short-circuit condition and disables the power MOSFET. Addition of one external resistor limits maximum di/dt of the external Power MOSFET. A fast feedback circuit may be used to limit shoot-through current during t_{rr} (diode reverse recovery time) in a bridge configuration.

The Si9910 is available in 8-pin plastic DIP and SOIC packages, and are specified over the industrial, D suffix (–40 to 85°C) temperature range.

Functional Block Diagram



Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70009. Applications information may also be obtained via FaxBack, request document #70579.

b. Patent Number 484116.

Absolute Maximum Ratings

Voltages Referenced to V_{SS} Pin
V_{DD} Supply Range ..... –0.3 V to 18 V
Pin 1, 4, 5, 7, 8 ..... –0.3 V to V_{DD} + 0.3 V
Pin 2 ..... –0.7 V to V_{DD} + 0.3 V
Input Current ..... ± 20 mA
Peak Current (I_{pk}) ..... 1 A
Storage Temperature ..... –65 to 150°C
Operating Temperature ..... –40 to 85°C
Junction Temperature (T_J) ..... 150°C
Power Dissipation (Package)[a]
8-Pin SOIC (Y Suffix)[b] ..... 700 mW
8-Pin Plastic DIP (J Suffix)[b] ..... 700 mW

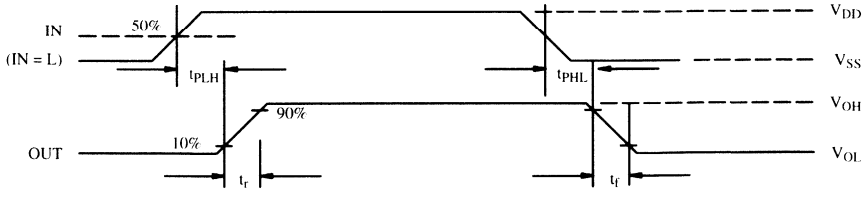
Notes
a. Device mounted with all leads soldered or welded to PC board.
b. Derate 5.6 mW/°C above 25°C.

Specifications[a]

Parameter	Symbol	Test Conditions Unless Otherwise Specified V_{DD} 10.8 V to 16.5 V T_A = OperatingTemperature Range	Limits Min[c]	Limits Typ[b]	Limits Max[c]	Unit
Input						
High Level Input Voltage	V_{IH}		0.70 x V_{DD}	7.4		V
Low Level Input Voltage	V_{IL}			6.0	0.35 x V_{DD}	V
Input Voltage Hysteresis	V_h		0.90	2.0	3.0	V
High Level Input Current	I_{IH}	V_{IN} = V_{DD}			± 1	µA
Low Level Input Current	I_{IL}	V_{IN} = 0 V			± 1	µA
Output						
High Level Output Voltage	V_{OH}	I_{OH} = –200 mA	V_{DD} –3	10.7		V
Low Level Output Voltage	V_{OL}	I_{OL} = 200 mA		1.3	3	V
Undervoltage Lockout	V_{UVLO}		8.3	9.2	10.6	V
I_{SENSE} Pin Threshold	V_{TH}	Max I_S = 2 mA, Input High 100 mV Change on Drain	0.5	0.66	0.8	V
Voltage Drain-Source Maximum	V_{DS}	Input High	8.3	9.1	10.2	V
Input Current for V_{DS} Input	I_{VDS}			12	20.0	µA
Peak Output Source Current	I_{OS+}			1		A
Peak Output Sink Current	I_{OS-}			–1		A
Supply						
Supply Range	V_{DD}		10.8		16.5	V
Supply Current	I_{DD1}	Output High, No Load		0.1	1	µA
	I_{DD2}	Output Low, No Load		100	500	µA
Dynamic						
Propagation Delay Time Low to High Level	t_{PLH}	C_L = 2000 pF		120		ns
Propagation Delay Time High to Low Level	t_{PHL}			135		ns
Rise Time	t_r			50		ns
Fall Time	t_f			35		ns
Overcurrent Sense Delay (V_{DS})	t_{DS}			1		µS
Input Capacitance	C_{in}			5		pF

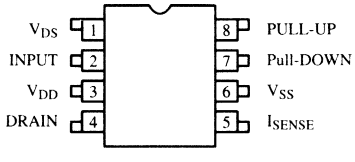
Notes
a. Refer to PROCESS OPTION FLOWCHART for additional information.
b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum.

AC Testing Conditions



Pin Configurations

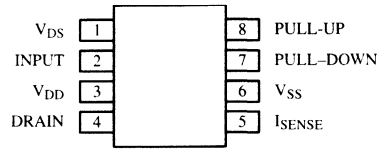
PDIP-8



Top View

Order Number:
Si9910DJ

SO-8



Top View

Order Number:
Si9910DY

Pin Description

Pin 1: V_{DS}

Pin 1 or V_{DS} is a sense input for the maximum source-drain voltage limit. Two microseconds after a high transition on input pin 2, an internal timer enables the $V_{DS(max)}$ sense circuitry. A catastrophic overcurrent condition, excessive on-resistance, or insufficient gate-drive voltage can be sensed by limiting the maximum voltage drop across the power MOSFET. An external resistor (R3) is required to protect pin 1 from overvoltage during the MOSFET "off" condition. Exceeding $V_{DS(max)}$ latches the Si9910 "off." Drive is re-enabled on the next positive- going input on pin 2. If pin 1 is not used, it must be connected to pin 6 (V_{SS}).

Pin 2: INPUT

A non-inverting, Schmidt trigger input controls the state of the MOSFET gate-drive outputs and enables the protection logic. When the input is low ($\leq V_{IL}$), V_{DD} is monitored for an undervoltage condition (insufficiently charged bootstrap capacitor). If an undervoltage ($\leq V_{DD(min)}$) condition exists, the driver will ignore a turn-on input signal. An undervoltage ($\leq V_{DD(min)}$) condition during an "on" state will not be sensed.

Pin 3: V_{DD}

V_{DD} supplies power for the driver's internal circuitry and charging current for the power MOSFET's gate capacitance. The Si9910 minimizes the internal I_{DD} in the "on" state (gate-drive outputs high) allowing a "floating" power supply to be provided by charge pump or bootstrap techniques.

Pin 4: DRAIN

Drain is an analog input to the internal dv/dt limiting circuitry. An external capacitor (C1) must be used to protect the input from exposure to the high-voltage ("off" state) drain and to set the power MOSFET's maximum rate of dv/dt. If dv/dt feedback is not used, pin 4 must be left open.

Pin Description (Cont'd)

Pin 5: I_{SENSE}

I_{SENSE} in combination with an external resistor (R_1) protects the power MOSFET from potentially catastrophic peak currents. I_{SENSE} is an analog feedback that limits current during the power MOSFET's transition to an "on" state. It is intended to protect power MOSFETs (in a half-bridge arrangement) from "shoot-through" current, resulting from excess di/dt and t_{rr} of flyback diodes or from logic timing overlap. An 0.8-V drop across (R1) should indicate a current level that is approximately four times the maximum allowable load current. When the I_{SENSE} input is not used, it should be tied to pin 6 (V_{SS}).

Pin 6: V_{SS}

V_{SS} is the driver's ground return pin. The applications diagram illustrates the connection of V_{SS} for source-referenced "floating" applications (half-bridge, high-side) and ground-referenced applications (half-bridge, low-side).

Pin 7: PULL-DOWN
Pin 8: PULL-UP

Pull-up and pull-down outputs collectively provide the power MOSFET gate with charging and discharging currents. Turn "on" or "off" di/dt can be limited by adding resistance (R_2) in series with the appropriate output.

Applications

"Floating" High-Side Drive Applications

As demonstrated in Figure 1, the Si9910 is intended for use as both a ground-referenced gate driver and as a "high-side" or source-referenced gate driver in half-bridge applications. Several features of the Si9910 permit its use in half-bridge high-side drive applications.

A simple and inexpensive method of isolating a floating supply to power the Si9910 in high-side driver applications had to be provided. Therefore, the Si9910 was designed to be compatible with two of the most commonly used floating supply techniques: the bootstrap and the charge pump. Both of these techniques have limitations when used alone. A properly designed bootstrap circuit can provide low-impedance drive which minimizes transition losses and the charge pump circuit provides static operation.

The Si9910 is configured to take advantage of either floating supply technique if the application is not sensitive to their particular limitations, or both techniques if switching losses must be minimized and static operation is necessary. The schematic above illustrates both the charge pump and bootstrap circuits used in conjunction with an Si9910 in a high-side driver application.

Input signal level shifting is accomplished with a passive pull-up (R4) and the Siliconix VN50300 (500-V/300-Ω) MOSFET for pull-down in applications below 500 V. Complete specifications for the VN50300 can be found in the Siliconix Low-Power Discretes Data Book. One of the VN50300's most important features in this application is its extremely low C_{oss} (output or drain) capacitance. C_{oss} (typically 5 pF), plus the Si9910's input capacitance (also typically 5 pF) plus any stray board capacitance. Total node capacitance defines the value of R4 needed to guarantee an input transition rate which safely exceeds the maximum dv/dt rate of the output half-bridge. Another feature of the VN50300 is its inherently low saturation current. Using level-shift devices with higher current capabilities may necessitate the addition of current-limiting components such as R5.

Bootstrap Undervoltage Lockout

When using a bootstrap capacitor as a high-side floating supply, care must be taken to ensure time is available to recharge the bootstrap capacitor prior to turn-on of the high-side MOSFET. As a catastrophic protection against abnormal conditions such as start-up, loss of power, etc., an internal voltage monitor has been included which monitors the bootstrap voltage when the Si9910 is in the low state. The Si9910 will not respond to a high input signal until the voltage on the bootstrap capacitor is sufficient to fully enhance the power MOSFET gate. For more details, please refer to Application Note AN705, which may be obtained via FaxBack, request document #8705.

Applications (Cont'd)

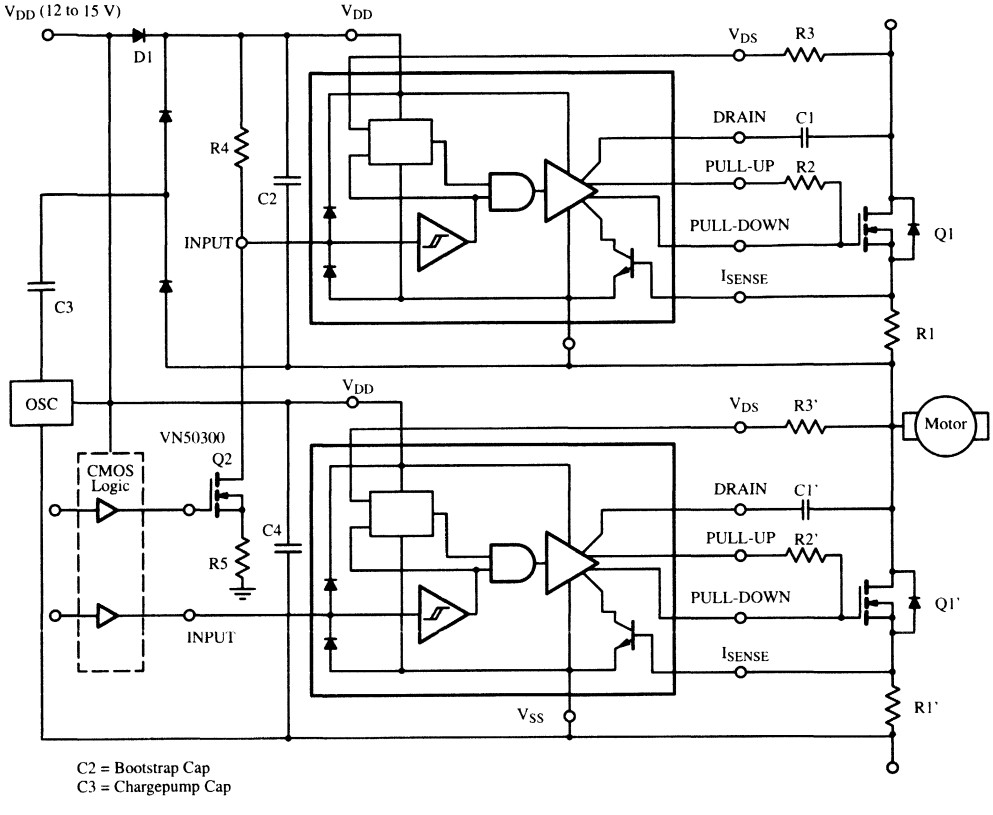


Figure 1. High-Voltage Half-Bridge with Si9910 Drivers

Si9910 Adaptive Power MOSFET Driver Improves Performance in High-Voltage Half-Bridge Applications

Jim Harnden

The Si9910 is the first of a new generation of "adaptive" power MOSFET gate drivers. These adaptive drivers provide protection for the power MOSFET switching element while allowing direct control of high-voltage switching from logic signals. To achieve this protection, the Si9910 monitors the power MOSFET's operating conditions through feedback loops and alters its output characteristics.

The Si9910 adaptive driver allows the system designer to take full advantage of the increased performance and efficiency of power MOSFETs. Previous gate-drive techniques required designing a system for safe operation under worst-case conditions, even those which occur infrequently. Thus, these systems operated most of the time under less than optimum conditions with considerable performance and efficiency penalties. The Si9910, however, prevents power MOSFET destruction under worst-case operating conditions without compromising system performance and efficiency during normal operation.

Si9910 Circuit Description

The Si9910 is a single-channel, non-inverting CMOS driver with a low-impedance, emitter-follower output and a Schmidt trigger input (see Figure 1). To take full advantage of the efficiency offered by the power MOSFET's capacitive input impedance characteristic, the Si9910 was designed to have extremely low quiescent current and low output gate-drive impedance.

New "power IC" processes incorporating CMOS, DMOS, and bipolar device technologies are employed to optimize the Si9910 driver characteristics. The driver's CMOS logic section requires a maximum quiescent current of 1 µA (with the output high and the power MOSFET turned on), while the emitter-follower output stage is capable of delivering 1 A of peak current to quickly charge and discharge MOSFET gate capacitance. Using a bipolar emitter-follower output eliminates shoot-through and quiescent bias current losses in the low-impedance output stage.

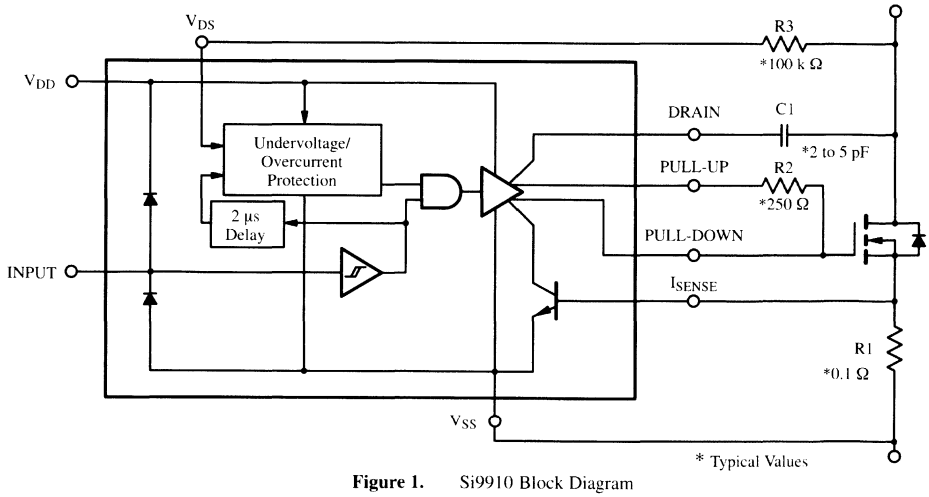


Figure 1. Si9910 Block Diagram

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High-Performance, High-Voltage Motor Drives

One potently damaging characteristic of a high-voltage motor-drive circuit is inductive flyback energy. Damaging voltages can result when inductor drive current is interrupted, unless some method is used to clamp the voltage and "free wheel" the inductive flyback energy (see Figure 2). For example, in unipolar motor-drive techniques, the flyback voltage is often clamped with a discrete diode to the motor supply or with a Zener diode to ground. One benefit that power MOSFETs offer is their intrinsic diodes which can serve as reliable and efficient voltage clamps.

Most high-performance motor drives require bipolar drive techniques (not to be confused with bipolar semiconductor technology). The power switching arrangement most commonly used is the half-bridge configuration. In a half-bridge, each motor winding is connected to a common node between switching devices that can connect it to either the motor supply voltage or to the motor supply return. In half-bridge drives, the MOSFET's intrinsic diode characteristics (especially reverse recovery time, t_{rr}) become very important[1] any time a motor winding's drive is interrupted and then re-enabled in the same path while flyback current is recirculating in an opposing clamp diode.

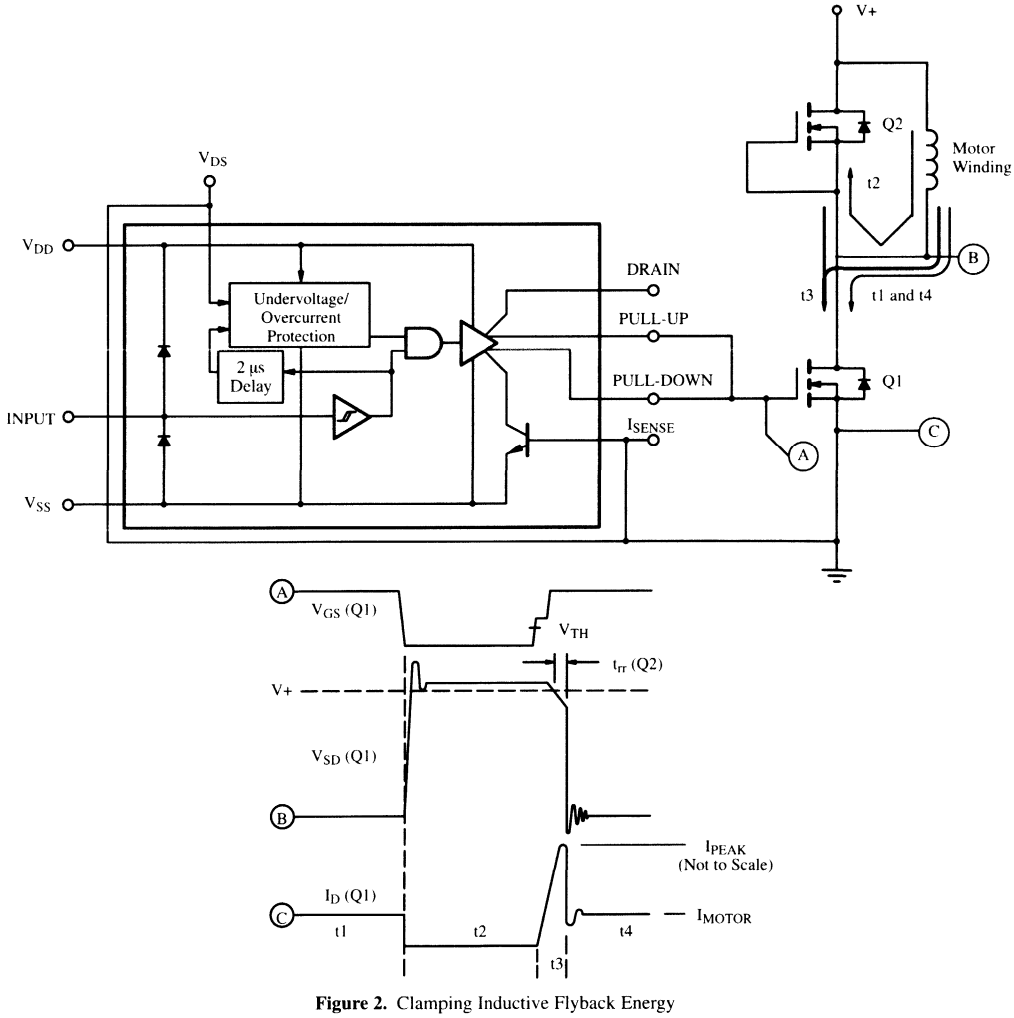


Figure 2. Clamping Inductive Flyback Energy

Protecting the Power MOSFET in Motor-Drive Applications

The half-bridge configuration shown in Figure 2 will be used throughout this article to demonstrate the problems associated with power MOSFET protection. The gate of the upper power MOSFET is shorted to its source so the MOSFET functions only as a clamp diode. The motor winding (inductive load) is shorted to V_{motor} at one end and switched by the lower power MOSFET at the other end. In an actual motor-drive circuit, both power MOSFETs in the half-bridge would be active and the other end of the motor's winding would be tied to another half-bridge. Depending on the modulation technique employed, any of the half-bridge power MOSFETs can be used to clamp flyback energy and can be exposed to reverse-recovery current spikes by being turned on in opposition to a conducting diode. The problems demonstrated by this simplified circuit are indicative of those exhibited by either the upper or lower MOSFETs in the half-bridge.

As shown in Figure 2, during time t1 the lower MOSFET (Q1) is turned on and load current is conducted through the inductor to ground. At the leading edge of time t2, Q1 is turned off and flyback current from the inductor recirculates through the intrinsic diode in MOSFET Q2. Shoot-through current occurs during time t3 when Q1 is switched back on. As Q1 turns on, it begins to conduct load current as well as reverse current through the diode of Q2. When enough reverse current has been conducted to sweep out the minority carriers in the diode of Q2, it begins to recover. Duration of the shoot-through current spike is dependent on t_{rr} (which is, in part, a function of the diode's previous forward current and the forced di/dt during recovery). The magnitude of the current spike depends on the gate-drive voltage and forward transfer conductance (g_{fs}) of Q1 at the time of Q2 diode recovery and can be many times greater than the motor current.

Limiting the MOSFET's di/dt

As mentioned above, the current spike duration is dependent on the power MOSFET t_{rr} which is, in turn, a function of the diode forward current (motor flyback current) and di/dt during the forced recovery. Most commercial power MOSFETs have t_{rr} ratings specified with a recovery di/dt of 100 A/µs. Recovering at higher or lower di/dt rates will not change the amount of charge which must be "swept" out of the bipolar junction before recovery. Recovering at a higher di/dt rate results in higher peak currents of less duration. The only MOSFET failure mode *directly* triggered by excessive di/dt arises when it results in a peak current that is sufficient to force the MOSFET outside of its safe operating area (SOA). Until now, limiting di/dt has often been a technique used to limit the maximum rate of dv/dt (and its associated failure modes of commutating dv/dt and SOA).[2]

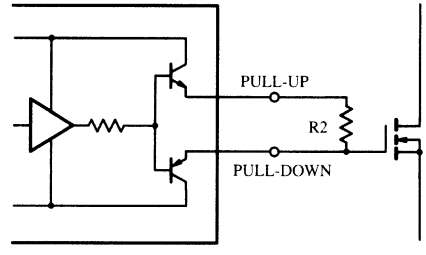


Figure 3a. Simplified "Split" Emitter-Follower Output Circuit

[1] Addressing this issue in high-voltage (500 V) applications is a new line of MOSPOWER transistors from Siliconix with intrinsic diode recovery times rivaling discrete fast-recovery diodes. However, even these fast-recovery diodes don't solve all the problems associated with flyback energy and diode recovery. Power MOSFETs are capable of extremely fast voltage transitions and no commercially available 500-V diode (discrete or intrinsic) will be fast enough to allow the system switching losses to be absolutely minimized without regard to potentially damaging shoot-through currents.

[2] To recap, commutating or recovery dv/dt is proportional to the peak current level at the point of recovery. Peak recovery current is directly related to di/dt and t_{rr}. And a power MOSFET's t_{rr} increases as the diode's forward current increases, which is a direct function of the motor's winding current.

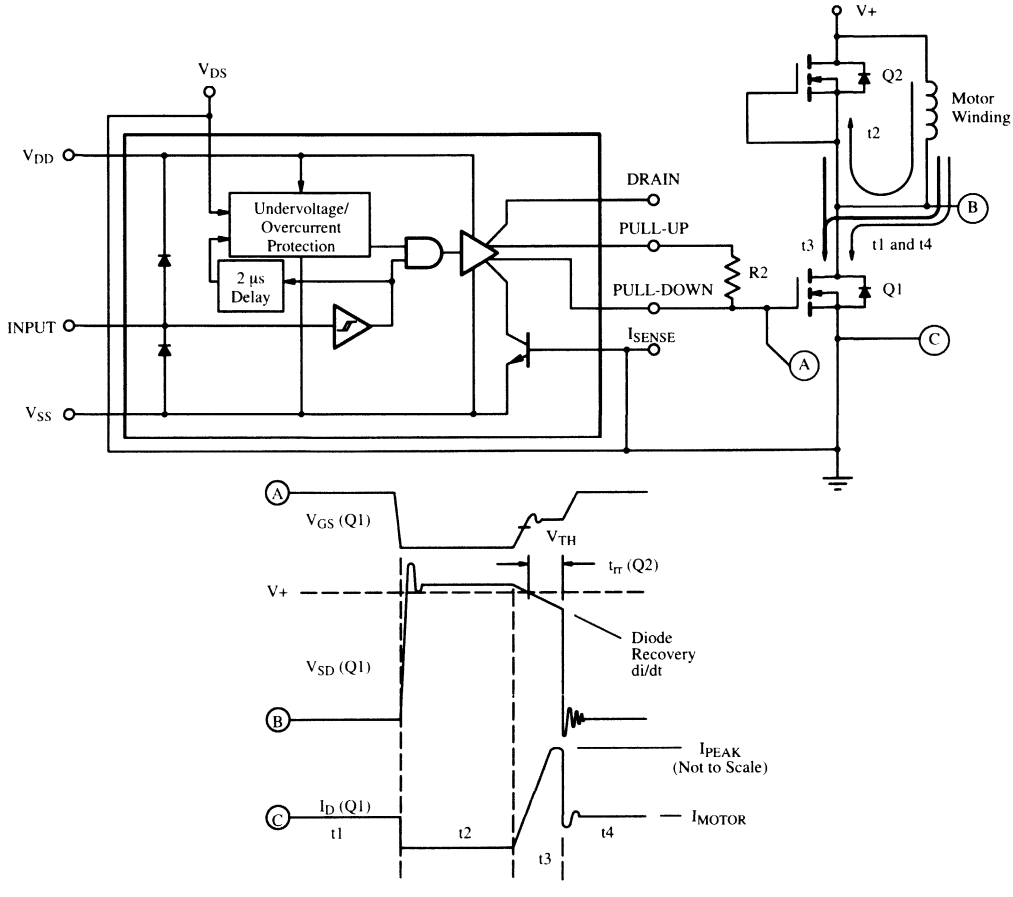


Figure 3b. Controlling di/dt via MOSFET Gate Drive Impedance

In a half-bridge that uses the adaptive controls of the Si9910, both the maximum recovery current and associated commutating dv/dt, which only occur when the system is delivering maximum motor current, are directly controlled.

The "split" emitter-follower output (Figure 3a) of the Si9910 allows the addition of a single external resistor to set the maximum rate of system di/dt during MOSFET turn-on (Figure 3b). This is a system parameter that is independently set and is not effected by variations in load current or operating conditions. With power MOSFETs, di/dt is a function of total gate capacitance during an "on" transition and the gate driver's pull-up resistance. Once a gate drive impedance and gate capacitance is established, di/dt will vary only as a result of dv/dt variations which reduce the amount of charge coupled to the MOSFET gate through the device's reverse transfer capacitance (Miller feedback capacitance).

As the value of gate-drive resistance (R2 in Figure 3b) is increased, the dv_{GS}/dt of Q1 (during time t3) is reduced. The MOSFET's conducted current is a direct function of its gate voltage and transconductance (g_{fs}). Therefore, restricting dv_{GS}/dt directly reduces di/dt.

With the Si9910 adaptive MOSFET driver, the pull-up gate-drive resistance (R2) can be calculated based on a safe system di/dt level, without regard to peak current or dv/dt protection of the power MOSFETs.

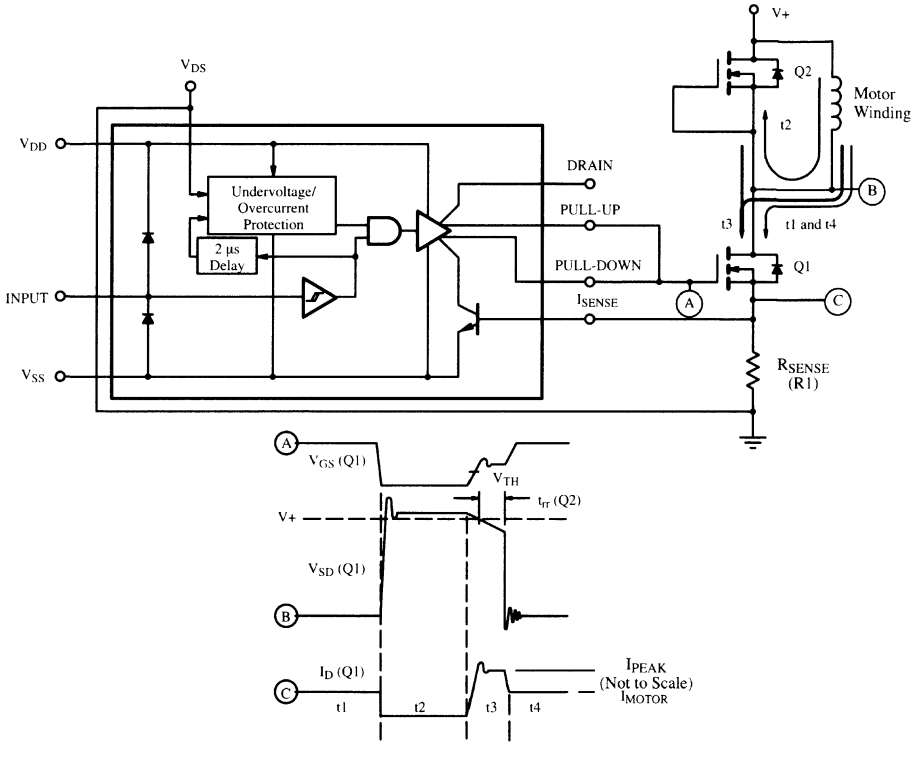


Figure 4. Limiting Peak Current

Limiting the t_{rr}-Induced Shoot-Through Current Level

The Si9910 I_{SENSE} input can be used in conjunction with a very low-value external sense resistor to directly limit the maximum peak current (Figure 4). Figure 5 illustrates a simplified schematic of the Si9910's peak current limiting circuit. When the voltage drop across the external sense resistor (R_{SENSE}) exceeds the V_{BE} of internal transistor Q3, it begins to turn-on, shunting further increases in voltage at the common base of the output emitter-follower and, therefore, the MOSFET's gate-drive voltage (during time t3 in Figure 4).

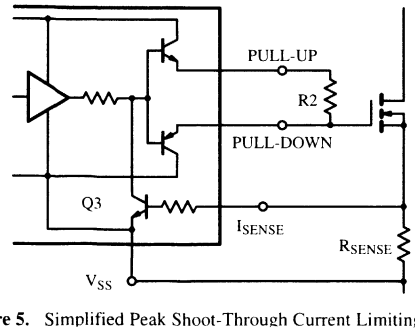


Figure 5. Simplified Peak Shoot-Through Current Limiting Circuit

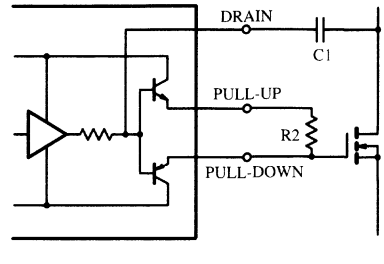


Figure 6. Simplified dv/dt Feedback Circuit

The value of external resistor R_{SENSE} should be calculated to limit the maximum shoot-through current level. The I_{SENSE} feedback is not intended to limit motor current since it restricts the MOSFET's dv_{GS}/dt, leaving the MOSFET in transition for a longer period of time. R_{SENSE} should be sized to limit current at a level approximately four times greater than the peak motor current.

$$R_{SENSE} = \frac{0.8\ V}{4 \times \text{Peak Motor Current}}$$

This transient current level is consistent with the power MOSFET's peak current rating which (in most commercially available power MOSFETs) is four times the continuous current rating.

Directly Limiting the MOSFET's dv/dt

Figure 6 is a simplified schematic of the Si9910's feedback circuit used to sense and limit maximum half-bridge dv/dt. As the common base of the emitter-follower stage changes from a low to a high level, the output follows, turning the power MOSFET on. As the power MOSFET switches on, the voltage across its drain-source decreases rapidly. The rate of dv/dt will depend on all of the conditions described earlier that are associated with diode reverse recovery. When a switching transition occurs, it will couple charge through the external capacitor (C1) which decreases the rise time of the emitter-follower's common base and, in turn, limits the dv_{GS}/dt of the power MOSFET. In a typical motor-drive circuit, maximum dv/dt will only occur during worst-case motor current, which is a transient condition. This technique permits faster switching (and higher efficiency) during normal operation and provides dv/dt protection for the MOSFETs when it is required.

The drain input must be limited to low voltage, which requires connection to the MOSFET's drain via a capacitor capable of withstanding the full motor-drive voltage (Figure 7).

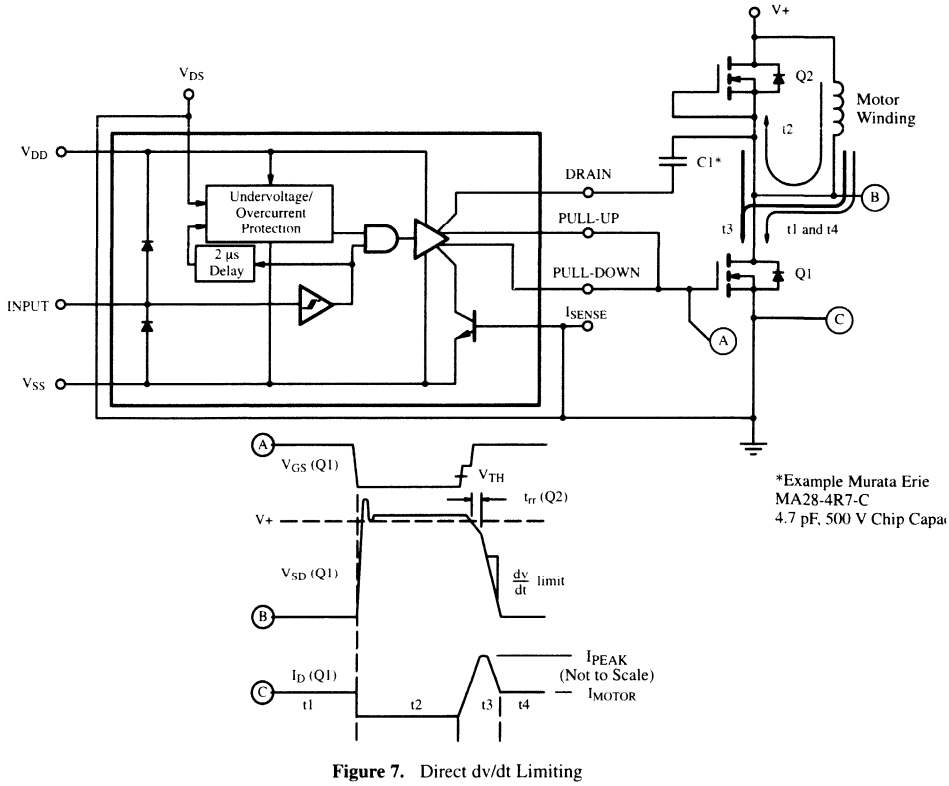
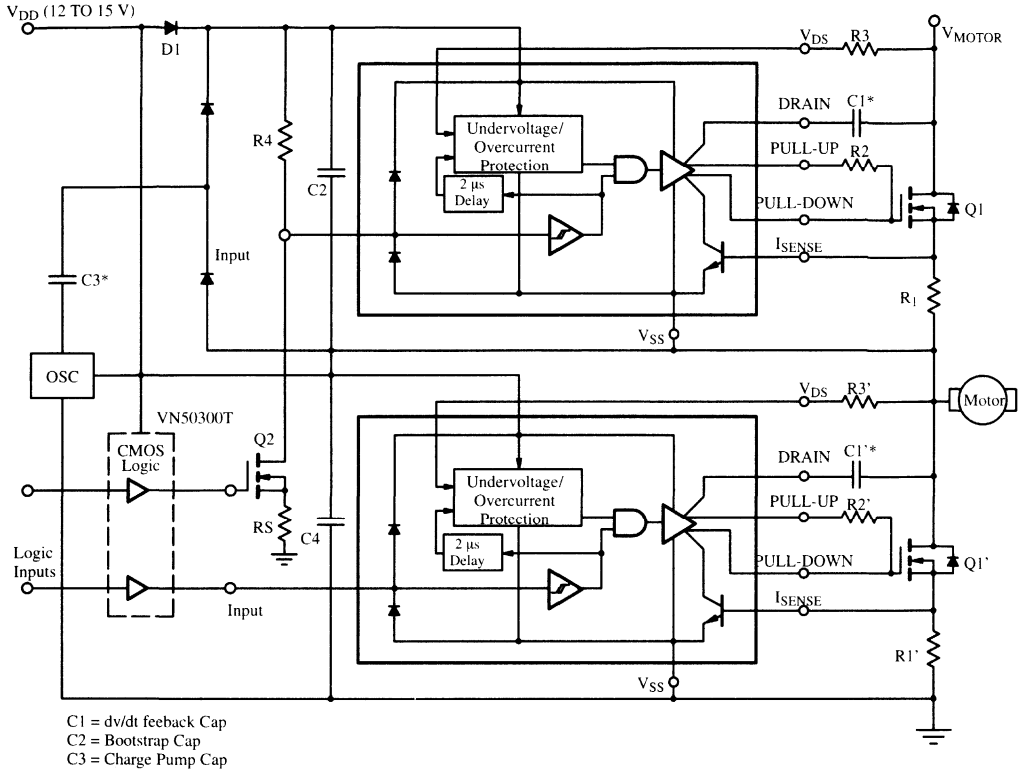


Figure 7. Direct dv/dt Limiting



C1 = dv/dt feeback Cap
C2 = Bootstrap Cap
C3 = Charge Pump Cap

*C1 – C3 0.3 to 1000 pF, 500 V, surface mount capacitors are available in a line of high Q porcelain ceramic capacitors from Murata.

Figure 8. High-Voltage Half-Bridge with Si9910 Drivers

"Floating" High-Side Drive Applications

As demonstrated in Figure 8, the Si9910 is intended for use as both a ground-referenced gate driver and as a "high-side" or source-referenced gate driver in half-bridge applications. Several features of the Si9910 facilitate its use in half-bridge high-side drive applications.

The Si9910 was designed to be compatible with two of the most commonly used floating supply techniques: the bootstrap and the charge pump. Both of these techniques have limitations when used alone. A properly designed bootstrap circuit can provide low-impedance drive which minimizes transition losses, but it does not provide static (100% duty-cycle) drive. Eventually the bootstrap capacitor's charge will be depleted by system leakages, resulting in reduced (potentially damaging) levels of gate-drive voltage. A charge pump circuit can provide static operation but usually yields increased gate-drive impedance, which ultimately results in slower transition rates and increased switching losses. As the charge pump capacitance is increased to provide faster transition rates, the oscillator circuit is subjected to higher peak currents in the presence of the dv/dt rates that exist in half-bridge motor drives. This limits the extent to which the charge pump capacitor can be increased.

The Si9910 is configured to take advantage of either floating supply technique, (if the application is not sensitive to their particular limitations), or a combination of both techniques (if switching losses must be minimized and static operation is necessary). Figure 8 illustrates both the charge pump and bootstrap circuits used in conjunction with an Si9910 in a high-side driver application.

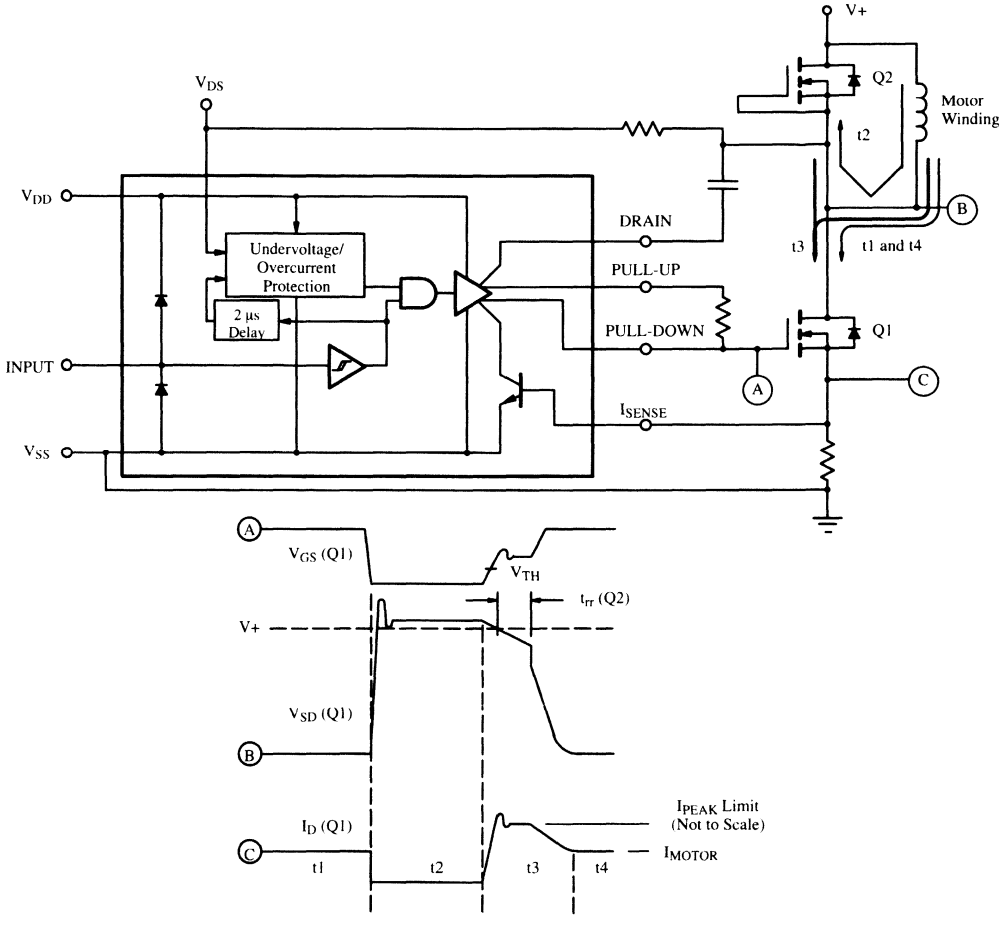


Figure 9. All Feedback Options Active

Bootstrap Undervoltage Lockout

When using a bootstrap capacitor as a high-side floating supply, sufficient time must be allowed to recharge the bootstrap capacitor prior to turn-on of the high-side MOSFET. As protection against catastrophic transient conditions such as start-up, loss of power, etc., an internal voltage monitor has been included which monitors the bootstrap voltage when the Si9910 is in the low state. The Si9910 will not respond to a high input signal until the voltage on the bootstrap capacitor is sufficient to fully enhance the power MOSFET gate.

Maximum V_{DS} Monitor

The Si9910 V_{DS} input monitors the source-drain voltage drop across the MOSFET in the "on" state. Excess V_{DS} can occur as a result of high on-resistance ($r_{DS(ON)}$) at increased temperature, insufficient gate enhancement voltage, or excessive current. Regardless of the cause, the effects can be catastrophic. The first priority of the Si9910 is to protect the power MOSFET. Therefore, a maximum V_{DS} monitor is enabled 2 µs after each positive-going input transition. Voltage exceeding the V_{DS} maximum (data sheet limit) will cause the gate driver to go to a low state and to wait for the next positive-going input command.

The V_{DS} pin is a low-voltage input which must be isolated from the high voltages at the power MOSFET's drain by an external resistor. The value of the external resistor is not critical to the operation of the maximum V_{DS} shutdown circuit. A 100-kΩ resistor is sufficient to isolate the high-voltage with minimum power losses and still drive the low capacitance input with tolerable response times.

Input Level Translation

Input logic signals must be level shifted to control the driver in the high-side of a half-bridge application. The circuit illustrated in Figure 8 uses a simple passive pull-up (R4) and a high-voltage, small-signal MOSFET (Q2) for level translation. The VN50300 was selected for its extremely low drain capacitance (1.8 pF typical). The drain capacitance of Q2 is important because of the direct effect it has on the value of R4.

The value of R4 should be sufficient to provide an RC time constant that is faster than the turn-on rate of Q1. The capacitance that must be driven is the total at the Si9910's input node (2 pF typical for the Si9910 plus 1.8 pF typical for the VN50300 plus any stray wiring and board capacitances).

R4 must also have a value that is high enough (relative to the on-resistance of Q2) to maintain a logic level of zero (3 V maximum) when the low-side device is turned on.

The minimum value of R4 necessary to achieve a safe RC time constant depends on the turn-on rate of Q1, which can be altered by adjusting the value of R2. (For most mid-sized MOSFETs [1000–3000 pF C_{iss}] typical values are 250 Ω for R2, 5 pF for the input-node capacitance, and 10 kΩ for R4.) Observing the half-bridge's positive-going output-voltage transition with an oscilloscope will reveal any "input-laging-output" imbalance as a sawtooth voltage waveform. Trying to observe the input-voltage transition directly is difficult since addition of any scope probe capacitance can significantly alter the node's switching characteristics.

Some applications will require current limiting of Q2. It is common, for instance, in brushless, three-phase motor drives to encounter a condition where both the high and low-side MOSFETs (Q1 and Q1') are off for some period during each cycle. During this time, for a particular phase, Q2 will be on, but since the lower output MOSFET is not on, the output voltage from the bridge is defined by the back EMF of the motor (which may be as much as 80 to 90% of V+ at maximum velocity). If Q2 is a VN50300, inherent protection results from the device's low saturation current capability (see the VN50300 characteristic curves in Siliconix Low Power Discretes Data Book). If level-shift devices that have higher-saturation current capability are substituted, measures may have to be implemented (such as series resistance in the source or drain of Q2) to protect the level-shift device and/or the input of the Si9910.

Flexible Feedback Options

Each of the feedback options — dv/dt limiting, peak current limiting and maximum V_{DS} — may be used separately or in any combination. Figure 9 shows all the external feedback options connected and the resulting voltage/current waveforms. If the designer chooses not to use the V_{DS} input to monitor maximum V_{DS}, it should be tied to V_{SS}. When the drain input is not in use, it must be left open. When the I_{SENSE} input is not in use, it should be shorted to V_{SS}.

Packaging Concept: Using Surface-Mount Si9910s with Power MOSFET Chips

Using surface-mount driver ICs, such as the Si9910DY shown in Figure 10, on a substrate with power MOSFET chips holds great promise for next-generation motor drives. The power MOSFET can be mounted directly on a substrate with good thermal transfer characteristics, thus solving the density and power dissipation problems commonly associated with motor controllers. Power MOSFETs are relatively easy to handle in die form and can be tested prior to packaging. Handling ICs in die form, however, presents problems which can be avoided with low-cost, compact surface-mount packages such as the Si9910DY.

Summary

The Si9910 introduces a new generation of "adaptive" power MOSFET gate drivers that use active feedback to protect the power MOSFET, while allowing logic-level control of high-voltage signals. The Si9910's first priority is to protect the power MOSFET that it drives.

When all of its protective options are enabled, the Si9910 is capable of controlling the power MOSFET dv/dt, di/dt, maximum peak current, minimum gate-drive voltage, and maximum source-drain voltage drop. The Si9910 allows the system designer to take full advantage of the increased performance and efficiency characteristics of power MOSFETs by designing the system with optimized switching losses and efficiency, while leaving worst-case system protection to the driver.

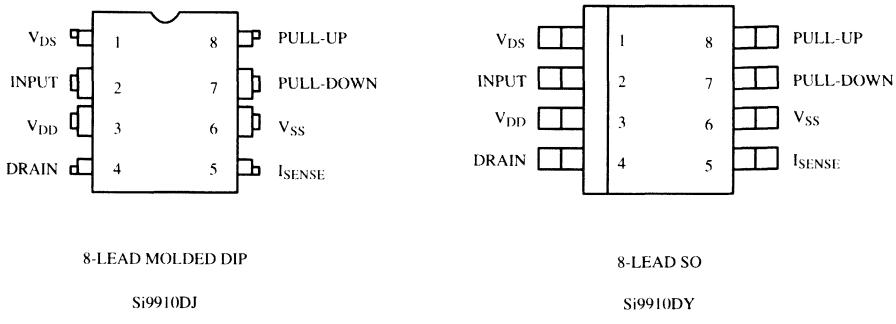


Figure 10. Si9910DY and Si9910DJ Package Pin-Outs

N-Channel Half-Bridge Driver

Features

- Single Input for High-Side and Low-Side MOSFETs
- 20- to 40-V Supply
- Static (dc) Operation
- Cross-Conduction Protected
- Undervoltage Lockout
- ESD and Short Circuit Protected
- Fault Feedback

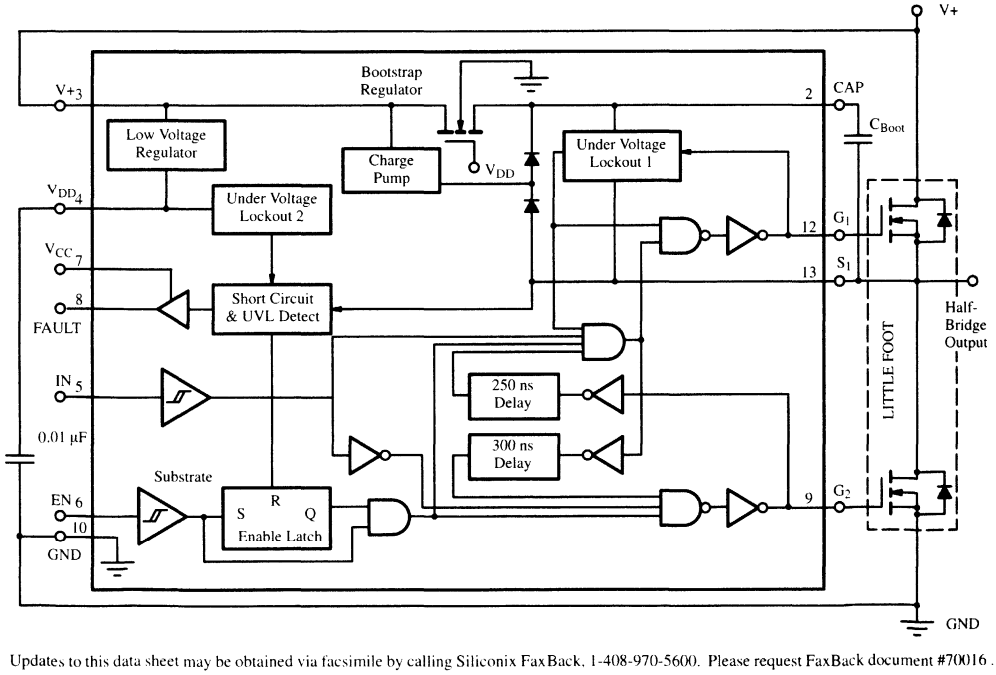
Applications

- Power Supplies
- Motor Drives
- Office Automation
- Computer Peripherals
- Industrial Controllers
- Robotics
- Medical Equipment

Description

The Si9976DY is an integrated driver for an n-channel MOSFET half-bridge. Schmitt trigger inputs provide logic signal compatibility and hysteresis for increased noise immunity. An internal low-voltage regulator allows the device to be powered directly from a system supply of 20 to 40 volts. Both half-bridge n-channel gates are driven directly with low-impedance outputs. Addition of one external capacitor allows an internal circuit to level shift both the power supply and logic signal for the half-bridge high-side n-channel gate drive. An internal charge pump replaces leakage current lost in the high-side driver circuit to provide "static" (dc) operation in any output condition. Protection features include an undervoltage lockout, cross-conduction prevention logic, and a short circuit monitor. The Si9976DY is available in the 14-pin SOIC (surface mount) package, specified to operate over the industrial (–40 to 85°C) temperature range.

Functional Block Diagram



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Absolute Maximum Ratings

Voltage on IN, EN (pins 5, 6)
with respect to ground ..... –0.3 to V_{DD} +0.3 V
Voltage on V_{CC} (pin 7) ..... –0.3 to +18 V
Voltage on V+, S1 (pins 3, 13) ..... –0.3 to +50 V
Voltage on CAP, G1[a] (pins 2, 12) ..... –0.3 to +60 V
Peak Output Current ..... 0.5 A
Operating Temperature (T_A) ..... –40 to 85°C
Storage Temperature ..... –50 to 150°C

Maximum Junction Temperature (T_J) ..... 125°C
Power Dissipation[b] ..... 1 W
Θ_{JA} ..... 100°C/W[b]

Notes
a. Internally generated voltage for reference only.
b. Derate 10 mW/°C above 25°C.
c. PC board mounted with no forced air flow.

Specifications[a]

Parameter	Symbol	Test Conditions UnlessOtherwise Specified V+ = 20 to 40 V T_A = Operating Temperature Range	Limits D Suffix –40 to 85°C Min[c]	Typ[b]	Max[c]	Unit
Input						
Input Voltage High (EN and IN)	V_{INH}		4.0			V
Input Voltage Low (EN and IN)	V_{INL}				1.0	
Input Hysteresis Voltage	V_H			0.5		
Input Current—Input Voltage High	I_{INH}	(EN and IN) V_{IN} = 15 V			1	µA
Input Current—Input Voltage Low	I_{INL}	(EN and IN) V_{IN} = 0 V	–1			
Output						
Output Voltage High, G1[d]	V_{OUTH}	S1 = V+, I_{OUT} = –10 mA	10	12		V
Output Voltage High, G2[e]		S1 = GND, I_{OUT} = –10 mA	12	15		
Output Voltage Low, G1 and G2	V_{OUTL}	S1 = GND, I_{OUT} = 60 mA		1.2	3	
Fault Output Voltage High	V_{OH}	V_{CC} = 4.5 V, I_{OUT} = –0.2 mA	3.5	4		
Fault Output Voltage Low	V_{OL}	V_{CC} = 4.5 V, I_{OUT} = 0.6 mA		0.3	1.0	
Undervoltage Lockout 1	UVL1			11		
Undervoltage Lockout 2	UVL2			14		
Capacitor Current	I_{CAP}	S1 = GND, V_{CAP} = 0 V			–10	mA
		S1 = GND, V_{CAP} = 9 V			–2	
Supply						
V+ Supply Range			20		40	V
V+ Supply Current	I+ (H)	G2 High, No Load		1.7	3.5	mA
	I+ (L)	G2 Low, No Load, S1 = GND		2	4.5	
V_{CC} Supply Range			4.5		16.5	V
V_{CC} Supply Current	I_{CC}	V_{CC} = 16.5 V			10	µA
V_{DD} Supply Voltage[f]	V_{DD}		15	16	17.5	V

Specifications[a]

Parameter	Symbol	Test Conditions UnlessOtherwise Specified V+ = 20 to 40 V T_A = Operating Temperature Range		Limits D Suffix –40 to 85°C Min[c]	Typ[b]	Max[c]	Unit
Dynamic							
Propogation Delay Time Low to High Level	t_{PLH}	50% IN to V_{OUT} = 5 V, C_L = 600 pF	G1		350		ns
			G2		400		
Propogation Delay Time High to Low Level	t_{PHL}		G1		150		
			G2		50		
Propogation Delay Time, Low to High Level, Enable-to-Fault Output		50% IN to FAULT = 2 V, S1 shorted to GND or V+			500		
Output Rise Time (G1, G2)	t_r	1 to 10 V, C_L = 600 pf			110		
Output Fall Time (G1, G2)	t_f	10 to 1 V, C_L = 600 pf			50		
Short Circuit Pulse Width	t_{SC}	50% to 50% of V_{OUT}			350		

Notes
a. Refer to PROCESS OPTION FLOWCHART for additional information.
b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum.
d. To supply the output current of 10 mA on a dc basis, an external 13-V supply must be connected between the CAP pin and the S1 pin with the negative terminal of the supply connected to S1. This is not needed in an actual application because output currents are supplied by the C_{BOOT} capacitor. Voltage specified with respect to V+.
e. For testing purposes, the 10-mA load current must be supplied by an external current source to the V_{DD} pin to avoid pulling down the V_{DD} supply.
f. Internally generated voltage for reference only.

Truth Table

EN	IN	Condition	FAULT OUTPUT	G1 OUT	G2 OUT
1	0	Normal Operation	0	Low	High
1	1	Normal Operation	0	High	Low
0	X	Disabled	X[a]	Low	Low
1	0	Load Shorted to V+	1[b]	Low	Low
1	1	Load Shorted to Ground	1[b]	Low	Low
1	1	Undervoltage on C_{BOOT}	0	Low	Low
1	0	Undervoltage on C_{BOOT}	0	Low	High
X	X	Undervoltage on V_{DD}[c]	1	Low	Low

Notes
a. FAULT output retains previous state until ENABLE rising edge.
b. Latch FAULT condition, reset by ENABLE rising edge.
c. V_{DD} is an internally generated low-voltage supply.

Pin Description

Pin 1

No connection.

Pin 2: CAP

Connection for the positive terminal of the bootstrap capacitor C_{BOOT}. A 0.01-µF C_{BOOT} capacitor can be used for most applications.

Pin 3: V+

This is the only external power supply required for the Si9976DY, and must be the same supply used to power the half-bridge it is driving. The Si9976DY powers it's low-voltage logic, low-side gate driver, and bootstrap/charge pump circuits from self-contained voltage regulators which require only a bootstrap capacitor on the CAP pin and a bypass capacitor on the V_{DD} pin.

No voltage sensing circuitry monitors V+ directly; however, the low-voltage, internally generated V_{DD} supply and the bootstrap voltage (which are derived from V+) are directly protected by undervoltage monitors.

Pin 4: V_{DD}

Connection to the internally generated low-voltage supply which must be bypassed to ground with a 0.01-µF capacitor.

Pin 5: IN

Logic input. A low level input turns off the high-side half-bridge MOSFET and, after an internally set dead time, turns the low-side half-bridge MOSFET on. A high input level has the opposite effect. The input is compatible with 5-, 12- or 15-V logic outputs.

Pin 6: EN

Enable input. A low EN input level prevents turn on of either half-bridge MOSFET. If the Si9976DY is internally disabled as a result of an output short-circuit condition, a low-to-high transition on EN is required to clear the fault and resume operation. The input logic levels are the same as IN.

Pin 7: V_{CC}

If the FAULT output is used, the V_{CC} pin must be connected to the logic supply voltage in order to set the high level of the FAULT output. If the FAULT output is not used, this pin may be left open with no effect on internal fault sensing or protection circuitry.

Pin 8: FAULT

The Fault output is latched high when a short-circuit output condition is detected. FAULT will return low when the circuit is reset using the EN pin. The FAULT output also indicates the status of the undervoltage sense circuit on V_{DD}, however the fault condition is cleared automatically when the undervoltage condition clears.

Pin 9: G2

This pin drives the gate of the external low-side power transistor.

Pin 10: GND

The ground return for V+, logic reference, and connection for source of external low-side power transistor.

Pin 11

No connection.

Pin 12: G1

This pin drives the gate of the external high side power transistor.

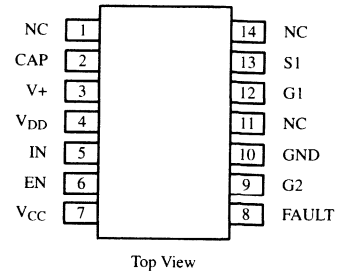
Pin 13: S1

Connection for the source of the external high-side power transistor, the drain of the external low-side power transistor, the negative terminal of the bootstrap capacitor, and the system load. The voltage on this pin is sensed by the circuitry that monitors the load for shorts.

Pin 14

No connection.

SO-14



Top View

Detailed Description

Power On Conditioning

Bootstrap-type floating supplies require that the bootstrap capacitor be charged at power on. In the case of the Si9976DY, this is accomplished by pulsing the IN line low with the EN line held high, thus turning on the low-side MOSFET and providing the charging path for the capacitor.

Operating Voltage: 20 to 40 V

The Si9976DY is intended to be powered by a single power supply within the range of 20 to 40 V and is designed to drive a totem pole pair of NMOS power transistors such as those within the Si9955. The power transistors must be powered by the same power supply as this driver. In addition to the high-voltage power supply (20 to 40 V), the Si9976DY must have a power supply connected to the V_{CC} terminal, if a fault output signal is desired. This power supply provides operating voltage for the fault output and allows the high output voltage level to be compatible with system logic that monitors the fault condition. The value of this power supply must be within the range of 4.5 to 16.5 V to ensure functionality of the output. Internal fault circuitry, which is used for shorted-load protection, is not affected by this power supply.

Cross-Conduction Protection

The high-side power transistor can only be turned on after a fixed time delay following the return to ground of the low-side power transistor's gate. The low-side transistor can only be turned on after a fixed time delay following the high-side transistor turn-off signal.

Undervoltage Lockout

During power up, both power transistors are held off until the internal regulated power supply, V_{DD}, is approximately one V_{be} from the final value, nominally 16 V. After power up, the undervoltage lockout circuitry continues to monitor V_{DD}. If an undervoltage condition occurs, both the high-side and low-side transistors will be turned off and the fault output will be set high. When the undervoltage condition no longer exists, normal function will resume automatically. Separate voltage sensing of the bootstrap capacitor voltage allows a turn-on signal to be sent to the high-side drive circuit if either the bootstrap capacitor has full voltage, or the load voltage is high (driven high by an inductive load or shorted high). The voltage sensing circuit will allow the high-side power transistor to turn on if an on signal is present and the voltage on the bootstrap capacitor rises from undervoltage to operating voltage.

Short Circuit Protection

This device is intended to be used only in a half-bridge which drives inductive loads. A shorted load is presumed if the load voltage does not make the intended transition within an allotted time. Separate timing is provided for the two transitions. A longer time is allowed for the high-side to turn on (300 ns vs. 200 ns) since the propagation delays are longer. Excessive capacitive loading can be interpreted as a short. The value of capacitance that is needed to produce the indication of a short depends on the load driving capability of the power transistors.

ESD Protection

Electrostatic discharge protection devices are between V_{DD} and GND, V_{CC} and GND, and from terminals IN, EN, G2, and FAULT to both V_{DD} and GND. V+, CAP, S1, and G1 are not ESD protected.

Fault Feedback

Detection of a shorted load sets a latch which turns off both the high-side and the low-side power transistors. If V_{CC} is present, a one level will be present on the FAULT output. To reset the system, the enable input, EN, must be lowered to a logic zero and then raised to a logic one. The logic level of the input, IN, will determine which power transistor will be turned on first after reset. An undervoltage condition on V_{DD} is not latched, but causes a one level on the FAULT output, if V_{CC} is present.

Static (dc) Operation

All components of a charge pump, except the holding (bootstrap) capacitor, are included in the circuit. This charge pump will provide current that is sufficient to overcome any leakage currents which would reduce the enhancement voltage of the high-side power transistor while it is on. This allows the high-side power transistor to be on continuously. When the low-side power transistor is turned on, additional charge is restored to the bootstrap capacitor, if needed. The maximum switching speed of the system at 50% duty cycle is limited by the on time of the low-side power transistor. During this time, the bootstrap capacitor charge must be restored. However, if the duty cycle is skewed so that the on time of the high-side power transistor is long enough for the charge pump to completely restore the charge lost during switching, then the on time of the low-side power transistor is not restricted.

Designing with the Si9976DY N-Channel Half-Bridge Driver and LITTLE FOOT Dual MOSFETs

Wharton McDaniel

Introduction

The Si9976DY is a fully integrated half-bridge driver IC which was designed to work with the LITTLE FOOT® family of power MOSFET products in 20- to 40-V systems. The Si9976DY provides the gate drive for both the low- and high-side MOSFETs while the Si9959DY (SO-8, 2.0 A), Si9955DY (SO-8, 3.0 A), Si9945 (SO-8, 3.3A) or Si9940DY (SO-16, 5.0 A) dual n-channel LITTLE FOOT MOSFETs provide power handling capability without the need of a heatsink. All of these devices are supplied in surface-mount packages. The combination of the Si9976DY and one of the dual n-channel MOSFETs creates a powerful and flexible solution for power switching in dc motor drives.

Si9976DY Overview

The Si9976DY is an integrated driver for an n-channel MOSFET half-bridge (see Figure 1). Schmitt trigger inputs provide logic signal compatibility and hysteresis for noise immunity. Low impedance outputs are provided to drive both the low- and high-side MOSFETs of the half-bridge. The addition of a bootstrap capacitor allows the internal circuitry to level shift both the power supply and the logic signals that are required for the high-side n-channel MOSFET gate drive. A charge pump has been included to replace the leakage current in the high-side driver, which allows static (dc) operation.

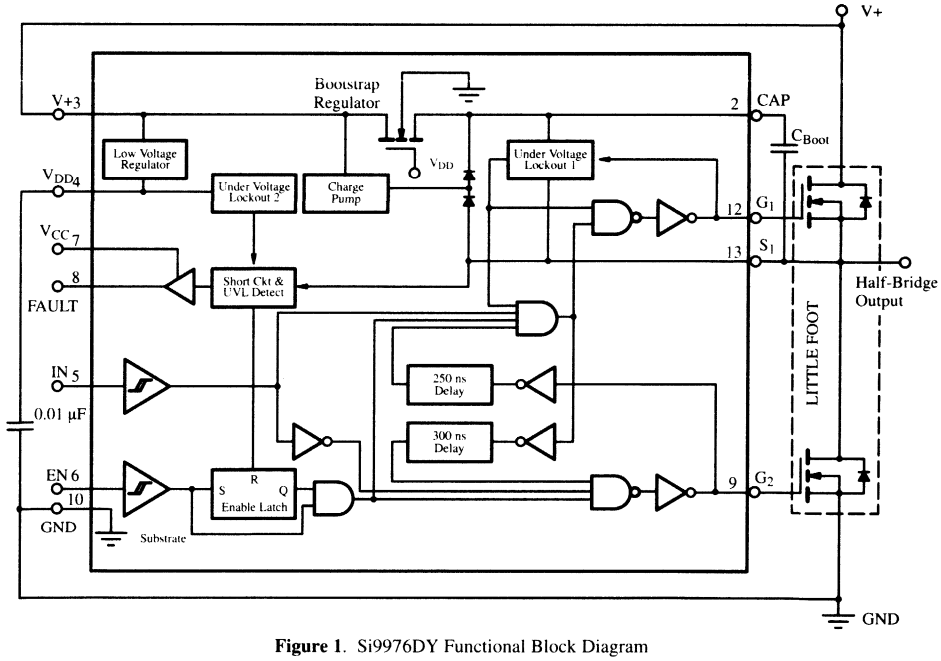


Figure 1. Si9976DY Functional Block Diagram

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A separate voltage input, V_{CC}, powers the FAULT output to allow easy interfacing to the user's system. Protection circuits include an undervoltage lockout to assure safe gate-drive levels, timing delays to prevent cross-conduction, and a monitor for short circuits on the half-bridge output (S1). An internal voltage regulator drops the input voltage (V+) to a nominal 16 V for the low-side circuitry, which allows the Si9976DY to operate over an input voltage range of 20 to 40 V. The device is specified over the industrial temperature range (–40° to +85°C).

Input Voltage Requirements

The Si9976DY operates from a single supply voltage of 20 to 40 V dc. This voltage feeds both the bootstrap and the low-voltage regulators. The bootstrap voltage regulator charges the bootstrap capacitor, while the low-voltage regulator drops the input voltage to a nominal V_{DD} of 16 V for the low-side logic and the output drive for the low-side MOSFET.

If the FAULT output is used, a separate voltage (4.5 to 16 V), must be applied to the V_{CC} pin. This guarantees compatibility with the logic levels in the motor controller.

Output Drive Details

A unique feature of the Si9976DY is the integral high-side drive circuitry. This includes logic-signal level shifting, a bootstrap power supply, a charge pump, an undervoltage lockout, and a 40-mA output driver.

A bootstrap supply and a charge pump comprise the high-side power supply, and utilize the benefits of each technique. By itself, bootstrap supply provides sufficient charge for MOSFET turn-on. However, it has two drawbacks when used alone. First, a bootstrap capacitor must be recharged after every MOSFET turn-on. Second, a bootstrap supply cannot sustain a MOSFET in the on state indefinitely because the gate leakage current continues to deplete the charge on the bootstrap capacitor. A charge pump meanwhile, can provide a continuous source of charge, but in fully integrated form it cannot provide sufficient charge for MOSFET turn-on at typical modulation frequencies. Combining the two techniques solves these problems. The bootstrap supply provides the turn-on charge while the charge pump provides the leakage current to allow static operation.

Because a bootstrap supply is used, the bootstrap capacitor must get charged immediately after power on and then be recharged after every high-side turn on. Likewise, the low-side MOSFET must be turned on to complete the charging circuit for the bootstrap capacitor. Some drive schemes toggle between the top and bottom MOSFETs, which accomplishes the required charge and recharge of the bootstrap capacitor automatically. It is important to understand that the charge pump operates only when the high-side is turned on.

The bootstrap capacitor provides the charge that turns on the high-side MOSFET. This capacitor should be sized such that it will hold 10 times the charge required to turn on a MOSFET fully (i.e., V_{GS} = 10 V). A typical capacitor value can be calculated by using the equation C_{BOOT} = 10 x (Q_g/V_{GS}). The value of Q_g is taken from the gate charge curve of the MOSFET being driven at V_{GS} =10 V. Using this method of capacitor selection, the bootstrap voltage will drop approximately 1 V when the MOSFET is turned on. A 0.01-µF capacitor works well for the Si9955DY, which requires a 10-nC charge to turn on with V_{GS} = 10 V.

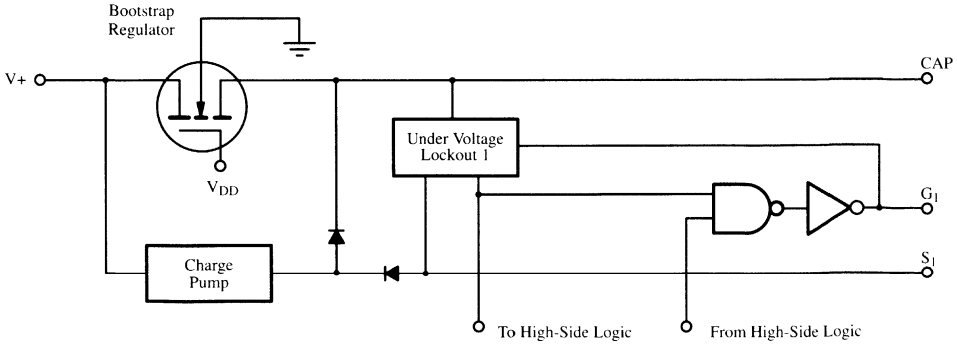


Figure 2. High-Side Drive

A certain minimum recharge time is required for the bootstrap capacitor after each high-side turn-on. The recharge time is a function of the amount of charge which has been used to turn on the high-side MOSFET, the size of the bootstrap capacitor, and the drain current of the bootstrap transistor in the Si9976DY. In the case of the Si9976DY, the recharge time decreases as V+ increases. Part of this decrease is due to the contribution of the charge pump to the recharging of the bootstrap capacitor. As V+ increases, the charge pump contribution increases. In some cases, the charge pump becomes the only source of charge required to recharge the bootstrap capacitor.

Table 1. Recommended Values

Part Number	$r_{DS(on)}$	Q_g @ V_{GS} = 10 V (nC)	Minimum Recommended C_{BOOT} (µF)
Si9940	0.05	30	0.039
Si9945	0.10	15	0.018
Si9955	0.13	8	0.01
Si9959	0.30	4.7	0.0056

Figure 3 shows the typical recharge time for the Si9959DY, Si9955DY, and Si9940DY LITTLE FOOT power MOSFETs as a function of V+. The bootstrap capacitor for each MOSFET was selected using the method described, and the switching frequency was 20 kHz.

If a shorter recharge time is required, an external signal diode can be added from V_{DD} to the positive side of the bootstrap capacitor (CAP). This increases the charging current, especially at the lower values of V+. Also, the value of the capacitor on V_{DD} should be increased, since this is the source of the additional charging current. The reduced recharge time is shown in Figure 4.

The low-side drive circuitry operates directly from V_{DD} and does not have recharge requirements. The capacitor connected to V_{DD} supplies the charge required to turn on the low-side MOSFET. It must be sized to ensure that V_{DD} does not drop below 14 V, which would trigger an undervoltage condition. As in the case of the bootstrap capacitor, the V_{DD} bypass capacitor should be sized such that it will hold 10 times the charge required by the MOSFET at a V_{GS} = 10 V ($C = 10 \times Q_g/V_{GS}$). The Si9955DY requires a 10-nC charge for turn on with V_{GS} = 10 V. Therefore, a 0.01 µF capacitor will work well. Since the requirements for value selection are the same as for the bootstrap capacitor, the recommended values in Table 1 also apply to the V_{DD} bypass capacitor. If an external bootstrap diode is used to reduce the bootstrap capacitor recharge time, the value of the V_{DD} bypass capacitor should be doubled. This compensates for the additional load of recharging the bootstrap capacitor and prevents the occurrence of an undervoltage condition.

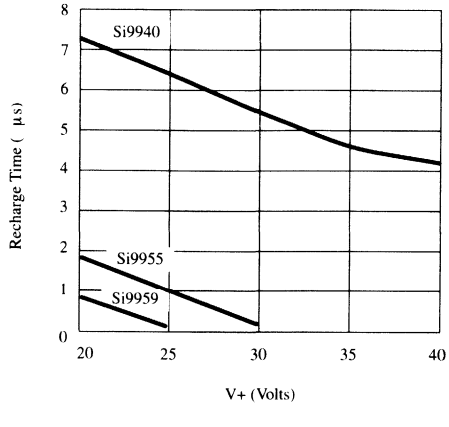


Figure 3. V+ vs. Recharge Time

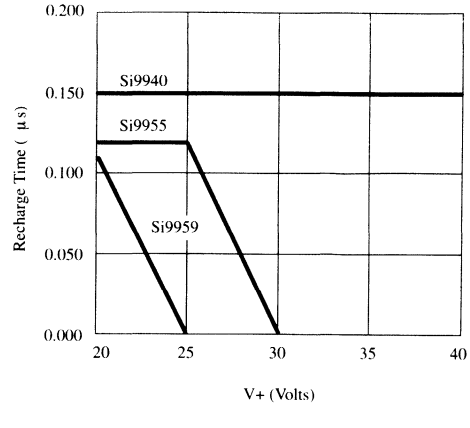


Figure 4. V+ vs. Recharge Time with Modification

Cross Conduction Protection

Turn-on delays have been incorporated to prevent cross conduction of the half-bridge MOSFETs (Figure 5). The high-side MOSFET can be turned on only after a 250-ns time delay, which is initiated by the low-side output, G2, switching to ground. The low-side MOSFET can be turned on only after a 300-ns delay which is initiated by the high-side control logic. These delays prevent one half-bridge MOSFET from turning on before the other is completely turned off. The difference in the method of generating the delays occurs because the high-side output, G1, is level shifted with respect to S1.

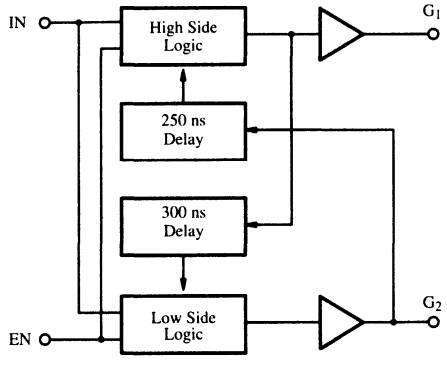


Figure 5. Cross Conduction Protection

Undervoltage Lockout

During power up, both MOSFETs are held off until the internal power supply, V_{DD}, is within approximately 0.7 V of the final value, which is nominally 16 V. After power up, the low-side undervoltage lockout circuitry, UVL2, continues to monitor V_{DD}. If an undervoltage condition occurs, both the high-side and the low-side MOSFETs will be turned off, and the FAULT output will be high. When the undervoltage condition no longer exists, the FAULT output will be cleared and normal function will resume.

A separate undervoltage lockout circuit, UVL1, monitors the bootstrap voltage. If an undervoltage condition exists when the IN line is switched high, this circuit will prevent the high-side MOSFET from turning on. In addition, one of the following conditions will exist. If S1 is high (as the result of inductive flyback current through the high-side MOSFET's body-drain diode or a short from S1 to V+), the high-side MOSFET will be allowed to turn on as soon as the undervoltage condition has been removed. If S1 is low, the high-side MOSFET will be allowed to turn on only after the undervoltage condition has been removed and the IN line has been toggled low and back to high.

Short Circuit Protection

If the load voltage, S1, does not make the intended transition through ½ V_{DD} to either ground or V+ before a specified time, the Si9976DY sees this as an output short circuit (Figure 6). The transition should take place in less than 300 ns for a transition to V+, and 200 ns for a transition to ground. Detection of a short circuit condition latches both outputs off and the fault line high. The outputs are re-enabled by a rising edge on the enable line, EN.

FAULT Output

The FAULT output goes high whenever the Si9976DY detects an output short circuit or a V_{DD} undervoltage condition. The detection of the short circuit inhibits operation and sets a fault latch which is cleared by a rising edge on the enable line, EN. The V_{DD} undervoltage condition inhibits operation and indicates a fault but is nonlatching.

Table 2. FAULT Output Truth Table

EN	IN	Condition	FAULT Output	G1 Out	G2 Out
1	0	Normal Operation	0	Low	High
1	1	Normal Operation	0	High	Low
0	X	Disabled	X	Low	Low
1	0	Load Shorted to V+	1	Low	Low
1	1	Load Shorted to Ground	1	Low	Low
1	1	Undervoltage on C_{BOOT}	0	Low	Low
1	0	Undervoltage on C_{BOOT}	0	Low	High
X	X	Undervoltage on V_{DD}	1	Low	Low

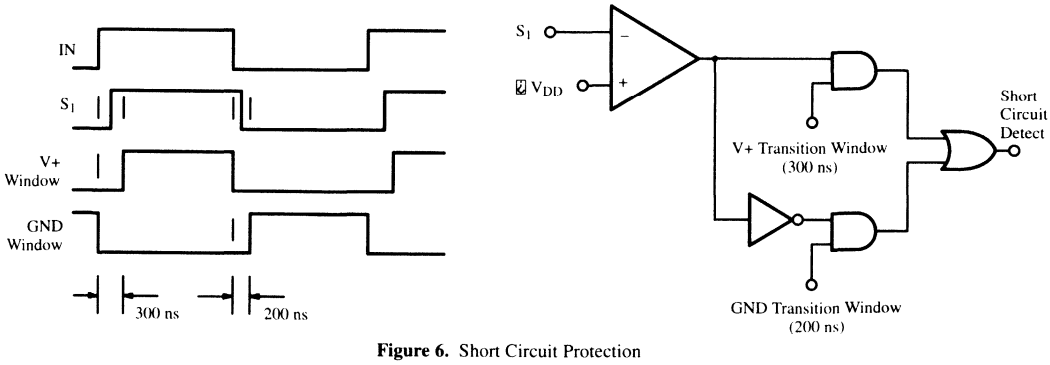


Figure 6. Short Circuit Protection

The system-logic supply voltage of 4.5 to 16.5 V can be applied to V_{CC} to facilitate interfacing of the FAULT output to the user's system. If V_{CC} is not supplied, there will be no signal on the FAULT output. However, the fault protection circuitry will continue to function as described.

PWM Circuits in H-Bridges

Anti-Phase Control

The Si9976 was designed to be used in an anti-phase control strategy. This approach is unique in that the PWM signal controls both speed and direction with duty cycle alone. Zero to 50% duty cycle defines zero to full speed in one direction, 50% duty cycle is zero speed, and 50% to 100% duty cycle defines zero to full speed in the opposite direction. This approach ensures that the bootstrap capacitor is always charged, since the H-bridge is continuously switching.

The basic hook-up of an anti-phase H-bridge is very simple. One half-bridge is driven directly with the PWM signal, and the other half-bridge is driven with the inverse of the PWM signal (see Figure 7).

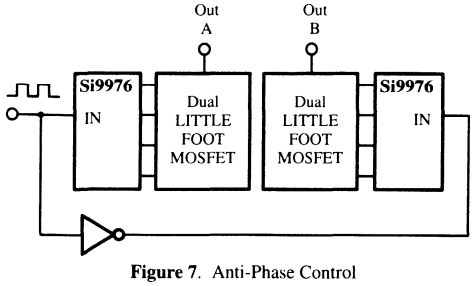


Figure 7. Anti-Phase Control

Sign-Magnitude Control

As a secondary function, the Si9976 can be used in sign-magnitude controls. In this approach, direction of rotation is determined by the diagonal pair of MOSFETs that are turned on, and speed is controlled by pulse width modulation of the active diagonal pair.

The logic required to control the H-bridge is more complex due to the need to steer the pulse width modulation signal to the active MOSFET pair. The circuit in Figure 7a applies the PWM signal only to the low-side active MOSFET.

There are a couple of things to be aware of in this mode of operation. Application of the PWM signal to the EN input when the IN input is held low will create an erroneous Fault signal which is the inverse of the PWM signal. This can be eliminated by applying the inverse of the PWM signal to the IN input as shown in Figure 7b. Secondly, care must be taken to ensure that the bootstrap capacitor has been charged prior to a high-side turn on. As low-side on-times decrease, this becomes of greater concern. Minimum low-side on-times must be observed to ensure that the high-side will turn on. Remember that this minimum time can be reduced by adding an external bootstrap diode (see Figure 8). When this is done, it increases the load on V_{DD} and therefore on the decoupling capacitor. The value of the V_{DD} decoupling capacitor should be doubled to prevent an undervoltage condition from occurring.

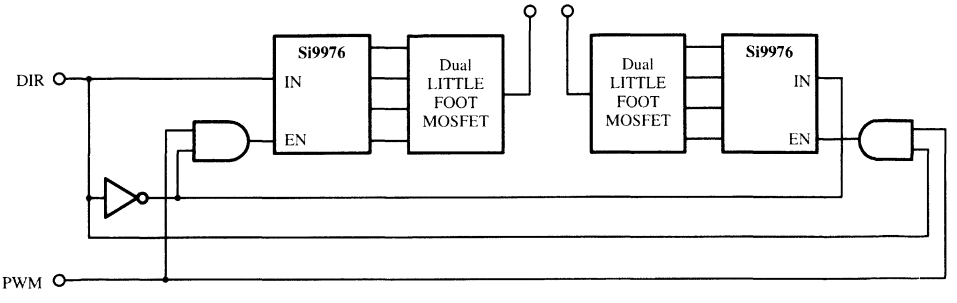


Figure 7a. Sign-Magnitude Control

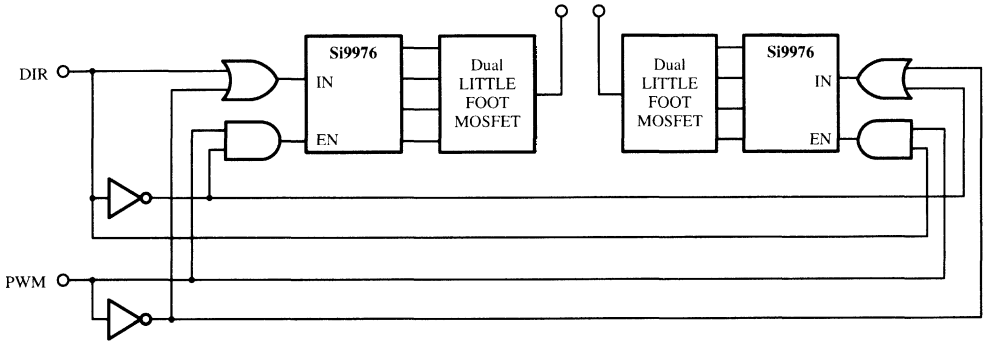


Figure 7b. Sign-Magnitude Control for Low-Side MOSFET PWM

Braking

Braking is accomplished by turning on both upper or both lower MOSFETs in the H-bridge so the motor windings are shorted together. If the upper MOSFETs are used for this function, be certain that the bootstrap capacitors are charged prior to turning them on.

Current Sensing

If current sensing is required, a fractional Ω resistor can be inserted in between the low-side MOSFET source connection and ground. External op amps or comparators can then be used to implement current limit or some other current control. A Schottky diode must be connected from the half-bridge output to ground to protect output from negative voltage spikes. In addition to causing potential damage to the Si9976, negative spikes can cause an erroneous latching FAULT. The sensing resistor provides a small amount of isolation of the MOSFET decoupling capacitors from ground. Make sure that decoupling capacitors on MOSFETs are connected directly across the MOSFET pair, high-side drain to low-side source to maximize their effectiveness at reducing noise (see Figure 9).

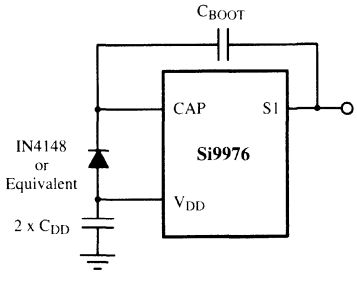


Figure 8. External Bootstrap Diode

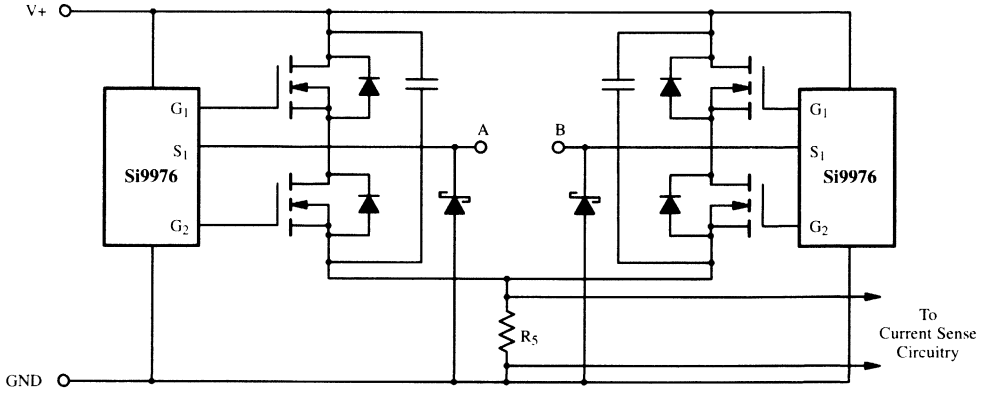


Figure 9. Current Sensing

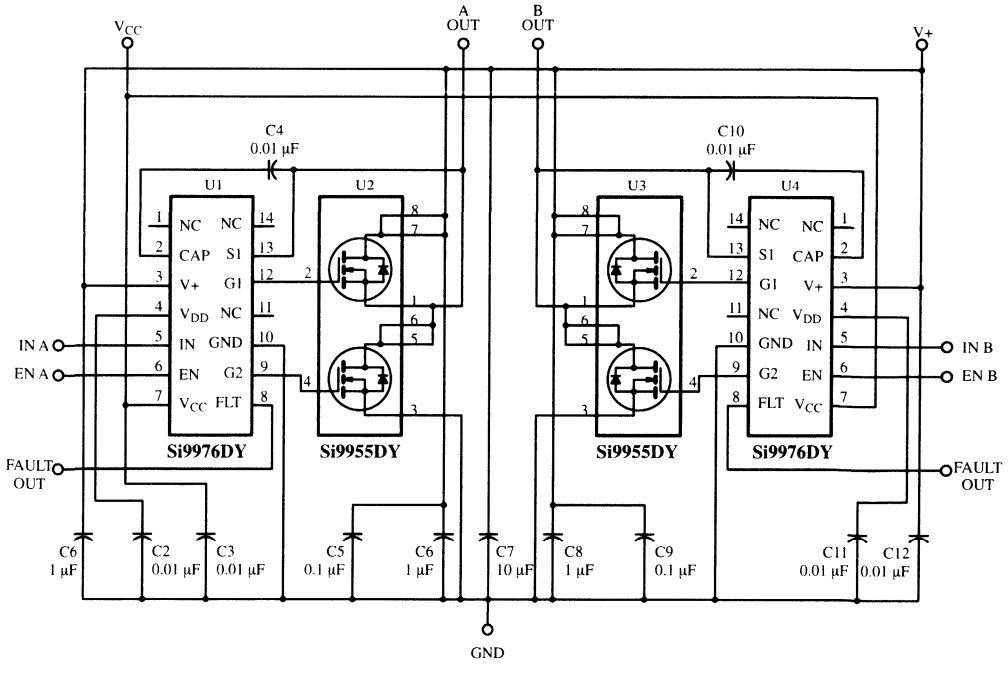


Figure 10 Full-Bridge Configuration with the Si9976DY and the Si9955DY

A Full-Bridge Application

Figure 10 shows a basic implementation of the Si9976DY and Si9955DY in a full-bridge configuration. Each half-bridge is made up of one Si9976DY driver IC, one Si9955DY LITTLE FOOT dual n-channel MOSFET, a bootstrap capacitor, a filter capacitor for V_{DD}, and decoupling capacitors for each IC. This configuration yields a full-bridge circuit with a continuous current rating of 3 A without heatsinking. Use of the Si9959DY or the Si9940DY yields current ratings of 2 A or 5 A, respectively.

Any circuit which generates signals with fast rise and fall times can generate noise. This noise, if not dealt with, can affect the operation of the circuit. Proper PC board layout techniques and device decoupling will take care of these problems. The signal ground trace from the Si9976DY and the trace from the low-side MOSFET source should be run separately to the common ground point. This prevents the noise generated by fast MOSFET transitions from modulating the signal ground of the Si9976DY. Similarly, the trace to the V+ input of the Si9976DY and the trace to the drain of the high-side MOSFET should be connected separately to the supply bypass capacitor.

In addition to layout considerations, decoupling capacitors are required to deal with noise. Adding capacitors across the power supply lines, V+, V_{DD}, and V_{CC}, provides a low impedance to ground for switching noise and serves as a local energy reservoir when there is a demand for surge current. The V_{DD} capacitor provides the surge current required to turn on the low-side MOSFET.

In addition to basic decoupling, the capacitors added across the half-bridge itself minimize the surge current in the power supply traces, and therefore reduce the generated noise. Although a single capacitor, typically 0.01 µF, works well to decouple a single pin, it is advisable to apply several decades of capacitance across the input power, V+ to GND, to handle the broad spectrum of noise that can be present. The high-frequency (lower value) capacitors should be located as close as possible to the device being decoupled, while the larger capacitors (> 1 µF) can be located farther away and bypass only the power supply.

Figure 11 shows a typical layout for a Si9976DY with LITTLE FOOT dual n-channel MOSFETs. The use of surface-mount packages allows automated assembly of the entire motor drive circuit, without the need for a separate heatsink and its associated material and assembly costs.

Summary

The Si9976DY provides both low- and high-side gate drive, high-side level shifting, a bootstrap/charge pump high-side power supply, and protection for undervoltage and short circuit conditions in a single surface-mount IC. The Si9940DY, Si9945DY, Si9955DY and Si9959DY are surface-mount MOSFETs for power switching over a broad current range (2 to 5 A) and require no heatsinking. The use of surface-mount packages allows automated assembly of the entire drive system while minimizing use of PC board space. The Si9976DY, when used with one of the dual n-channel LITTLE FOOT power MOSFETs, provides a very flexible approach to power switching in dc motor drives.

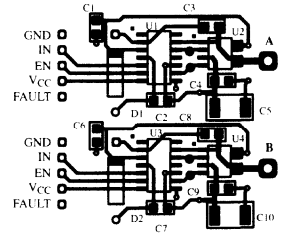


Figure 11 Typical PC Board Layout (Scale 1:1)

Configurable H-Bridge Driver

Features

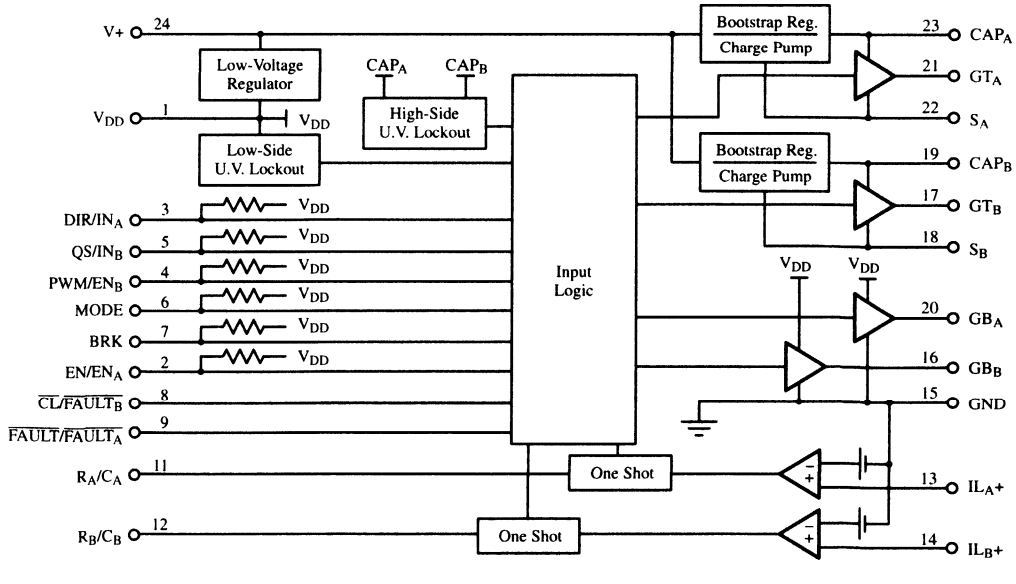
- H-Bridge or Dual Half-Bridge Operation
- 20- to 40-V Supply
- Static (dc) Operation
- Cross-Conduction Protected
- Current Limit
- Undervoltage Lockout
- ESD Protected
- Fault Output

Description

The Si9978DW is an integrated driver for an n-channel MOSFET H-bridge. The mode control allows operation as either a full H-bridge driver or as two independent half-bridges. The DIR/PWM input configuration allows easy implementation of either sign/magnitude or anti-phase PWM drive schemes for full H-bridges. Schmitt triggers on the inputs provide logic signal compatibility and hysteresis for increased noise immunity. An internal low-voltage regulator allows the device to be powered directly from a system supply of 20 to 40 volts. All n-channel gates are driven directly from low-impedance outputs. The addition of one external capacitor per half-bridge allows internal circuitry to level shift both the power supply and logic signal for the high-side n-channel gate drives. Internal charge pumps replace leakage current lost in the high-side driver circuits to provide "static" (dc) operation in any output condition. Protection features include an undervoltage lockout, cross-conduction prevention logic, and overcurrent monitors.

The Si9978DW is available in the 24-pin wide-body SOIC (surface mount) package, specified to operate over the industrial (–40 to +85°C) temperature range.

Functional Block Diagram



Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70011 .

Absolute Maximum Ratings

Voltage on pins 2–7 with respect to ground −0.3 to V_{DD} + 0.3 V
Voltage on pin 24 ..... −0.3 to 50 V
Voltage on pins 17, 19, 21, 23 ..... −0.3 to +60 V
Voltage on pins 18, 22 ..... −2 to 50 V

Operating Temperature (T_A) ..... −40 to +85°C
Storage Temperature ..... −65 to 150°C
Maximum Junction Temperature (T_J) ..... 150°C
Power Dissipation ..... 500 mW

Recommended Operating Conditions

V+ ..... +20 to 40 V_{DC}
R_A, R_B ..... 100 kΩ

Specifications

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 20 to 40 V	Limits −40 to 85°C			Unit
			Min[a]	Typ[b]	Max[a]	
Power						
Supply Voltage Range	V+		20		40	V
Logic Voltage	V_{DD}		14.5	16	17.5	
Supply Current	I+	I_{DD} = 0 mA		3	5	mA
Inputs (DIR, PWM, EN, QS, MODE, BRK)						
High-State	V_{IH}		4.0			V
Low-State	V_{IL}				1.0	
High-State Input Current	I_{IH}	$V_{IH} = V_{DD}$			10	µA
Low-State Input Current	I_{IL}	V_{IL} = 0 V	−100	−50	−25	
Outputs						
Low-Side Gate Drive, High State	V_{GBH}		14	16	17.5	V
Low-Side Gate Drive, Low State	V_{GBL}				1	
High-Side Gate Drive, High State	V_{GTH}	$S_{A, B}$ = 0 V	14	16	18	
High-Side Gate Drive, Low State	V_{GTL}				1	
Low-Side Switching, Rise Time	t_{rL}	Rise Time = 1 to 10 V Fall Time = 10 to 1 V C_L = 600 pF		110		ns
Low-Side Switching, Fall Time	t_{fL}			50		
High-Side Switching, Rise Time	t_{rH}			110		
High-Side Switching, Fall Time	t_{fH}			50		
Break-Before-Make Time				250		
$\overline{FAULT}$, $\overline{CL}$	V_{OL}	I_{OL} = 1 mA			0.4	V
$\overline{FAULT}$, $\overline{CL}$ Leakage Current	I_{OH}	$\overline{FAULT}$, $\overline{CL}$ = V_{DD}		0.2	10	µA
Protection						
Low-Side Undervoltage Lockout	UVLL			0.8 V_{DD}		V
Low-Side Hysteresis	V_H			0.8		
High-Side Undervoltage Lockout	UVLH	$S_{A, B}$ = 0 V		V_{DD}−3.3 V		

Specifications

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 20 to 40 V	Limits −40 to 85°C			Unit
			Min[a]	Typ[b]	Max[a]	
Current Limit						
Comparator Input Bias Current	I_{IB}		−5	−0.2	5	µA
Comparator Threshold Voltage	V_{TH}	T_A = 25°C	90	100	110	mV
			85		115	
One Shot Pulse Width	t_p	R_A, R_B = 100 kΩ, C_A, C_B = 100 pF	8	10	12	µs
		R_A, R_B = 100 kΩ, C_A, C_B = 0.001 µF	80	100	120	
Propagation Delay	t_{pd}	C_L = 600 pF		600		ns

Notes:
a. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

Truth Table

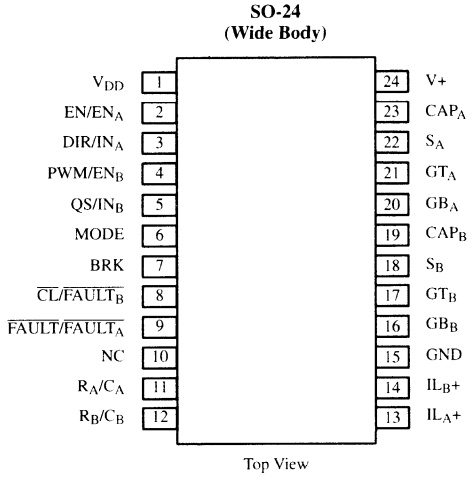
H-Bridge Mode

MODE	DIR/ IN_A	EN/ EN_A	QS/ IN_B	PWM/ EN_B	BRK	IL_A+	IL_B+	GT_A	GB_A	GT_B	GB_B	$\overline{CL}$/ $\overline{FAULT_B}$	FAULT/ $FAULT_A$	Condition
1	1	1	1	⎍	0	L	X	H	L	L	⎍	1	1	Normal Operation
1	1	1	0	⎍	0	L	X	⎍	L	L	⎍	1	1	
1	0	1	1	⎍	0	L	X	L	⎍	H	L	1	1	
1	0	1	0	⎍	0	L	X	L	⎍	⎍	L	1	1	
1	**X**	**1**	**X**	**X**	**1**	**L**	**X**	**L**	**H**	**L**	**H**	**1**	**1**	**Brake**
1	**X**	**0**	**X**	**X**	**X**	**L**	**X**	**L**	**L**	**L**	**L**	**1**	**1**	**Disable**
1	**X**	**1**	**X**	**X**	**0**	⎍	**X**	**L**	**L**	**L**	**L**	⎎	⎎	**Overcurrent**
1	X	X	X	X	X	X	X	L	L	L	L	1	0	Undervoltage on V_{DD}

Half-Bridge Mode

MODE	DIR/ IN_A	EN/ EN_A	QS/ IN_B	PWM/ EN_B	BRK	IL_A+	IL_B+	GT_A	GB_A	GT_B	GB_B	$\overline{CL}$/ $\overline{FAULT_B}$	FAULT/ $FAULT_A$	Condition
0	1	1	X	0	X	L	L	H	L	L	L	1	1	Normal Operation
0	0	1	X	0	X	L	L	L	H	L	L	1	1	
0	X	0	1	1	X	L	L	L	L	H	L	1	1	
0	X	0	0	1	X	L	L	L	L	L	H	1	1	
0	**X**	**1**	**X**	**X**	**X**	⎍	**X**	**L**	**L**	**X**	**X**	**1**	⎎	**Overcurrent on A**
0	**X**	**X**	**X**	**1**	**X**	**X**	⎍	**X**	**X**	**L**	**L**	⎎	**1**	**Overcurrent on B**
0	X	X	X	X	X	X	X	L	L	L	L	0	0	Undervoltage on V_{DD}

Pin Configuration



Pin Description

Pin 1: V_{DD}

V_{DD} is an internally generated voltage. It is connected to this pin to allow connection of a decoupling capacitor. A minimum of 1 µF is recommended.

Pin 2: EN/EN_A

The EN input allows normal operation when at logic "1", and turns all gate drive outputs off when at logic "0". When the mode pin is at logic "1", EN controls the entire H-bridge. When the mode pin is at logic "0", this pin becomes the ENABLE pin for half-bridge A.

Pin 3: DIR/IN_A

The function of this pin is determined by the MODE pin. When the MODE pin is at logic "1", it is the DIR pin, and when MODE is at logic "0", it is the IN_A pin.

As the DIR input, it is the direction control for the H-bridge, and determines which diagonal pair of power MOSFETs is active. A logic "1" turns on GT_A and enables GB_B, while a logic "0" turns on GT_B and enables GB_A. When implementing an anti-phase PWM control, the DIR input serves as the PWM input.

As the IN_A pin, it is the input that controls the "A" half-bridge. When at logic "1", the high-side MOSFET is turned on, and when at logic "0", the low-side MOSFET is turned on.

Pin 4: PWM/EN_B

With the mode pin at logic "1", this pin is the PWM input. It controls the switching of the active diagonal pair. A logic "1" turns the active MOSFETs on, while a logic "0" turns it off. The QS input determines whether the bottom or both bottom and top MOSFETs are switched. When implementing an anti-phase PWM control, the PWM input is connected to a logic "1". When the mode pin is at logic "0", this pin becomes the ENABLE pin for half-bridge B.

Pin 5: QS/IN_B

With the mode pin at logic "1", this input determines whether the bottom MOSFETs of the H-bridge or both bottom and top MOSFETs switch in response to the PWM signal. A logic "1" on this input enables only the bottom MOSFETs. This is the default condition as this pin is pulled up internally. When this pin is pulled to ground, both the bottom and top MOSFETs are enabled.

This input controls the B half-bridge when the MODE pin is at logic "0". When at logic "1", the high-side MOSFET is turned on, and when at logic "0", the low-side MOSFET is turned on.

Pin Description (Cont'd)

Pin 6: MODE

This input determines whether the Si9978 functions as an H-bridge or as two independent half-bridges. When the MODE pin is at logic "1", the Si9978 functions as an H-bridge, and when MODE is at logic "0", it functions as two independent half-bridges.

Pin 7: BRK

When this input and MODE are at logic "1", both bottom gate drives are switched high, turning on the bottom MOSFETs. When this input is at logic "0", the Si9978 operates normally.

Pin 8: $\overline{CL}/\overline{FAULT_B}$

This is an open drain output which is active low. When the MODE pin is at logic "1", this pin functions as $\overline{CL}$ and indicates that the H-bridge is in current limit. It stays low for the duration of the current limit one-shot. With the MODE pin at logic "0", it serves as the $\overline{FAULT}$ output for half-bridge B to indicate when an undervoltage or overcurrent condition is detected. When indicating an overcurrent condition, the output stays low for the duration of the current limit one-shot. The $\overline{FAULT}$ output resets automatically when the condition clears.

Pin 9: $\overline{FAULT}/\overline{FAULT_A}$

This is an open drain output which is switched low when an undervoltage or overcurrent condition is detected. When indicating an overcurrent condition, the output stays low for the duration of the current limit one-shot. When the MODE pin is at logic "1", this pin is the H-bridge $\overline{FAULT}$ output. With the MODE pin at logic "0", it serves as the $\overline{FAULT}$ output for half-bridge A. The $\overline{FAULT}$ output resets automatically when the condition clears.

Pin 10: NC

No internal connection.

Pin 11: R_A/C_A

The timing resistor and capacitor for the current limit one-shot are connected to this pin. The values of the resistor and capacitor determine the off time set by the one-shot. The one-shot is triggered when the current limit comparator detects an overcurrent condition.

Pin 12: R_B/C_B

The timing resistor and capacitor for the current limit one-shot are connected to this pin. The values of the resistor and capacitor determine the off time set by the one-shot. The one-shot is triggered when the current limit comparator detects an overcurrent condition.

Pin 13: IL_A+ and Pin 14, IL_B+

These are the overcurrent sense inputs. Internally, they are connected to the noninverting inputs of the current limit comparators. Externally they are connected to the source(s) of the low-side MOSFET(s) and the current sense resistor.

Pin 15: GND

The GND pin is the ground return for V+ and the ground reference for the logic. Also, this is the ground reference input for the current limit comparators and is connected to the ground side of the internal 100-mV references. This pin should be connected directly to the ground side of the current sensing resistors.

Pin 16: GB_B and Pin 20, GB_A

These pins drive the gates of the low-side power MOSFETs.

Pin 17: GT_B and Pin 21, GT_A

These pins drive the gates of the high-side power MOSFETs.

Pin 18: S_B and Pin 22, S_A

These are the source connections of the high-side power MOSFETs, the drain of the external low-side power MOSFET, the negative terminal of the bootstrap capacitor, and the output for each half-bridge.

Pin 19: CAP_B and Pin 23, CAP_A

These are the connections for the positive terminals of the bootstrap capacitors C_{BA} and C_{BB}. A 0.01-µF capacitor can be used for most applications.

Pin 24: V+

This is the only external power supply required for the Si9978DW, and must be the same supply used to power the H-bridge it is driving. The Si9978DW powers the low-voltage logic, low-side gate driver, and bootstrap/charge pump circuits from self-contained voltage regulators which require only a bootstrap capacitor on the CAP pins.

No voltage sensing circuitry monitors V+ directly; however, the low-voltage, internally generated supply and the bootstrap voltage (which are derived from V+) are directly protected by undervoltage monitors.

Applications

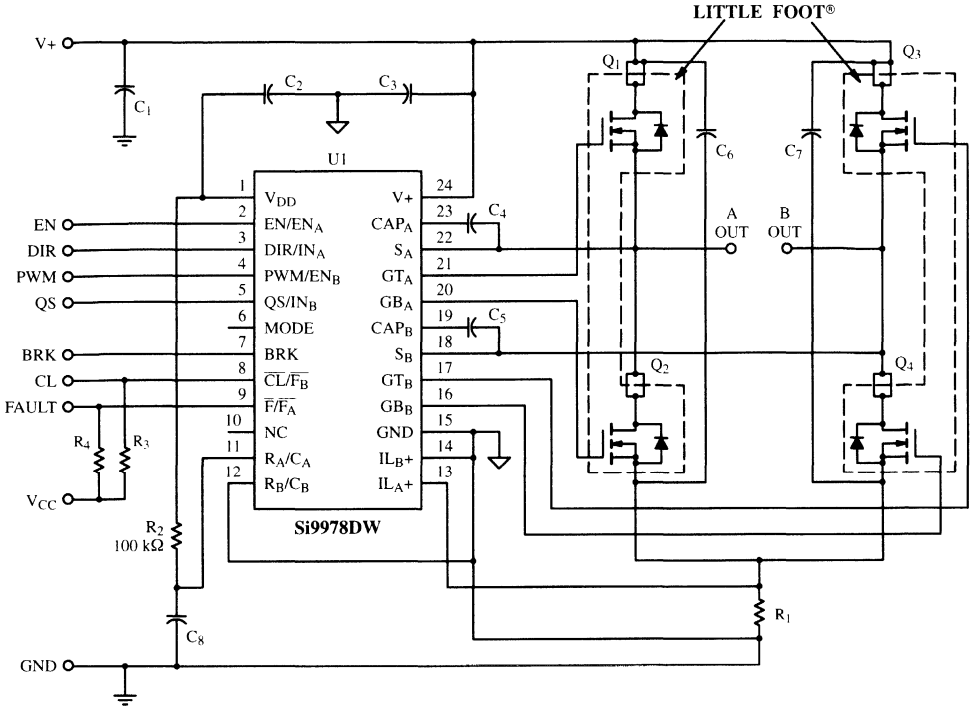


Figure 1. Basic H-Bridge Circuit

Designing With the Si9978DW Configurable H-Bridge Controller

Wharton McDaniel

Currently, there are a number of fully integrated H-bridges on the market. Both bipolar and MOS technologies have been used to create these parts. However, all of them suffer from problems such as limited current handling capability, large package size, and difficulty of assembly. The Si9978DW addresses these problems with an architecture that allows flexible current handling capability, small size, and ease of assembly. Instead of trying to integrate the power devices with the controller on a single piece of silicon, the Si9978DW approach is to separate the controller from the MOSFETs. The benefit is efficient manufacture of both the controller and the MOSFETs, the flexibility to select the optimum MOSFET for the application, and the ability to use surface-mount parts for both the controller and MOSFETs which makes assembly easier. Altogether this means a low cost H-bridge solution.

The Si9978DW is a monolithic controller designed to be used with LITTLE FOOT® power MOSFETs to create an all-n-channel H-bridge or two separate half bridges. In addition to this functional flexibility, the dual function allows standardization of components and reduces inventory costs. The Si9978DW features integral high-side drive circuitry and an internal voltage regulator, which allows operation over a 20- to 40-V dc input voltage range. Protection features include cross-conduction protection, current limiting, and undervoltage lockout. The $\overline{\text{FAULT}}$ outputs indicate when undervoltage or overcurrent shutdown has occurred. The Si9978DW is packaged in a 24-pin wide body SOIC.

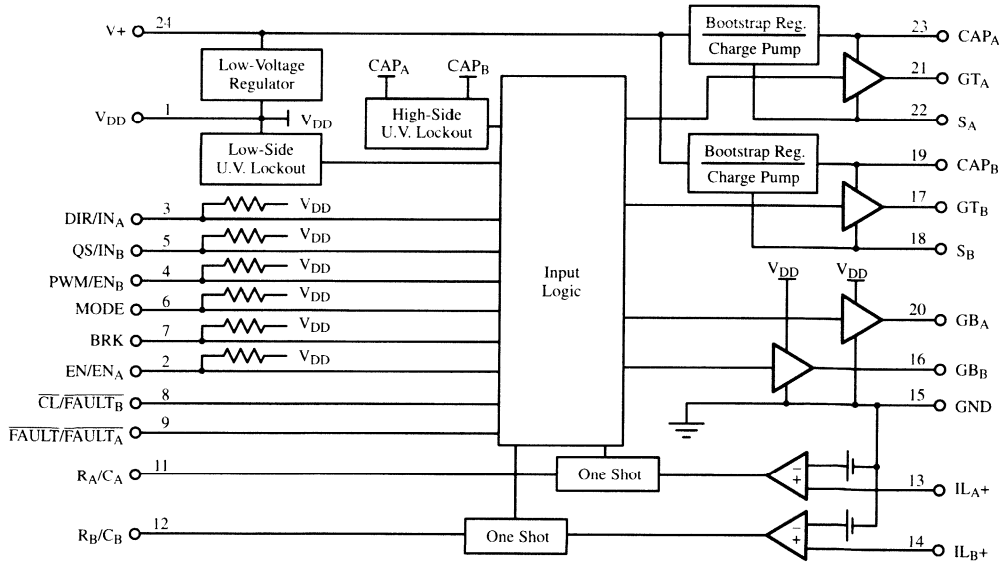


Figure 1. The Si9978 is made up of the control logic, the gate drive outputs, V_{DD} regulator, and protection circuitry.

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Control Logic

The Si9978 has two modes of operation, full H-bridge, and independent half-bridge. The mode of operation determines the function of the input pins and the $\overline{\text{FAULT}}$ outputs. With the MODE pin at logic 1, which is the default condition, the Si9978 functions as a full H-bridge. With the MODE pin at logic 0, the Si9978DW functions as two independent half-bridges. The definitions of the control inputs depend on the mode of operation. All control inputs are pulled up to V_{DD}. The $\overline{\text{FAULT}}$ outputs are open drain. Truth Tables have been provided for each mode of operation.

Full H-Bridge Operation

When operating as a full H-bridge, the control inputs become DIR, QS, PWM, BRK, and EN. When connecting the bridge for anti-phase operation, the DIR input is driven by the control system PWM signal. When connected for sign-magnitude operation, the DIR input controls direction, and the system PWM signal drives the PWM input.

Independent Half-Bridge Operation

In the independent half-bridge mode, the control inputs become the independent controls for each half-bridge, INA, ENA, INB, ENB. The BRK input is not functional in this mode of operation.

Gate Drive Outputs

Each half-bridge output is driven by a pair of n-channel MOSFETs. These are controlled by a low- and a high-side gate driver. They have been designed to drive a 600 pF load with a 110-ns rise time and a 50-ns fall time.

Table 1. H-Bridge Mode

MODE	DIR/ IN_A	EN/ EN_A	QS/ IN_B	PWM/ EN_B	BRK	IL_A+	IL_B+	GT_A	GB_A	GT_B	GB_B	$\overline{\text{CL}}$/ $\overline{\text{FAULT}_B}$	FAULT/ FAULT_A	Condition
1	1	1	1	⎍	0	L	X	H	L	L	⎍	1	1	Normal Operation
1	1	1	0	⎍	0	L	X	⎍	L	L	⎍	1	1	
1	0	1	1	⎍	0	L	X	L	⎍	H	L	1	1	
1	0	1	0	⎍	0	L	X	L	⎍	⎍	L	1	1	
1	**X**	**1**	**X**	**X**	**1**	**L**	**X**	**L**	**H**	**L**	**H**	**1**	**1**	Brake
1	**X**	**0**	**X**	**X**	**X**	**L**	**X**	**L**	**L**	**L**	**L**	**1**	**1**	Disable
1	**X**	**1**	**X**	**X**	**0**	⎍	**X**	**L**	**L**	**L**	**L**	⎎	⎎	Over-current
1	X	X	X	X	X	X	X	L	L	L	L	1	0	Undervoltage on V_{DD}

Table 2. Half-Bridge Mode

MODE	DIR/ IN_A	EN/ EN_A	QS/ IN_B	PWM/ EN_B	BRK	IL_A+	IL_B+	GT_A	GB_A	GT_B	GB_B	$\overline{\text{CL}}$/ $\overline{\text{FAULT}_B}$	FAULT/ FAULT_A	Condition
0	1	1	X	0	X	L	L	H	L	L	L	1	1	Normal Operation
0	0	1	X	0	X	L	L	L	H	L	L	1	1	
0	X	0	1	1	X	L	L	L	L	H	L	1	1	
0	X	0	0	1	X	L	L	L	L	L	H	1	1	
0	**X**	**1**	**X**	**X**	**X**	⎍	**X**	**L**	**L**	**X**	**X**	**1**	⎎	Over-current on A
0	**X**	**X**	**X**	**1**	**X**	**X**	⎍	**X**	**X**	**L**	**L**	⎎	**1**	Over-current on B
0	X	X	X	X	X	X	X	L	L	L	L	0	0	Undervoltage on V_{DD}

The low-side gate is driven directly from the commutation logic and is powered by V_{DD}. This means that V_{DD} must be decoupled with a 1-µF capacitor; otherwise the turn-on surge current can cause V_{DD} to drop to the level of an undervoltage condition. The high side is a floating circuit powered from a combination bootstrap/charge pump supply. The bootstrap capacitor is charged to V_{DD} when ever the low-side MOSFET is turned on. At all other times, the charge pump keeps the bootstrap capacitor charged, replacing the charge used in powering the high-side circuitry and in turning on the MOSFET.

The value of the bootstrap capacitor is a function of the MOSFET being driven. The bootstrap voltage should not drop more than 1 V as the result of a MOSFET turn-on. For a 60-V dual n-channel MOSFET like the Si9945DY, 15 nC (Qg) is required for turn-on at a Vgs of 10 V. Using the equation $C = Qg/V_{GS}$, 1.5 nF is required to provide sufficient charge for turn-on. To meet the criterion of dropping only 1 V at turn-on, the capacitor needs to be 10 times as large, making the equation $C_{BOOT} = 10(Qg/V_{GS})$. This makes the minimum value of C_{BOOT} equal to 0.015 µF. Table 3 gives minimum recommended values for several MOSFETs that might be used with the Si9979. This minimum recommended value is one standard value above the minimum calculated value.

Protection Circuitry

The protection circuitry provides current limit, cross-conduction protection, undervoltage lockout, and the $\overline{\text{FAULT}}$ output.

Current Limit

The current limit circuitry consists of two comparators, each driving a one-shot multivibrator (Figure 2). In the full H-bridge mode, comparator A controls the entire H-bridge. In the half-bridge mode, the two comparators function independently with their respective half-bridge. Each comparator has an internal 100-mV reference voltage on the inverting input and an external sensing resistor connected to the non-inverting input. These inputs should be connected directly to the sensing resistor. This will eliminate the effects of any noise in the ground traces.

The motor current must generate 100 mV across a sensing resistor for the comparator to trip. This in turn triggers theone-shot, turning off the active MOSFETs for a period defined by the product of the appropriate R and C.

Table 3. Bootstrap Capacitor Selection

Part Number	$r_{DS(on)}$	Qg @ V_{GS} = 10 V (nC)	Minimum Recommended C_{BOOT} (µF)
Si9940	0.05	30	0.039
Si9945	0.10	15	0.018
Si9955*	0.13	8	0.01
Si9959	0.30	4.7	0.0056

*Recommended replacement Si9945

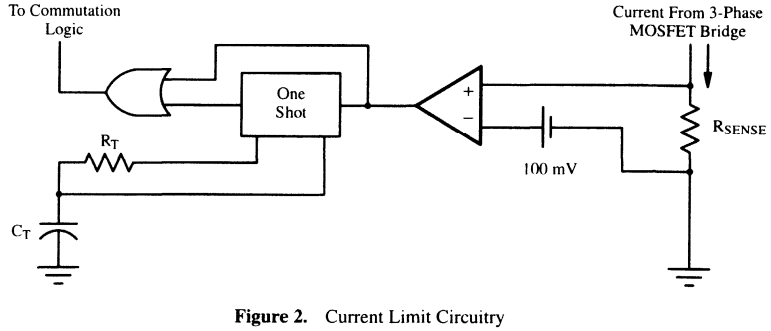


Figure 2. Current Limit Circuitry

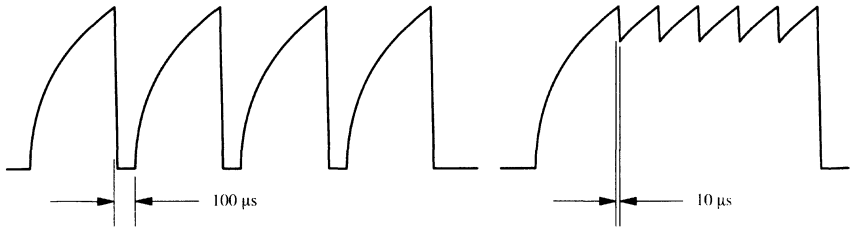


Figure 3. Current Waveforms

If the current has dropped below the threshold by the time the off period has expired, the MOSFETs will be turned on again. If the overcurrent condition remains after the off period has expired, the MOSFETs will be held off until the current drops below the threshold.

Cycle-by-cycle current limiting is achieved when the current limit off period is in the 100-µs range. If the current limit off period is reduced to the 10-µs range, a constant current mode current limit is achieved. In this mode, the RMS current (and therefore the torque) is maximized for the current limit setting. This result is particularly useful when a maximum acceleration rate is required at power on. Figure 3 shows typical current waveforms for both durations of the off period.

Cross Conduction Protection

When driven as an anti-phase H-bridge or in the independent half-bridge mode, the high-side and low-side MOSFETs of each active phase are toggled. To prevent shoot-through, each half-bridge has break-before-make circuitry. This delays the MOSFET turn-on for approximately 250 ns from the turn-off of the opposite MOSFET.

Undervoltage Lockout

Internal circuitry monitors the voltage level on V_{DD} and the high-side supplies. This ensures that there is sufficient voltage to turn on the MOSFETs. Should the voltage level on V_{DD} drop below 0.75 x V_{DD}, all gate drives will be turned off until the undervoltage condition is gone. Each of the high-side supplies is monitored only when it is referenced to ground. If the high-side voltage is under V_{DD} - 3.3 V, the high side will not be allowed to turn on.

$\overline{FAULT}$ Outputs

The Si9978DW has a pair of $\overline{FAULT}$ outputs whose exact function changes according to mode of operation. In the H-bridge mode, the $\overline{FAULT}$ output indicates either an undervoltage or a current limit condition. The CL output indicates when there is a current limit condition. In the half-bridge mode, these outputs become $\overline{FAULT}_A$ and $\overline{FAULT}_B$, indicating either an undervoltage or a current limit condition for their respective half-bridge.

These outputs are configured as open drain outputs. The open drain configuration permits connection to wide range of voltages and several $\overline{FAULT}$ outputs can be wire-OR'd. A negative going transition indicates the undervoltage or current limit condition exists.

An H-Bridge Circuit

Figure 4 shows a basic H-bridge circuit. This circuit is based on the Si9978DW driving two dual MOSFETs in SO packages (LITTLE FOOT). All that remains is the passive devices required for current limit timing, filtering of the floating high-side supplies, pull-ups for the $\overline{FAULT}$ outputs, and decoupling of the V+ power supply, the Si9978DW, and the power MOSFETs.

The Power MOSFETs

Assuming that the H-bridge has to handle a 2-A load, a 130-mΩ (@25°C) MOSFET is needed to allow operation at elevated temperature. The Si9945DY exceeds this requirement with on-resistance of 100 mΩ at 25°C. With the junction at 150°C, the $R_{DS(on)}$ will rise to 0.19 Ω. At a 2-A load, the 0.8-W dissipation is within the Si9945DY's rating and leaves headroom for starting current.

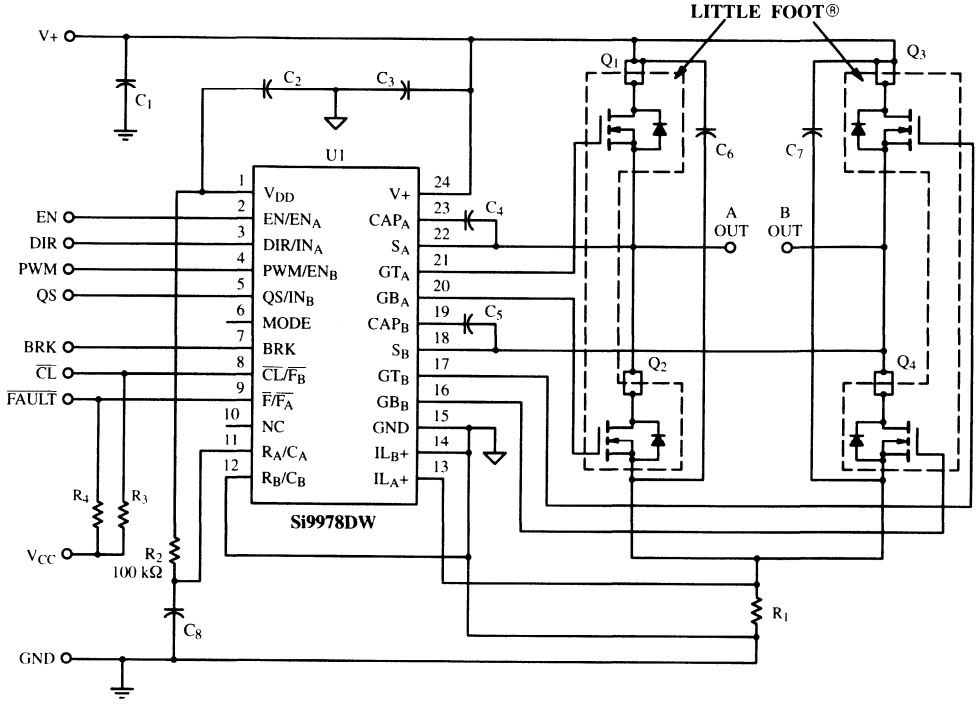


Figure 4. Basic H-Bridge Circuits

The Current Sense Resistor

The current limit level is determined by the motor starting requirements, such as acceleration time, the power capability of the power MOSFETs, and the ability of the system power supply to supply current to the motor. For this design, the current limit level will be set at 3 A peak. There is a simple way to set this level. Select a sensing resistor which will give 100 mV when 3 A flows through it. Using Ohm's law, Rs = 100 mV/Ipk. Thus a 33-mΩ resistor is required. A 0.5-W resistor will handle the starting condition. At the load current of 2 A, power dissipation is less than 150 mW.

Current Limit One-Shot Timing

If the current limit off-time is kept short, acceleration can take place as quickly as possible while respecting the peak starting current of 3 A. The recommended setting is 10 µs. Since this off-time is defined by the product of R and C, R is set to 100 kΩ, making C equal to 100 pF. Since the Si9978DW is connected as a full H-bridge, the comparator driven by IL_A+ controls the current limit function for the entire H-bridge. R_A and C_A are the timing components and therefore assume the values of 100 kΩ and 100 pF. IL_B+ and R_B/C_B should be connected to ground to ensure that noise does not cause a malfunction.

Bootstrap Capacitor Selection

The value of the bootstrap capacitor is determined by the gate charge required for the MOSFET selected. The Si9945DY requires 15 nC (Qg) at a V_{gs} of 10 V (Figure 12). Using the equation $C_{BOOT} = 10\ (Qg/V_{GS})$, the typical value is 0.015 µF. Table 3 shows a recommended minimum value of 0.018 µF, which provides some headroom.

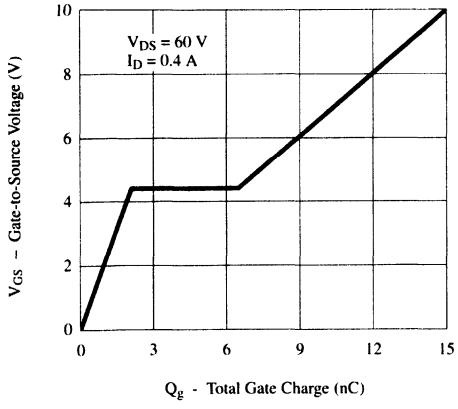
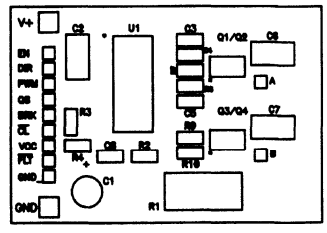


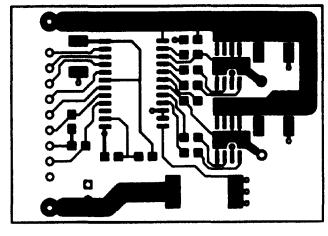
Figure 5. Gate Charge

Decoupling

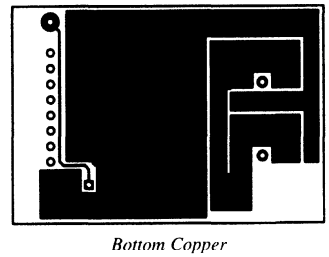
Decoupling is required for V+, V_{DD}, and the power MOSFETs. A 0.1-µF capacitor, C3, should be connected to the V+ pin. V_{DD} requires a 1-µF capacitor, C2. C2 provides the surge current required from V_{DD} during low-side MOSFET turn on in addition to stabilizing the V_{DD} regulation circuit. Finally, 1-µF capacitors should be connected directly across each half-bridge from high-side drain to low-side source. This will minimize or eliminate the ringing seen on the MOSFET gate signals and noise generated by high switching speeds.



Component Placement



Top Copper



Bottom Copper

Figure 6.

PC Board Layout

Figure 6 shows the board layout of the basic H-bridge circuit. The board is double sided FR4 and measures 2.05" by 1.38". There are a couple of issues that need to be stressed when designing the PC board.

Decoupling Capacitors - Care must be taken in the placement and connection of the decoupling capacitors. The capacitor should be placed physically close to the device being decoupled. The connections should be direct and as short as possible. When decoupling a pin on an integrated circuit, connect the capacitor directly from the pin being decoupled to the ground pin of the IC. When decoupling a MOSFET half-bridge, connect the capacitor directly from the drain of the high-side MOSFET to the Source of the low-side MOSFET.

Power and Ground Traces - The traces carrying the motor current should be kept separate from the power traces of devices carrying signal level currents. This will minimize noise due to the high level currents drawn by a motor load. Do not use power or ground plane for this purpose. Also, make certain that these traces are made wide enough to minimize the voltage drop created by the motor current.

Heat Transfer and LITTLE FOOT - Surface mount power MOSFETs rely on the PC board to serve as a heat sink. Wide traces should be connected to the Drain pins of the power MOSFETs to draw heat away from their packages and transfer the heat into the PC board. These traces should be at least 0.1" wide.

Conclusion

By separating the controller and the power MOSFETs, the Si9978DW yields a good balance between circuit integration, compact H-bridge size and flexibility in application. The controller functions are highly integrated, leaving only a few external passive components. The integration makes it easy to use n-channel LITTLE FOOT which are electrically, volumetrically, and economically efficient. Also, since they are separate from the controller, the MOSFETs can be matched to the load. The Si9978DW, combined with LITTLE FOOT, gives compact, flexible H-bridge drive circuits for dc motor control.

3-Phase Brushless DC Motor Controller

Features

- Hall-Effect Commutation
- 60° or 120° Sensor Spacing
- Integral High-Side Drive for all N-Channel MOSFET Bridges
- PWM Input
- Quadrature Selection
- Tachometer Output
- Reversible
- Braking
- Output Enable Control
- Cross Conduction Protection
- Current Limiting
- Undervoltage Lockout
- Internal Pull-Up Resistors

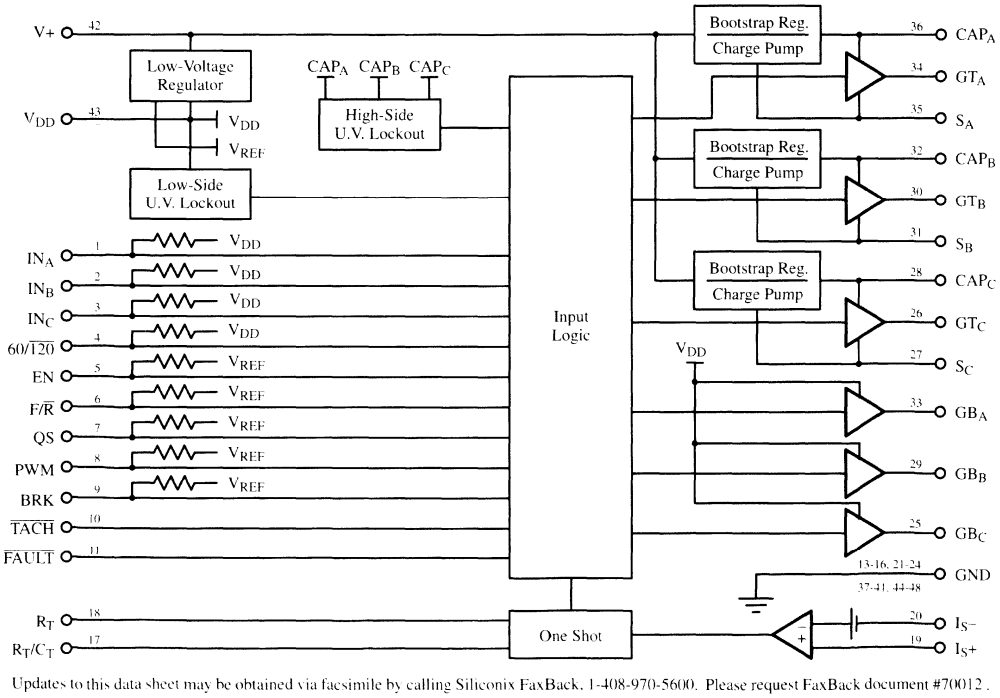
Description

The Si9979CS is a monolithic brushless dc motor controller with integral high-side drive circuitry. The Si9979 is configured to allow either 60°or 120° commutation sensor spacing. The internal low-voltage regulator allows operation over a wide input voltage range, 20- to 40-V dc.

The Si9979CS provides commutation from Hall-effect sensors. The integral high-side drive, which utilizes combination bootstrap/charge pump supplies, allows implementation of an all n-channel MOSFET 3-phase bridge. PWM, direction, quadrature select, and braking inputs are included for control along with a tachometer output. Protection features include cross conduction protection, current limiting, and undervoltage lockout. The $\overline{\text{FAULT}}$ output indicates when undervoltage, over current, disable, or invalid sensor shutdown has occurred.

The Si9979CS is specified to operate over the commercial (0°C to 70°C) temperature range.

Functional Block Diagram



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Absolute Maximum Ratings

Voltage on Pin 42 ..... 50 V
Voltage on Pins 1–4, 10, 11 ..... –0.3 V to V_{DD} + 0.3 V
Voltage on Pins 5–9 ..... –0.3 V to 5.5 V
Voltage on Pins 26, 28, 30, 32, 34, 36 ..... 60 V
Voltage on Pins 27, 31, 35 ..... –2 to 50 V

Operating Temperature ..... 0 to 70°C
Storage Temperature ..... –65 to 150°C
Junction Temperature (T_J) ..... 150°C
Power Dissipation (P_D) ..... 0.7 W

Recommended Operating Range

V+ ..... +20 to 40 V_{DC}
R_T ..... 10 kΩ Min

Specifications

Parameter	Symbol	Specific Test Conditions V+ = 20 to 40 V	Limits C Suffix: 0 to 70°C Min[a]	Typ[b]	Max[a]	Unit
Power						
Supply Voltage Range	V+		20		40	V
Logic Voltage	V_{DD}	–20 mA ≤ I_{DD} ≤ 0 mA	14.5	16	17.5	
Supply Current	I+	I_{DD} = 0 mA		4.5		mA
Logic Current	I_{DD}		–20			
Commutation Inputs (IN_A, IN_B, IN_C, 60/$\overline{120}$)						
High-State	V_{IH}		4.0			V
Low-State	V_{IL}				1.0	
High-State Input Current	I_{IH}	V_{IH} = V_{DD}			10	µA
Low-State Input Current	I_{IL}	V_{IL} = 0 V		–50		
Logic Inputs (F/$\overline{R}$, EN, QS, PWM, BRK)						
High-State	V_{IH}		2.0			V
Low-State	V_{IL}				0.8	
High-State Input Current	I_{IH}	V_{IH} = 5.5 V			10	µA
Low-State Input Current	I_{IL}	V_{IL} = 0 V		–125		
Outputs						
Low-Side Gate Drive, High State	V_{GBH}		14	16	17.5	V
Low-Side Gate Drive, Low State	V_{GBL}				0.1	
High-Side Gate Drive, High State	V_{GTH}			16	18	
High-Side Gate Drive, Low State	V_{GTL}				0.1	
Low-Side Switching, Rise Time	t_{rL}	Risetime = 1 to 10 V Falltime = 10 to 1 V C_L = 600 pF		70		ns
Low-Side Switching, Fall Time	t_{fL}			25		
High-Side Switching, Rise Time	t_{rH}			100		
High-Side Switching, Fall Time	t_{fH}			40		
Break-Before-Make Time	t_{BLH}			100		
	t_{BHL}			300		
$\overline{TACH}$ Output/$\overline{FAULT}$ Output	V_{OL}	I_{OL} = 1.0 mA		0.15	0.4	V
$\overline{TACH}$ Output Pulsewidth	t_T		300	600		ns

Specifications

Parameter	Symbol	Specific Test Conditions V+ = 20 to 40 V	Limits C Suffix: 0 to 70°C Min[a]	Typ[b]	Max[a]	Unit
Protection						
Low-Side Undervoltage Lockout	UVLL			12.2		V
Low-Side Hysteresis	V_H			0.8		
High-Side Undervoltage Lockout	UVLH	$S_{A, B, C}$ = 0 V		V_{DD} – 3.3		
Current Limit						
Comparator Input Bias Current	I_{IB}		–5			µA
Comparator Threshold Voltage	V_{TH}		90	100	110	mV
Common Mode Voltage	V_{CM}		0		1	V
One Shot Pulse Width	t_p	R_T = 10 k C_T = 0.001 µF	8	10	12	µs
		R_T = 10 k C_T = 0.01 µF	80	100	120	

Notes
a. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum.
b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

Commutation Truth Table

Inputs										Outputs							Conditions
Sensors (60°Spacing)			Sensors (120°Spacing)							Top Drive			Bottom Drive				
IN_A	IN_B	IN_C	IN_A	IN_B	IN_C	EN	F/$\overline{R}$	BRK	I_S+	GT_A	GT_B	GT_C	GB_A	GB_B	GB_C	$\overline{FAULT}$	
0	0	0	1	0	1	1	1	0	0	1	0	0	0	1	0	1	
1	0	0	1	0	0	1	1	0	0	1	0	0	0	0	1	1	
1	1	0	1	1	0	1	1	0	0	0	1	0	0	0	1	1	
1	1	1	0	1	0	1	1	0	0	0	1	0	1	0	0	1	
0	1	1	0	1	1	1	1	0	0	0	0	1	1	0	0	1	
0	0	1	0	0	1	1	1	0	0	0	0	1	0	1	0	1	
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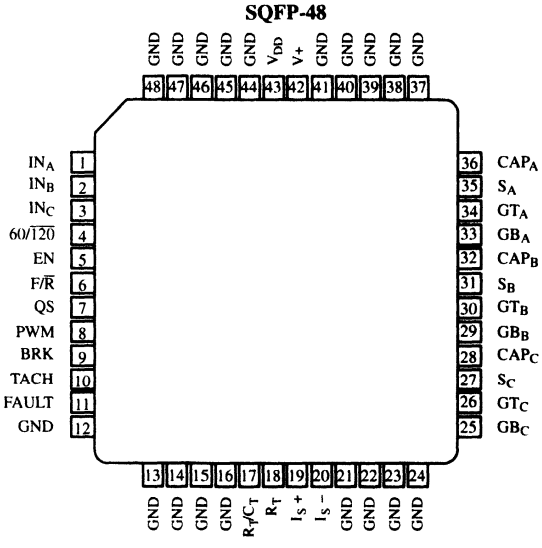
1	0	0	1	0	0	1	0	0	0	0	0	1	1	0	0	1	
1	1	0	1	1	0	1	0	0	0	0	0	1	0	1	0	1	
1	1	1	0	1	0	1	0	0	0	1	0	0	0	1	0	1	
0	1	1	0	1	1	1	0	0	0	1	0	0	0	0	1	1	
0	0	1	0	0	1	1	0	0	0	0	1	0	0	0	1	1	
X	X	X	X	X	X	0	X	0	X	0	0	0	0	0	0	0	Disable
X	X	X	X	X	X	0	X	1	X	0	0	0	1	1	1	0	Power Down
L	L	L	L	L	L	1	X	1	0	0	0	0	1	1	1	1	Brake
L	L	L	L	L	L	1	X	1	1	0	0	0	1	1	1	0	Over I in BRK
L	L	L	L	L	L	1	X	0	1	0	0	0	0	0	0	0	Over I
1	0	1	1	1	1	1	X	0	X	0	0	0	0	0	0	0	
1	0	1	1	1	1	1	X	1	X	0	0	0	1	1	1	0	
0	1	0	0	0	0	1	X	0	X	0	0	0	0	0	0	0	
0	1	0	0	0	0	1	X	1	X	0	0	0	1	1	1	0	

Notes: L. Any valid sensor combination
X. Don't care

Pin Configuration



Top View

Pin Description

Pins 1–3: IN_A, IN_B, IN_C

IN_A, IN_B, and IN_C are the commutation sensor inputs, and are intended to be driven by open collector Hall effect switches. These inputs have internal pull up resistors tied to V_{DD}, which eliminates the need for external pull up resistors.

Pin 4: 60/$\overline{120}$

The 60/$\overline{120}$ input allows the use of the Si9979 with either a 60° or 120° commutation sensor spacing. An internal pull up resistor, which is tied to V_{DD}, sets the default condition to 60° spacing. 120° spacing is selected by pulling this input to ground.

Pin 5: EN (Enable)

A logic "1" on this input allows commutation of the motor. This is the default condition as this pin is pulled up internally. When this pin is pulled to ground, all gate drive outputs are turned off.

Pin 6: F/$\overline{R}$ (Forward/Reverse)

A logic "1" on this input selects commutation for motor rotation in the "forward" direction. This is the default condition as this pin is pulled up internally. When this pin is pulled to ground, the commutation sensor logic levels are inverted internally, causing reverse rotation.

Pin 7: QS (Quadrature Select)

This input determines whether the bottom MOSFETs or both bottom and top MOSFETs switch in response to the PWM signal. A logic "1" on this input enables only the bottom MOSFETs. This is the default condition as this pin is pulled up internally. When this pin is pulled to ground, both the bottom and top MOSFETs are enabled.

Pin 8: PWM

An open collector (drain) or TTL compatible signal is applied to this input to control the motor speed. The QS input determines which MOSFETs are switched in response to the PWM signal. If no PWM signal is being used, this input is left open. It is pulled up internally, which allows the MOSFETs to follow the commutation sequence.

Pin Description (Cont'd)

Pin 9: BRK

With this input at logic "1", the top MOSFETs are turned off and the bottom MOSFETs are turned on, shorting the motor windings together. This provides a braking torque which is dependent on the motor speed. This is the default condition as this pin is pulled up internally. When this pin is pulled to ground, the MOSFETs are allowed to follow the commutation sequence.

Pin 10: $\overline{\text{TACH}}$

This output provides a minimum 300-nanosecond output pulse for every commutation sensor transition, yielding a 6 pulse per electrical revolution tachometer signal. This output is open drain.

Pin 11: $\overline{\text{FAULT}}$

The $\overline{\text{FAULT}}$ output switches low to indicate that at least one of the following conditions exists, controller disable ($\overline{\text{EN}}$), undervoltage lockout, invalid commutation sensor code shutdown, or overcurrent shutdown. This output is open drain.

Pin 17: R_T/C_T

The junction of the current limit one shot timing resistor and capacitor is connected to this pin. This one-shot is triggered by the current limit comparator when an overcurrent condition exists. This action turns off all the gate drives for the period defined by R_T and C_T, thus stopping the flow of current.

Pin 18: R_T

One side of the current limit one shot timing resistor is connected to this pin.

Pin 19: I_S+

This is the sensing input of the current limit comparator and should be connected to the positive side of the current sense resistor. When the voltage across the current sense resistor exceeds 100 mV, the comparator switches and triggers the current limit one-shot. The one-shot turns off all the gate drives for the period defined by R_T and C_T, thus stopping the flow of current. If the overcurrent condition remains after the shutdown period, the gate drives will be held off until the overcurrent condition no longer exists.

Pin 20: I_S-

This pin is the ground reference for the current limit comparator. It should be connected directly to the ground side of the current sense resistor to enhance noise immunity.

Pins 12–16: 21–24, 37–41, 44–48, GND

These pins are the return path for both the logic and gate drive circuits. Also, they serve to conduct heat out of the package, into the circuit board.

Pin 25: GB_C

This is the gate drive output for the bottom MOSFET in Phase C.

Pin 26: GT_C

This is the gate drive output for the top MOSFET in Phase C.

Pin 27: S_C

This pin is negative supply of the high-side drive circuitry. As such, it is the connection for the negative side of the bootstrap capacitor, the top MOSFET Source, the bottom MOSFET Drain, and the Phase C output.

Pin 28: CAP_C

This pin is the positive supply of the high-side circuitry. The bootstrap capacitor for Phase C is connected between this pin and SC.

Pin 29: GB_B

This is the gate drive output for the bottom MOSFET in Phase B.

Pin 30: GT_B

This is the gate drive output for the top MOSFET in Phase B.

Pin 31: S_B

This pin is negative supply of the high-side drive circuitry. As such, it is the connection for the negative side of the bootstrap capacitor, the top MOSFET Source, the bottom MOSFET Drain, and the Phase B output.

Pin Description (Cont'd)

Pin 32: CAP_B

This pin is the positive supply of the high-side circuitry. The bootstrap capacitor for Phase B is connected between this pin and SB.

Pin 33: GB_A

This is the gate drive output for the bottom MOSFET in Phase A.

Pin 34: GT_A

This is the gate drive output for the top MOSFET in Phase A.

Pin 35: S_A

This pin is negative supply of the high-side drive circuitry. As such, it is the connection for the negative side of the bootstrap capacitor, the top MOSFET Source, the bottom MOSFET Drain, and the Phase A output.

Pin 36: CAP_A

This pin is the positive supply of the high-side circuitry. The bootstrap capacitor for Phase A is connected between this pin and SA.

Pin 42: V+

The supply voltage for the Si9979 is connected between this pin and ground. The internal logic and high-side supply voltages are derived from V+.

Pin 43: V_{DD}

V_{DD} is the internal logic and gate drive voltage. It is necessary to connect a capacitor between this pin and ground to insure that the current surges seen at the turn on of the bottom MOSFETs does not trip the undervoltage lockout circuitry.

Applications

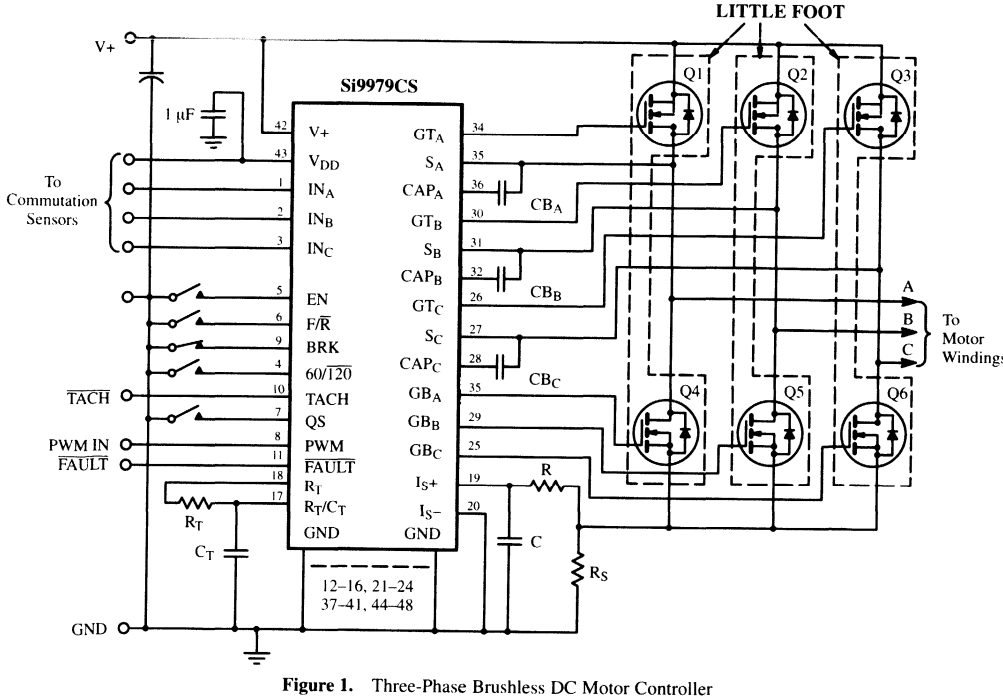


Figure 1. Three-Phase Brushless DC Motor Controller

Applications (Cont'd)

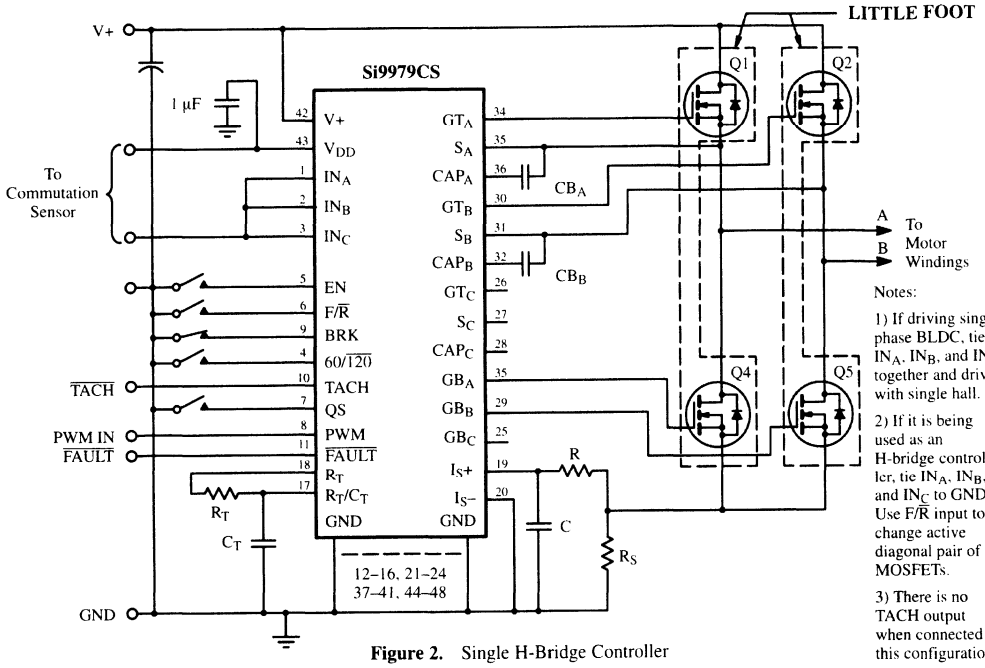


Figure 2. Single H-Bridge Controller

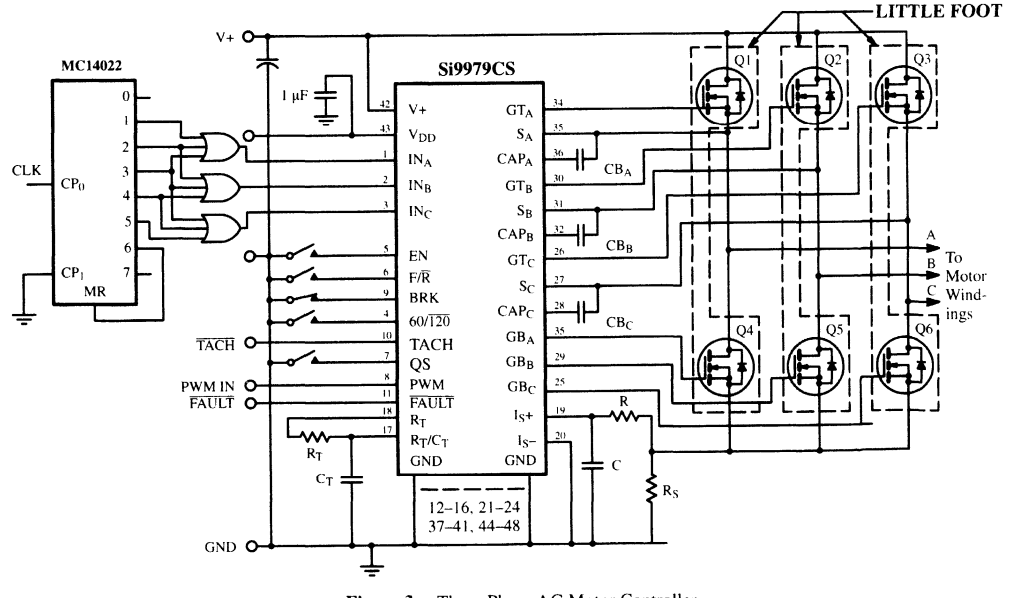


Figure 3. Three-Phase AC Motor Controller

Applications (Cont'd)

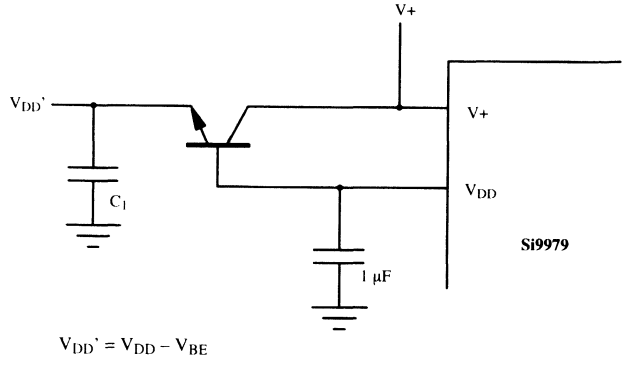


Figure 4. External V_{DD} Regulator

A Compact Controller for Brushless DC Motors

Wharton McDaniel

The drive electronics for 3-phase brushless dc motors often occupy a surprising amount of space. Complex circuitry is needed to drive the power MOSFETs, and this gets even more complex in applications above 15 V. Above 15 V, level shifted circuitry is required for proper drive of the high-side MOSFETs, whether they are n-channel or p-channel. Add to this the possible need for heat sinks. Even when the $r_{DS(on)}$ of the MOSFETs is low enough to eliminate the requirement for heatsinking, the MOSFETs' package size will require a lot of board area or headroom above the PC board surface. The Si9979 brushless dc controller eliminates much of this complexity for applications in the 20- to 40-V dc range. Housed in a 7-mm SQFP package, the Si9979 reduces assembly cost and simplifies both motor and electronics packaging.

The Si9979 is a monolithic controller with integral high-side drive circuitry, allowing easy implementation of an all-n-channel three-phase bridge. The commutation logic has been configured to work with either 60° or 120° commutation sensor spacing. The internal voltage regulator allows the Si9979 to operate over a wide input voltage range, 20 to 40 V dc, and to power the commutation sensors over this same range. Control inputs include direction, quadrature select, PWM, and braking. A tachometer output is also featured. Protection features include cross-conduction protection, current limiting, and undervoltage lockout. The $\overline{\text{FAULT}}$ output indicates when undervoltage, overcurrent, disable, or invalid sensor shutdown has occurred.

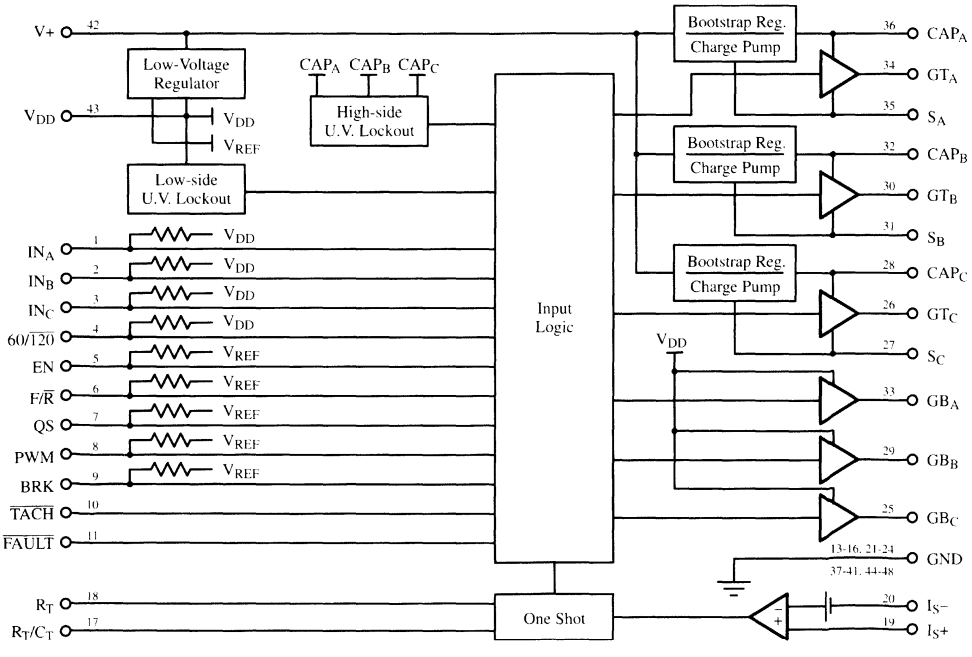


Figure 1. Si9979 Functional Block Diagram

Updates to this app note may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70585.

Functional Description

Functionally the Si9979 is made up of the commutation logic, the gate drive outputs, V_{DD} regulator and output, and protection circuitry.

Commutation Logic

The commutation logic generates the basic commutation signals from the commutation sensors and modifies those signals according to the control inputs EN, F/R, PWM, QS, and BRK.

Commutation Inputs

The basic commutation signals are generated from the code provided by the commutation sensors connected to IN_A, IN_B, and IN_C. These inputs are designed to be driven from open collector Hall Effect switches and have active pull ups to V_{DD}. The 60/120 input must be set to be compatible with the sensor spacing used. It also has an active pull-up to V_{DD}, with the default condition being 60-degree spacing. Figure 1 gives the basic timing for both 60-degree and 120-degree commutation.

Control Inputs

The control inputs EN, F/$\overline{R}$, PWM, QS, and BRK are TTL compatible inputs with internal pull-ups. TTL compatibility allows easy interface with microcontrollers and other common logic devices. Functions are divided as follows: EN input enables the outputs, F/R determines the direction of the motor's rotation, PWM accepts a digital pulse width modulation signal for controlling the motor's speed, QS determines whether bottom only or bottom and top MOSFETs are chopped by the PWM signal, and BRK breaks the motor by turning on all the bottom MOSFETs. The default conditions are EN - enabled, F/$\overline{R}$ - forward rotation, PWM - no chopping on active gate drives, QS - only bottom MOSFETs chopped by PWM, and BRK - braking function on.

$\overline{\text{TACH}}$ Output

This output is an extension of the commutation logic. When one of the commutation sensors changes state, a negative going pulse is emitted (500 ns typical). This gives six pulses per electrical revolution. The output is configured as an open drain for easy interfacing.

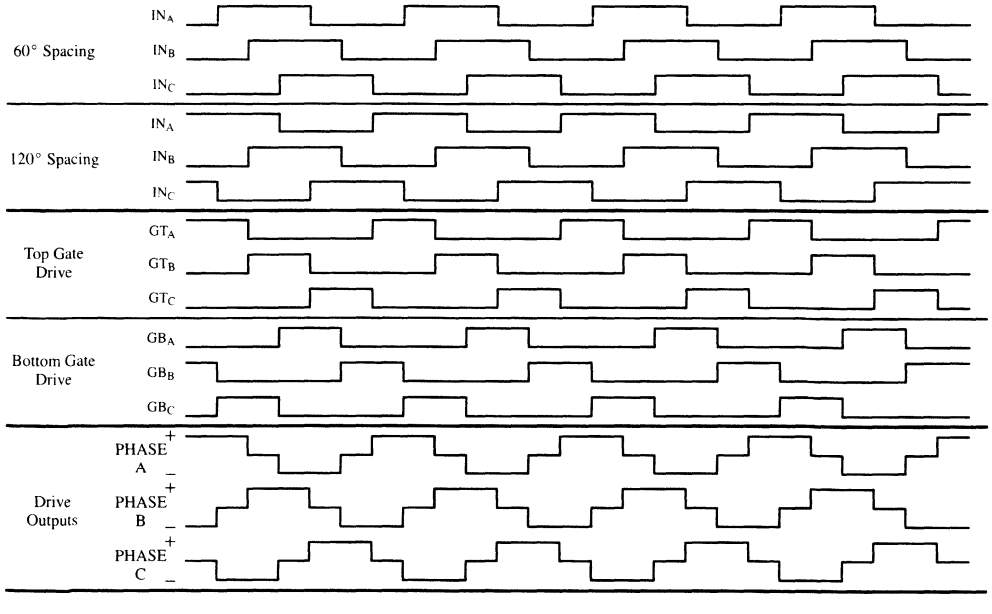


Figure 2. Basic Timing for Both 60° and 120° Commutation

Gate Drive Outputs

Each phase or half-bridge output is driven by a pair of n-channel MOSFETs. These are controlled by a low- and a high-side gate driver. They have been designed to drive a 600-pF load with a 110-ns rise time and a 50-ns fall time.

The low-side gate is driven directly from the commutation logic and is powered by V_{DD}. This means that V_{DD} must be decoupled with a 1-µF capacitor; otherwise the turn-on surge current can cause V_{DD} to drop to the level of an undervoltage condition.

The high side is a floating circuit powered from a combination bootstrap/charge pump supply. The bootstrap capacitor is charged to V_{DD} when ever the low-side MOSFET is turned on. For the rest of the time, the charge pump keeps the bootstrap capacitor charged, replacing the charge used in powering the high-side circuitry and in turning on the MOSFET. The value of the bootstrap capacitor is a function of the MOSFET being driven. The bootstrap voltage should not drop more than 1 V as the result of a MOSFET turn-on. For a 50-V dual n-channel MOSFET like the Si9940DY, 30 nC (Qg) is required for turn-on at a V_{GS} of 10 V. Using the equation $C = Q_g/V_{GS}$, 3 nF is required to provide sufficient charge for turn-on. To meet the criteria of dropping only 1 V at turn-on, the capacitor needs to be 10 times as large, making the equation $C_{BOOT} = 10(Q_g/V_{GS})$. This makes the minimum value of C_{BOOT} equal to 0.03 µF. Table 1 gives minimum recommended values for several MOSFETs that might be used with the Si9979. This minimum recommended value is one standard value above the minimum calculated value.

V_{DD} Regulator and Output

The regulation circuitry of the Si9979 has been sized to source 20 mA to power the commutation sensors. When the operating ambient temperature rises to 70°C, the input voltage (V+) must be limited to 32 V dc.

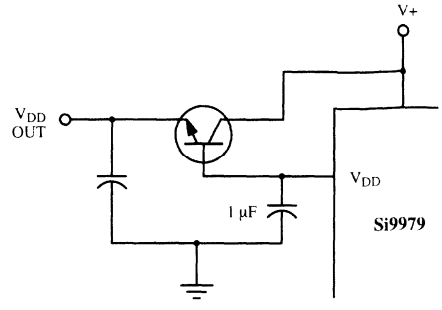


Figure 3. External V_{DD} Regulator

Otherwise the Si9979 may overheat. In cases where this condition cannot be met, or where more current is required, an external series pass NPN can be added as shown in Figure 3.

Protection Circuitry

The protection circuitry provides current limit, cross-conduction protection, undervoltage lockout, and the $\overline{\text{FAULT}}$ output.

Current Limit

The current limit circuitry consists of a comparator driving a one-shot multivibrator (Figure 4). The comparator has an internal 100-mV reference voltage on the inverting input and an external sensing resistor connected to the noninverting input. These inputs should be connected directly to the sensing resistor. This will eliminate the effects of any noise in the ground traces. The motor current must generate 100 mV across a sensing resistor for the comparator to trip. This in turn triggers the one-shot, turning off the active MOSFETs for a period defined by the product of RT and CT.

Table 1. Bootstrap Capacitor Selection

Part Number	$r_{DS(on)}$	Qg @ V_{GS} = 10 V (nC)	Minimum Recommended C_{BOOT} (µF)
Si9940	0.05	30	0.039
Si9945	0.10	15	0.018
Si9955	0.13	8	0.01
Si9959	0.30	4.7	0.0056

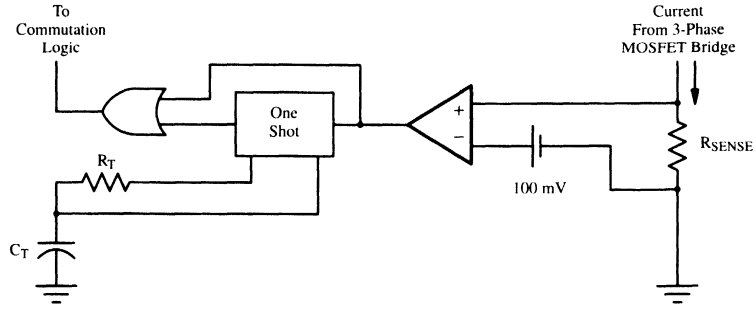


Figure 4. Current Limit Circuitry

If the current has dropped below the threshold by the time the off period has expired, the MOSFETs will be turned on again. If the overcurrent condition remains after the off period has expired, the MOSFETs will be held off until the current drops below the threshold.

With the current limit off period in the 100-µs range, cycle-by-cycle current limiting is achieved. If the current limit off period is reduced to the 10-µs range, a constant current mode current limit is achieved. In this mode, the RMS current (and therefore the torque) is maximized for the current limit setting. This is particularly useful when a maximum acceleration rate is required at power on. Figure 5 shows typical current waveforms for durations of the off period.

Cross Conduction Protection

When driven in the anti-phase mode, the high-side and low-side MOSFETs of each active phase are toggled. To prevent shoot-through, each half-bridge has break-before-make circuitry. This delays the MOSFET turn for 250 ns from the turn off of the opposite MOSFET.

Undervoltage Lockout

Internal circuitry monitors the voltage level on V_{DD} and the high-side supplies. This ensures that there is sufficient voltage to turn on the MOSFETs. Should the voltage level on V_{DD} drop below a nominal 12.2 V, all gate drives will be turned off until the undervoltage condition is gone. Each of the high-side supplies is monitored only when it is referenced to ground. If the high-side voltage is under a nominal 12.7 V, the high-side will not be allowed to turn on.

$\overline{\text{FAULT}}$ Output

A negative going transition indicates that an undervoltage, current limit, or invalid sensor code condition exists. This output is configured as an open drain.

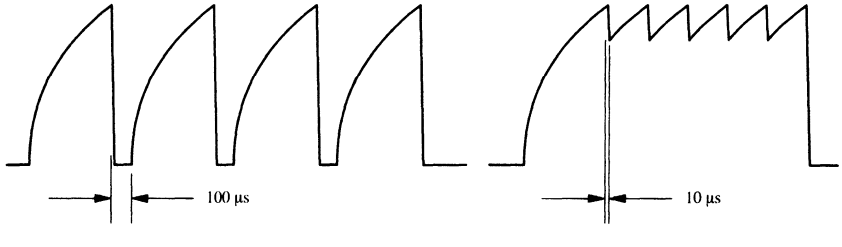
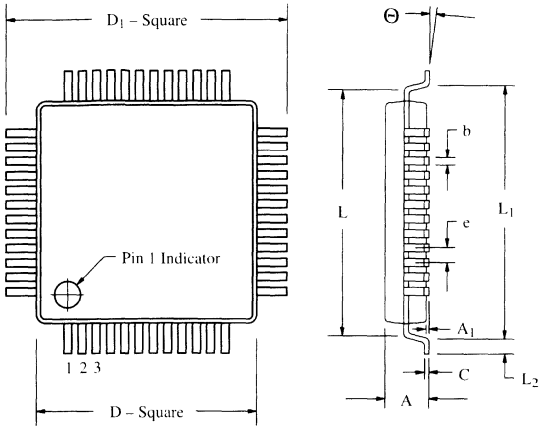


Figure 5. Current Waveforms



Dim	Millimeters		Inches*	
	Min	Max	Min	Max
A	1.35	1.60	0.053	0.063
A_1	0.04	0.16	0.002	0.006
b	0.14	0.26	0.006	0.010
C	0.117	0.177	0.005	0.007
D	6.90	7.10	0.272	0.280
D_1	8.70	9.30	0.343	0.366
e	0.40	0.60	0.016	0.024
L	–	7.80	–	0.307
L_1	7.80	8.20	0.307	0.323
L_2	0.30	0.70	0.012	0.028
Θ	0°	7°	0°	7°

*For Reference Only

Figure 6. 48-Pin SQFP Package

The Package

The Si9979 was packaged in a 48-pin SQFP to make drive circuits as compact as possible. The package has a 7-mm body with a total footprint of 9.3 mm on a side, occupying 86.5 mm^2. The package dimensions are given in Figure 6. Beyond the basic footprint, the ground pins of the package should be connected to copper. This will help transfer heat out of the package and in to the PC board (Figure 7). Heat dissipation is especially important when the internal regulator is used to supply the current to the commutation sensors.

A 3 Phase Brushless DC Drive

Figure 8 shows a typical 3-phase brushless dc drive circuit. Designers should consider both the motor being driven and any conditions imposed by the system when selecting the values of the current sense resistor, the R/C for the current limit one-shot, and the bootstrap capacitor, as well as the actual MOSFETs.

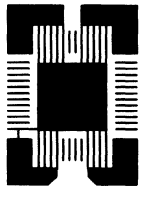


Figure 7. Pad Pattern with Heat Sinking Copper (2)

Motor Definition

The motor being driven will be operated at 24 V dc. The typical load current is 2 A. The starting current must be limited to 5-A peak because of a system power supply limitation. It will take five seconds for the motor to accelerate the load to speed.

The Commutation Sensor Interface

Most brushless dc motors use Hall effect switches with open collector outputs. These can be connected directly to IN_A, IN_B, and IN_C. However, there are some motors which use Hall effect sensors with differential outputs. These are not compatible with the commutation inputs on the Si9979. The circuit in Figure 9 is an example of how differential output Hall sensors can be interfaced to the single ended inputs of the Si9979.

The Current Sense Resistor

The current limit level is determined by the motor starting requirements, such as acceleration time, the power capability of the power MOSFETs, and the capability of the system power supply to supply current to the motor. For this design, the current limit level will be set at 5 A peak. There is a simple way to set this level. Select a sensing resistor which will give 100 mV when 5 A flows through it. Using Ohm's law, RS = 100 mV/IPK. Therefore a 20-mΩ resistor is required. A 0.5-W resistor will handle the starting condition, since it is a transient condition. At the load current of 2 A, power dissipation is less than 0.10 W.

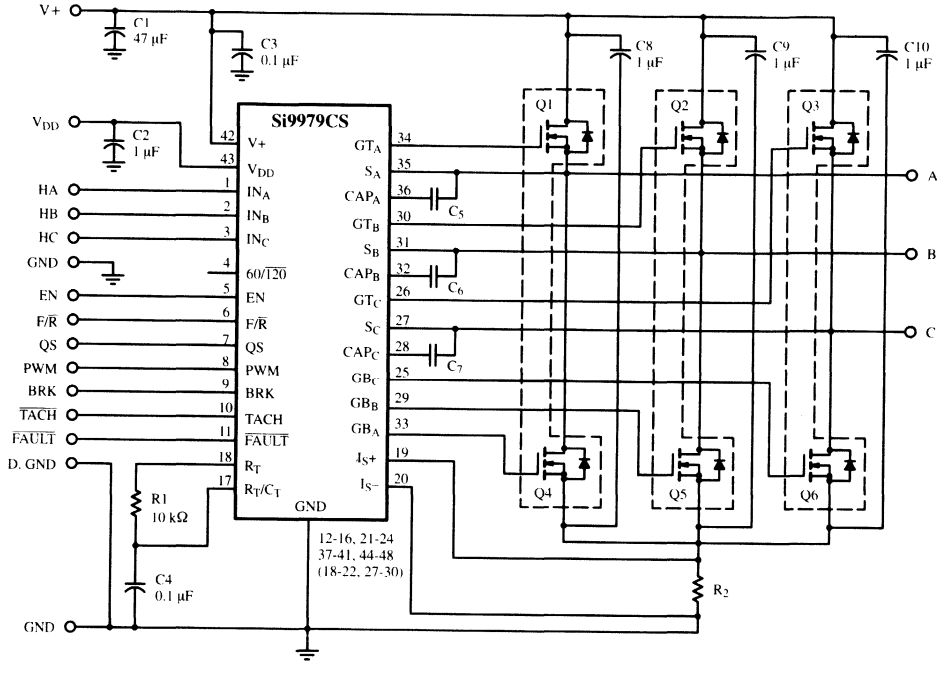


Figure 8. Three-Phase Brushless DC Motor Controller

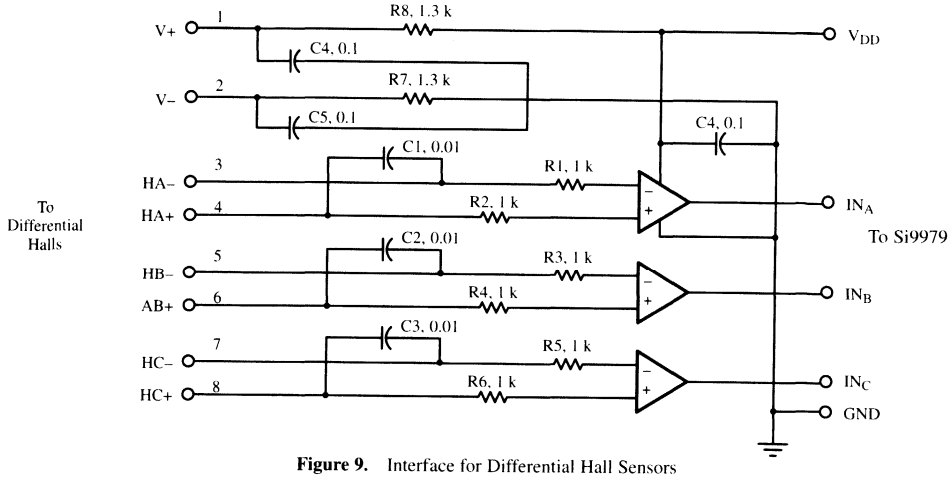


Figure 9. Interface for Differential Hall Sensors

There are alternative ways of setting current limits which use standard resistors to adjust the level. The first method is to use a resistive divider (Figure 10). This forces the voltage drop across the sensing resistor to be greater than 100 mV, so 100 mV can be achieved at Is+. If this method is used to get the 5-A level, R_{SENSE} should be selected at 50 mΩ. A current of 5 A will generate a 250-mV drop across RS. Then select values for R1 and R2 to divide this by 2.5, applying 100 mV to IS+. Setting R1 to 4.2 kΩ and R2 to 6.2 kΩ provides this division. This adjustability is gained at the cost of increasing the power rating of the sensing resistor to 1.5 W.

Another way to get an adjustable current limit level is to bias the IS- pin up from ground (Figure 11). This raises the threshold from 100 mV to 100 mV + VBias. With the 50-mΩ sense resistor, 150 mV of bias needs to be applied to IS- to raise the threshold to the 250-mV level required for a 5-A current limit. The bias voltage must be kept under 0.8 V to ensure the input is not damaged. As in the resistive divider method, this method forces the increase in the sense resistor's power rating. Also, the stability of the threshold voltage is affected by the stability of the bias voltage.

Current Limit One-Shot Timing

If the current limit off time is kept short, acceleration can take place as quickly as possible while respecting the peak starting current of 5 A. The recommended setting is 10 µs. Since this off time is defined by the product of R_T and C_T, R_T is set to 10 kΩ, making C_T equal to 0.001 µF.

The Power MOSFETs

Dc motors demand more current during startup than they do under normal running conditions. As a result, the most important specification for the power MOSFETs is their ability to withstand the starting current. This is especially true when surface-mount devices are involved.

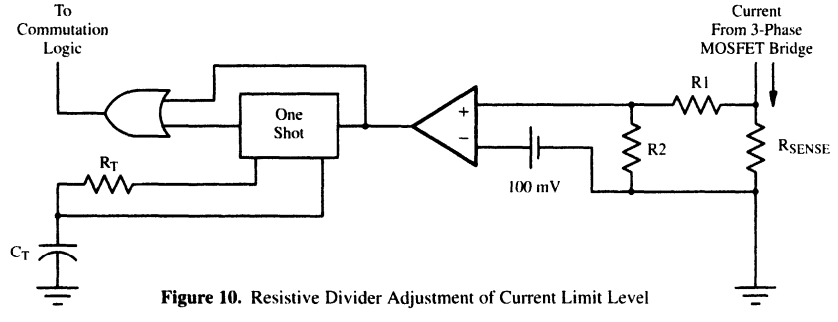


Figure 10. Resistive Divider Adjustment of Current Limit Level

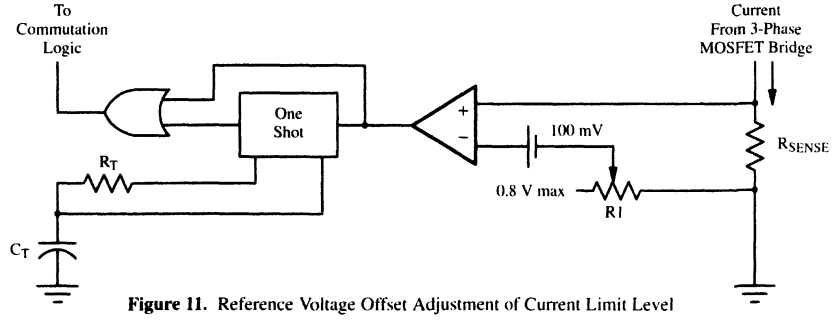


Figure 11. Reference Voltage Offset Adjustment of Current Limit Level

If the current starting level is 5 A, and the current limit circuitry is set for constant current operation, then power dissipation will determine the device chosen.

The Si9940DY LITTLE FOOT® power MOSFET is a good choice for this application. Its worst case on resistance is 85 mΩ. This puts the power dissipation at approximately 1.3 W. With the R_{ja} of 50°C/W, the junction temperature will stay below 150°C in ambient temperatures as high as 85°C.

The Bootstrap Capacitor

The value of the bootstrap capacitor is determined by the gate charge required for the MOSFET selected. The Si9940 requires 30 nC (Qg) at a V_{GS} of 10 V (Figure 12). Using the equation $C_{BOOT} = 10\ (Qg/V_{GS})$, the typical value is 0.03 µF. Table 1 shows a recommended minimum value of 0.039 µF, which provides some headroom.

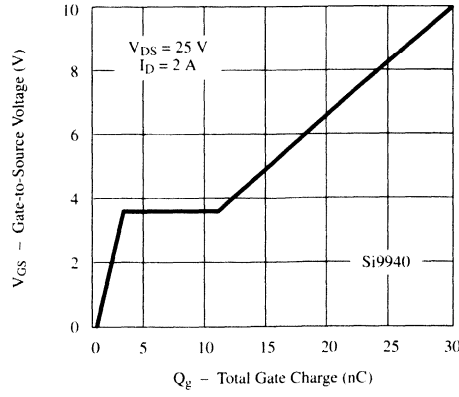


Figure 12.

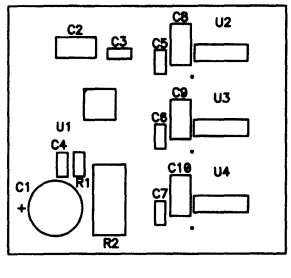
PC Board Layout

Careful attention should be paid to decoupling, to routing of traces that carry the motor current, and to placement of the power MOSFETs. There are several decoupling capacitors in the design. The capacitors that are decoupling IC pins should be placed as close as possible to the pin itself, with the ground side of the capacitor going directly to an IC ground pin. Decoupling of the power bus should occur at the MOSFETs to minimize the surge current in the traces. Separate power and ground traces should be run to eliminate noise generated by fast MOSFET transitions. These traces should be terminated as close as possible to the V+ and GND inputs on the PC board. Wherever separate traces are not feasible, the common trace should be as wide as possible. Wide traces should be connected to the drain pins of the power MOSFETs to draw heat away from their packages. These traces should be at least 0.1" wide.

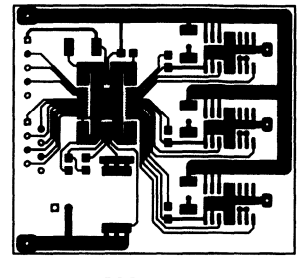
Figure 13 shows a sample PC board layout using the Si9979 with Si9940 MOSFETs. The overall dimensions of this board are 2.1" × 1.85". This size board can be mounted directly on a motor.

Conclusion

Drive circuitry can be made more compact when high levels of integration are combined with surface-mount packaging. The PC board layout shown below is small enough to be mounted directly on a motor. This keeps the motor leads short and minimizes the switching noise associated with long motor leads. LITTLE FOOT MOSFETs help minimize the board area while allowing the designer to tailor the design to the motor being driven. Combined with the Si9979, the result is a compact, all-surface-mount solution allowing fully automated assembly.



a) Component Placement



b) PC Board Layout

Figure 13.

12-V Voice Coil Motor Driver

Features

- 1.8-A H-Bridge Output
- Class B Linear Operation
- Externally Programmable Gain and Bandwidth
- Undervoltage Head Retract
- Programmable Retract Current
- Low Standby Current
- Rail-to-Rail Output Swing
- Single 12-V Supply
- System Voltage Monitor with Fault Output

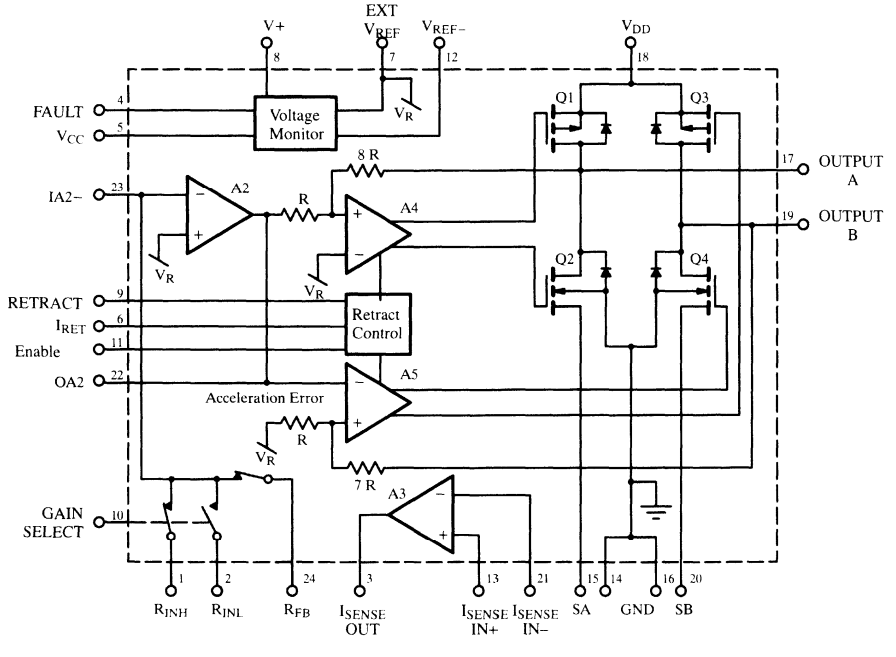
Description

The Si9961 is a linear actuator (voice coil motor) driver suitable for use in disk drive head positioning systems. The Si9961 contains all of the power and control circuitry necessary to drive the VCM that is typically found in $3^1/_2$-inch hard disk drives and optical disk drives. The driver is capable of delivering 1.8 A at a nominal supply of 12 V.

The Si9961 provides all necessary functions including a motor current sense amplifier, a loop compensation amplifier and a power amplifier featuring four complementary MOSFETs in a H-bridge configuration. The output crossover protection ensures no cross-conducting current and true Class B operation during linear tracking. Externally programmable gain switch at the input summing junction increases the resolution and dynamic range for a given DAC. The head retract circuitry can be activated by either an undervoltage condition or an external command. An external resistor is required to set the VCM current during retract.

The Si9961 is constructed on a self-isolated BiC/DMOS power IC process. The IC is available in 24-pin SO package for operation over the commercial, C suffix (0 to 70°C) temperature range.

Functional Block Diagram



Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70014.

Absolute Maximum Ratings

Voltages Referenced to Common Pin
V+ Supply Range ..... –0.3 V to 16 V
Pin ($\overline{FAULT}$) ..... –0.3 V to V_{CC} + 0.3 V
Pin (Output A & B, Source A & B) ..... –0.3 V to V_{DD} + 0.3 V
Pin (All Others) ..... –0.3 V to V+ + 0.3 V
Maximum Clamp Current
Output A, Output B (Pulsed 10 ms at 10% duty cycle) ..... ± 1.8 A
Pin (All Others) ..... ± 20 mA
Storage Temperature ..... –65 to 150°C
Operating Temperature ..... 0 to 70°C
Junction Temperature (T_J) ..... 150°C
Power Dissipation (Package)[a]
24-Pin SOIC[b] ..... 3.125 W
Thermal Impedance (Θ_{JA})[a]
24-Pin SOIC ..... 40°C/W

Notes
a. Device mounted with all leads soldered or welded to PC board.
b. Derate 25 mW/°C above 25°C.

Specifications

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 12 V ± 10%, V_{DD} = 11.6 V ± 10% V_{CC} = 5 V ± 10%, V_{REF-} = GND = 0 V V_{REF} = 5 V ± 5%	Limits C Suffix 0 to 70°C Min[b]	Typ[a]	Max[b]	Unit
Bridge Outputs (A_4, A_5)						
High Level Output Voltage	V_{OH}	I_{OH} = 1.0 A, V_{DD} = 10.2 V, OA_2= V_{REF} ± 1 V	8.0	9.1		V
Low Level Output Voltage	V_{OL}	I_{OL} = –1.0 A, OA_2 = V_{REF} ± 1 V		0.6	1.1	
Clamp Diode Voltage	V_{CL}	I_F = 1.0 A, $\overline{ENABLE}$ = High			2.5	
Amplifier Gain		Output V_{RANGE} = V_{REF} ± 2 V	12	16	18	V/V
Dynamic Crossover Current		Measured at V_{DD}		10		mA
Slew Rate	SR		1			V/µS
Small Signal Bandwidth (–3 dB)				0.2		MHz
Input Deadband			–60		60	mV
A_2, Loop Compensation Amplifier						
Input Offset Voltage	V_{OS}		–8		8	mV
Input Bias Current	I_B	Gain Select = High, IA_2^- = 5 V	–50		50	nA
Unity Gain Bandwidth		R_{LOAD} = 10 kΩ, C_{LOAD} = 100 pF to V_{REF}		1		MHz
Slew Rate	SR		1			V/µs
Power Supply Rejection Ratio	PSRR	@ 10 kHz		50		dB
Open Loop Voltage Gain	A_{VOL}			80		
Output Voltage Swing	V_O	R_{LOAD} = 10 kΩ to V_{REF}	V_{REF} –2		V_{REF} +2	V
A_3, Current Sense Amplifier						
Input Offset Voltage	V_{OS}		–5		5	mV
Input Impedance	R_{IN}	$I_{SENSE}IN+$ to $I_{SENSE}IN-$		5		kΩ
Small Signal Bandwidth (–3 dB)		R_{LOAD} = 10 kΩ, C_{LOAD} = 100 pF to V_{REF}		1		MHz
Common Mode Rejection Ratio	CMRR	@ 5 kHz		50		dB
Slew Rate	SR		2			V/µs
Gain			3.9	4	4.1	V/V

Specifications

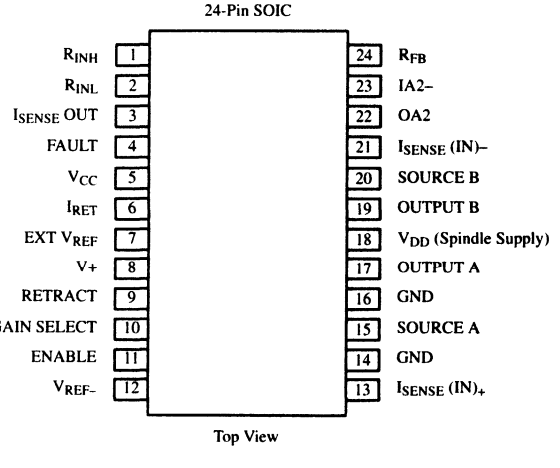
Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 12 V ± 10%, V_{DD} = 11.6 V ± 10% V_{CC} = 5 V ± 10%, V_{REF-} = GND = 0 V V_{REF} = 5 V ± 5%	Limits C Suffix 0 to 70°C Min[b]	Typ[a]	Max[b]	Unit
A_3, Current Sense Amplifier (Cont'd)						
Input Common-Mode Voltage Range	V_{CM}	To GND	–0.3		2	V
Output Voltage Swing	V_O	R_{LOAD} = 10 kΩ, C_{LOAD} = 100 pF to V_{REF}	V_{REF} –2		V_{REF} +2	V
Supply						
Supply Current (Normal)	I_{CC}	Static, No Load			0.01	mA
	I_{V+}	$\overline{RETRACT}$ = High		2	5	mA
	I_{DD}	$\overline{ENABLE}$ = Low		5	13	mA
Supply Current (Standby)	I_{CC}	Static, No Load			0.01	mA
	I_{V+}	$\overline{RETRACT}$ = High		0.2	0.4	mA
	I_{DD}	$\overline{ENABLE}$ = High		0.8	1.6	mA
V_{DD} Range	V_{DD}	Normal Mode	10.2	11.6	13.2	V
		Retract Mode	2.0		14	V
V_{CC} Range	V_{CC}		4.5	5	5.5	V
V+ Range	V+		10.8	12	13.2	V
Gain Select Switch						
R_{FB} Switch Resistance		IA2– = 5 V		108	240	Ω
R_{INH} Switch Resistance				135	300	Ω
R_{INL} Switch Resistance				810	1800	Ω
V_{REF} (EXT)						
Input Current	I_{REF}	OA2 = V_{REF}	0.15	0.40	0.65	mA
External Voltage Range	V_{REF}		4.75	5	5.25	V
Power Supply Monitor						
V_{CC} Undervoltage Threshold		V_{REF} = 5.0 V	3.82	4.12	4.42	V
Hysteresis				40		mV
V+ Undervoltage Threshold		V_{REF} = 5.0 V	9.1	9.8	10.6	V
Hysteresis				100		mV
Gain Select, $\overline{RETRACT}$, $\overline{ENABLE}$ Input						
Input High Voltage	V_{IH}		3.5			V
Input Low Voltage	V_{IL}				1.5	V
Input High Current	I_{IH}	V_{IN} = 5 V	–1		1	µA
Input Low Current	I_{IL}	V_{IN} = 0 V	–1		1	µA

Specifications

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 12 V ± 10%, V_{DD} = 11.6 V ± 10% V_{CC} = 5 V ± 10%, V_{REF-} = GND = 0 V V_{REF} = 5 V ± 5%	Limits C Suffix 0 to 70°C Min[b]	Typ[a]	Max[b]	Unit
$\overline{\text{FAULT}}$ Output						
Output High Voltage	V_{OH}	I_{OH} = –100 µA	V_{CC} –0.8	V_{CC} –0.33		V
Output Low Voltage	V_{OL}	I_{OL} = 1.6 mA		0.25	0.50	
Output High Sourcing Current	I_{OHS}	V_{OUT} = 0 V		400	1100	µA
RETRACT Current Control ($\overline{\text{RETRACT}}$ = Low, Output Current from A to B)						
I_{RET} Bias Voltage	V(I_{RET})	V_{DD} = 10 V, R_{RET} = 3.74 kΩ		0.66		V
Retract Output Pull-Up Voltage	$V_{OUT\,A}$	V_{DD} = 2.5 V to 14 V, I_{OUTA} = 30 mA	V_{DD} –1			
Retract Output Pull-Down Current	I_{OUTB}	V_{DD} = 10 V, V_{OUTB} = 5 V R_{RET} = 3.74 kΩ R_{SB} = 0.5 Ω, T_A = 25°C	22	30	38	mA
Maximum Emergency Retract Current	I_{OUTB} (Max)	V_{DD} = 2 V, V_{OUTB} = 0.7 V R_{RET} = < 10 Ω R_{SB} = 0.5 Ω	40			
Retract Current V_{DD} Supply Rejection Ratio		V_{DD} = 2 V to 14 V, R_{RET} = 3.74 kΩ		3.0		%/V
Retract Current Temperature Coefficient		V_{DD} = 10 V, R_{RET} = 3.74 kΩ		–0.3		%/°C

Notes
a. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum.

Pin Configurations



Order Number: Si9961ACY

Applications

Introduction

The Si9961 Voice Coil Motor (VCM) driver integrates the active feedback and drive components of a head-positioning servo loop for high-performance hard-disk applications. The Si9961 operates from a 12-V (±10%) power supply and delivers 1 A of steady-state output current. This device is made possible by a power IC process which combines bipolar, CMOS and complimentary DMOS technologies. CMOS logic and linear components minimize power consumption, bipolar front-ends on critical amplifiers provide necessary accuracy, and complimentary (p- and n-channel) DMOS devices allow the transconductance output amplifier to operate from ground to V_{DD}. Two user-programmable, current feedback/input voltage ratios may be digitally selected to optimize gain for both seek and track following modes, to maximize system accuracy for a given DAC resolution. An undervoltage lockout circuit monitors the V+ supply and generates a fault signal to trigger an orderly head-retract sequence at a voltage level sufficient to allow the spindle motor's back EMF-generated voltage to supply the necessary head parking energy. Head retract can also be commanded via a separate $\overline{\text{RETRACT}}$ input. VCM current during retract can be user programmed with a single external resistor. External components are limited to R/C filter components for loop compensation and the resistors that are required to program gain, retract current, and the load current sense.

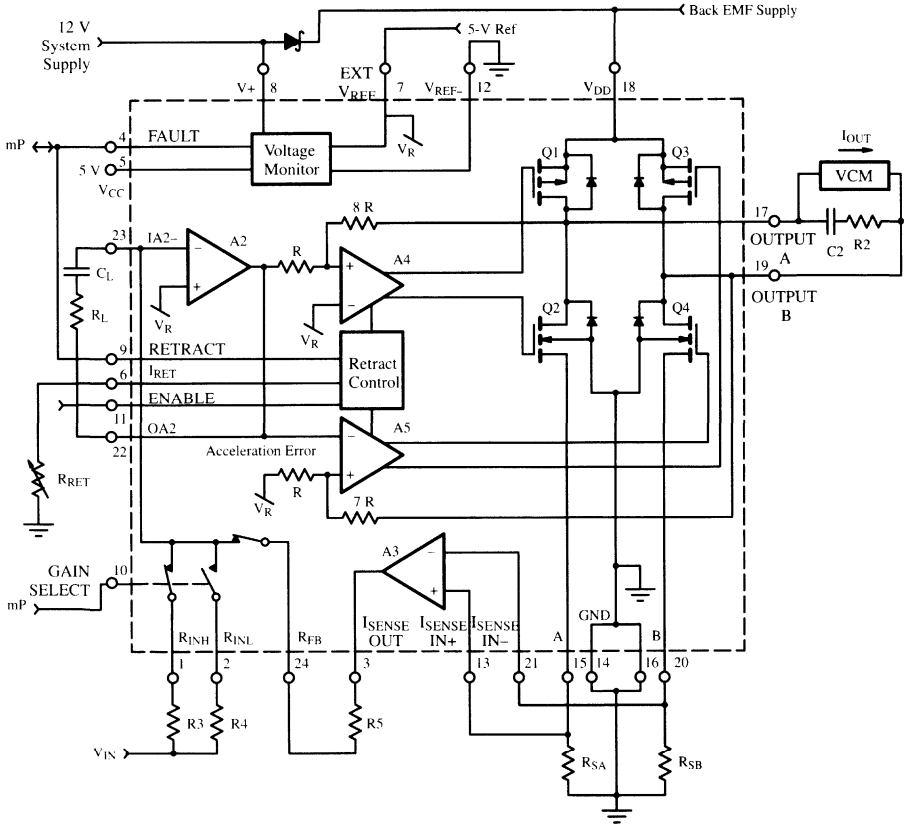


Figure 1. Si9961 Typical Application

Applications (Cont'd)

User-Programmable Gains

During linear operation, the transconductance amplifiers' gains (input voltage at V_{IN} vs. VCM current, in Figure 1) are set by external resistors $R_3 \rightarrow R_5$, R_{SA}, and R_{SB} and selected by gain input. After selecting a value for R_{SA} and R_{SB} that will yield the desired VCM current level, the High and Low feedback gain ratios may be determined by the following:

$$\text{High Gain} = \left(\frac{R_5}{R_3}\right)\frac{1}{4\,R_S} \qquad \text{(GAIN SELECT Input = High)}$$

$$\text{Low Gain} = \left(\frac{R_5}{R_4}\right)\frac{1}{4\,R_S} \qquad \text{(GAIN SELECT Input = Low)}$$

Where $R_S = R_{SA} = R_{SB}$
Input offset current may then be calculated as:

$$I_{OS} = \frac{1}{4\,R_S}\left(\left(\frac{(R_S + R_{IN})}{R_{IN}}\right)V_{OSA2} + 5\,V_{IAS3}\right)$$

Where $R_{IN} = R_3$ or R_4

Head Retract

A low on the $\overline{\text{RETRACT}}$ input pin turns output devices Q1 and Q4 on, and output devices Q2 and Q3 off. Maximum VCM current can be set during head retract by adding an external resistor between the IRET pin and ground. Maximum retract current may be calculated as:

$$I_{OUT} = 175 \times I_{ret} = 175 \times \frac{0.66\ V}{R_{ret}}$$

Head retract can be initiated automatically by an undervoltage condition (either the 12-V or 5-V supplies on the Si9961) by connecting the $\overline{\text{FAULT}}$ output to the $\overline{\text{RETRACT}}$ input.

A high $\overline{\text{ENABLE}}$ input puts both driver outputs in a high-impedance state. The $\overline{\text{ENABLE}}$ function can be used to eliminate quiescent output current when power is applied but the head has been parked, such as a sleep mode. A sleep-mode power down sequence should be preceded by a retract signal since a power failure during this state may not provide adequate spindle-motor back EMF to permit head retraction.

Transconductance Amplifier Compensation

The Si9961CY features an integrated transconductance amplifier to drive the voice coil motor (VCM). To ensure proper operation, this amplifier must be compensated specifically for the VCM being driven. As a first approximation, the torque constant and inertia of the VCM may be ignored, although they will have some influence on the final results, especially if large values are involved. (See Figure 1.)

Frequency Compensation:

The VCM transconductance (in siemens) of this simplified case may be expressed in the s (Laplace) plane as:

$$g_v = \frac{\frac{1}{L_v}}{s + \frac{R_v}{L_v}}$$

Where R_v = VCM resistance in ohms
L_V = VCM inductance in henrys
s is the Laplace operator

In this case, the transconductance pole is at $-Rv/Lv$. It is desirable to cancel this pole in the interest of stability. To do this, a compensation amplifier is cascaded with the VCM and its driver. The transfer function of this amplifier is:

$$H_c = A \times \frac{\left(s + \frac{1}{R_L \times C_L}\right)}{s}$$

Where R_L = Compensation amplifier feedback resistor in ohms
C_L = Compensation amplifier feedback capacitor in farads
A = Compensation amplifier and driver voltage gain at high frequency

If $R_L \times C_L$ is set equal to L_V/R_V, then the combined open loop transconductance in siemens becomes:

$$g_{to} = \frac{A}{s \times L_v}$$

In this case, the transconductance has a single pole at the origin. If this open loop transfer is closed with a transimpedance amplifier having a gain of B ohms, the resultant closed loop transconducatance stage has the transfer function (in siemens) of:

$$g_{tc} = \frac{\frac{A}{L_v}}{s + \frac{A \times B}{L_v}}$$

Where B = Current feedback transimpedence amplifier gain in ohms.

The entire transconductance now contains only a single pole at $-A*B/Lv$. A and B are chosen to be considerably higher than the servo bandwidth, to avoid undue phase margin reduction.

Applications (Cont'd)

As a typical example, in the referenced schematic, assume that Rsa and Rsb = 0.5 Ω, $R_5 = R_3$ = 10 kΩ, VCM inductance (Lv) = 1.5 mH, VCM resistance (Rv) = 15 Ω. Hence:

R_v = 15 Ω
L_v = 1.5 mH
B = 2 Ω
A = 16 x R_L/10000
C_L = $L_v/(R_v \times R_L)$ = 100 x $10^{-6}/R_L$ farads

Gain Optimization:

There are three things to consider when optimizing the gain (A) above. The first is servo bandwidth. The main criterion here is to avoid having the transconductance amplifier cause an undue loss of phase margin in the overall servo (mechanical + electrical + firmware) loop. The second is to avoid confirguing a bandwidth that is more than required in view of noise and stability considerations. The third is to keep the voltage output waveform overshoot to a level that will not cause cross-conduction of the output FETs.

The first two problems can be considered together. Let us assume a disk drive with a spindle RPM of 4400 and with 50 servo sectors per track. The sample rate is therefore:

$$f_s = 50 \times \frac{440}{60}$$ This is a sample frequency of 3667 Hz

As a rule of thumb, the open loop unity gain crossover frequency of the entire servo (mechanical + electrical + firmware) loop should be less than 1/10 of the sample frequency. In this example, the servo open loop unity gain crossover frequency would be less than 367 Hz. If we allow only a 10° degradation in phase margin due to the transconductance amplifier, then a phase lag of 10° at 367 Hz is acceptable. This results in a 3-dB point in the transconductance at :

$$f_{3db} = \frac{367}{\tan(10)}$$

or a 3-dB point in the transconductance at 2081 Hz.

The pole in the closed loop transconductance (–A * B / Lv) should then be 2081 * 2 * π = 13075. This means that A = 9.8. From the above equation for A, R_L = 6.2 kΩ. This sets the minimum gain limit governed by the servo bandwidth requirements. The gain should not be much greater than this, since increased noise will degrade the servo response.

The third problem, keeping the transconductance amplifier voltage output wave form overshoot to a level that will not cause the wrong output FETs to conduct, can be evaluated by deriving the voltage transfer function of the closed loop transconductance amplifier from input voltage to output voltage (Vin to output A and B on the reference schematic).

This is :

$$H_{to} = A \times \frac{s + p}{s + x}$$

Where p = $1/R_L \times C_L$) or R_v/L_v Comp amplifier zero/VCM pole
x = A x B/L_v closed loop pole

If a unit step voltage is applied to the above transfer function and the inverse Laplace transform is taken, the output result is:

$$V_O = A \times \frac{p + (x - p) \times e^{-x \times t}}{x}$$

Where t = time

As we can see, if x = p (i.e. if the VCM pole and compensation amplifier zero = the transconductance closed loop pole), then Vo reduces to A. In other words, a step input results in a step output without overshoot. If x < p then a step input results in an increased rise time output and no overshoot. If x > p, a step input results in a step output with an overshoot.

If this overshoot is large enough, there may be a cross-conduction condition in the output FETs.

Let us look at the above equation at t = 0 and t >> 0, expressed in terms of the open loop high frequency voltage gain, A.

$V_O = A$ At t = 0

$$V_O = \frac{p \times L_v}{B}$$ At t > > 0

In the example shown above, p = 10,000 and A = 9.8. This means that there is some overshoot. At t = 0, the output voltage is 9.8 V per volt of input. At some later time, it has dropped to 7.5 V per volt of input. An overshoot of 31 % is thus produced.

The maximum overshoot voltage requires careful consideration, since it constitutes a potentially catastrophic problem area. If we had decided to optimize for no overshoot, A would equal 7.5, and hence the closed loop pole (A * B / Lv) would be 10,000, which is a frequency of 1.592 kHz. This would have resulted in a phase margin degradation of 13° at the 367-Hz frequency desired. This may or may not be acceptable. One must weigh the servo bandwidth, phase margin degradation, and maximum voltage at the VCM for each individual case.

Applications (Cont'd)

Result:

In the example for the 2081-Hz roll-off case with 31% overshoot and proper pole cancellation, the compensation values are:

$R_L = 6.2\ k\Omega$
$C_L = 0.016\ \mu F$

In the example for the 1592-Hz roll-off case with no overshoot and proper pole cancellation, the compensation values are:

$R_L = 4.7\ k\Omega$
$C_L = 0.022\ \mu F$

The linearity of the transconductance amplifier (around a center value of 500 mA/volt) is shown in Figure 2. In this case, the output current sense resistors (R_{SA} and R_{SB}) were ± 5% tolerance, 0.5 Ω. Any mismatch between R_{SA} and R_{SB} contribute directly to mismatch between the positive and negative "full-scale". Including the external resistor mismatch, the overall loop nonlinearity is approximately 1% maximum over a ± 250-mV input voltage range.

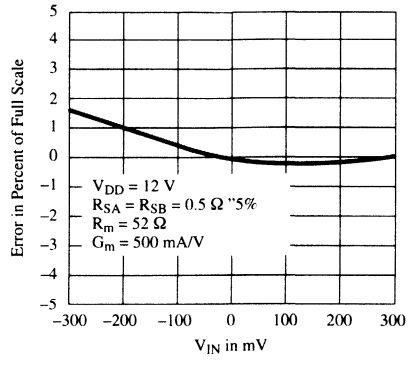


Figure 2. Si9961 Transconductance End Point Non-Linearity

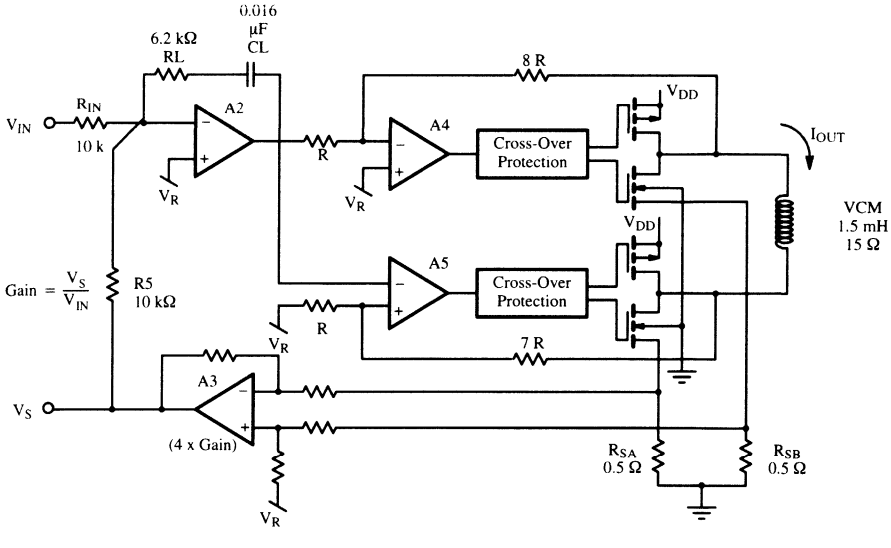


Figure 3. Transconductance Amplifier

Applications (Cont'd)

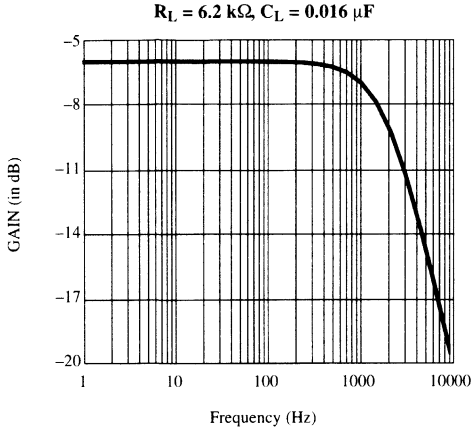


Figure 4.

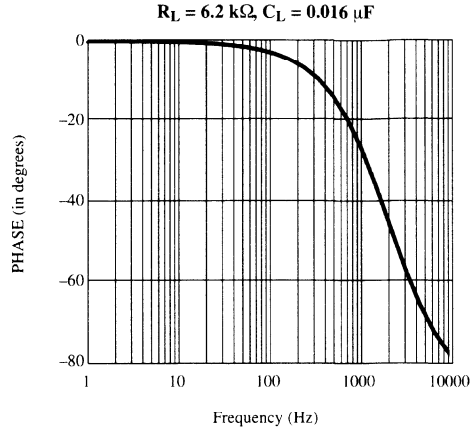


Figure 5.

Si9986CY

Buffered H-Bridge

Features

- 1.0-A H-Bridge
- 200-kHz Switching Rate
- Shoot-Through Limited
- TTL Compatible Inputs
- 3.8- to 13.2-V Operating Range
- Surface Mount Packaging

Applications

- VCM Driver
- Brushed Motor Driver
- Stepper Motor Driver
- Power Converter
- Optical Disk Drives
- Power Supplies
- High Performance Servo

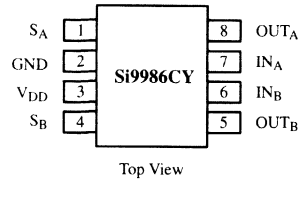
Description

The Si9986CY is an integrated, buffered H-bridge with TTL compatible inputs and the capability of delivering a continuous 1.0 A @ V_{DD} = 12 V (room temperature) at switching rates up to 200 kHz. Internal logic prevents the upper and lower outputs of either half-bridge from being turned on simultaneously. Unique input codes allow both outputs to be forced low (for braking) or forced to a high impedance level.

The Si9986CY is available in an 8-Pin SOIC package, specified to operate over a voltage range of 3.8 V to 13.2 V and a temperature range of 0 to 70°C.

Functional Block Diagram, Pin Configuration and Truth Table

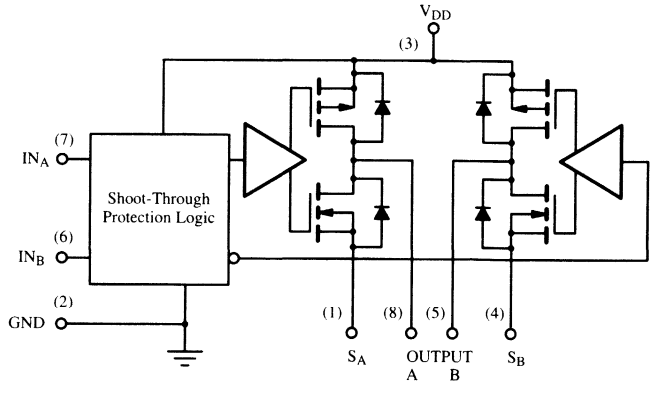
SO-8



Top View

Truth Table

IN_A	IN_B	OUT_A	OUT_B
1	0	1	0
0	1	0	1
0	0	0	0
1	1	HiZ	HiZ



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Absolute Maximum Ratings[a]

Voltage on any pin with respect to ground .... –0.3 V to V_{DD} +0.3 V
Voltage on pins 5, 8 with respect to GND ..... –1 V to V_{DD} +1 V
Voltage on pins 1, 4 ..... –0.3 V to GND +1 V
Peak Output Current ..... 1.5 A
Storage Temperature ..... –50 to 150°C
Maximum Junction Temperature (T_J) ..... 150°C
Maximum V_{DD} ..... 15 V
Power Dissipation[b] ..... 1 W
θ_{JA} ..... 100°C/W

Notes
a. Device mounted with all leads soldered or welded to PC board.
b. Derate 10 mW/°C above 25°C.

Recommended Operating Range

V_{DD} ..... 3.8 V to 13.2 V
Maximum Junction Temperature ..... 125°C
Operating Temperature Range (T_A) ..... 0 to 70°C

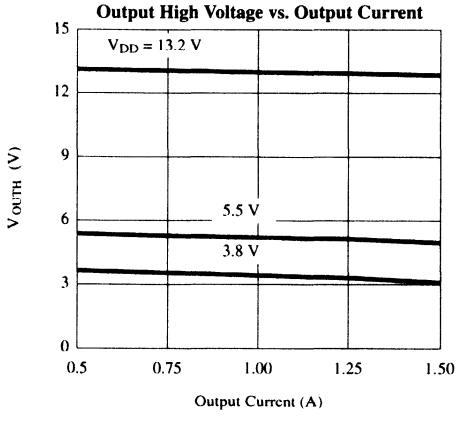
Specifications

Parameter	Symbol	Test Conditions Unless Otherwise Specified V_{DD} = 3.8 to 13.2 V S_A @ GND, S_B @ GND		Limits C Suffix, 0 to 70°C Min[a]	Typ[d]	Max[a]	Unit
Input							
Input Voltage High	V_{INH}			2			V
Input Voltage Low	V_{INL}					1	
Input Current with Input Voltage High	I_{INH}	V_{IN} = 2 V				1	µA
Input Current with Input Voltage Low	I_{INL}	V_{IN} = 0 V		–1			
Output							
Output Voltage High	V_{OUTH}	I_{OUT} = –500 mA	V_{DD} = 10.8 V	10.5	10.7		V
			V_{DD} = 4.5 V	4.1	4.3		
		I_{OUT} = –300 mA, V_{DD} = 3.8 V		3.4	3.7		
Output Voltage Low	V_{OUTL}	I_{OUT} = 500 mA	V_{DD} = 10.8 V		0.2	0.3	
			V_{DD} = 4.5 V		0.2	0.4	
		I_{OUT} = 300 mA, V_{DD} = 3.8 V			0.1	0.4	
Output Leakage Current High	I_{OLH}	$IN_A = IN_B \geq 2$ V, $V_{OUT} = V_{DD}$ = 13.2 V		–10	0		µA
Output Leakage Current Low	I_{OLL}	V_{OUT} = 0, V_{DD} = 13.2 V			0	10	
Output V Clamp High	V_{CLH}	$IN_A = IN_B \geq 2$ V	I_{OUT} = 100 mA		V_{DD} +0.7		V
Output V Clamp Low	V_{CLL}		I_{OUT} = –100 mA		–0.7		
Supply							
V_{DD} Supply Current	I_{DD}	IN = 100 kHz, V_{DD} = 5 V			2		mA
		$IN_A = IN_B$ = 4.5 V, V_{DD} = 5.5 V				300	µA
Dynamic							
Propogation Delay Time	T_{PLH}				250		nS
	T_{PHL}				100		

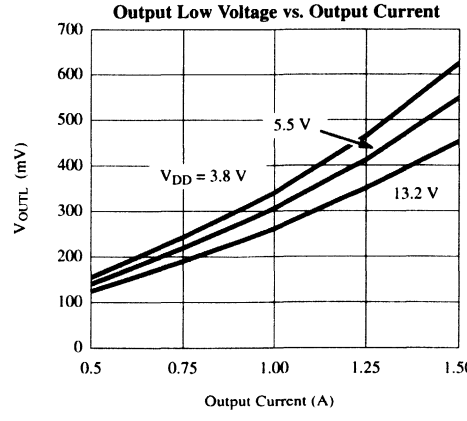
Notes
a. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

Typical Characteristics (25°C Unless Noted)

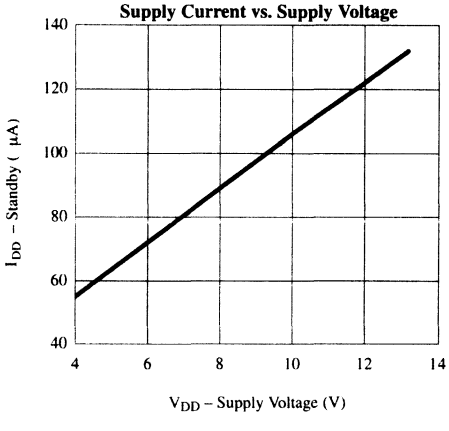
Output High Voltage vs. Output Current



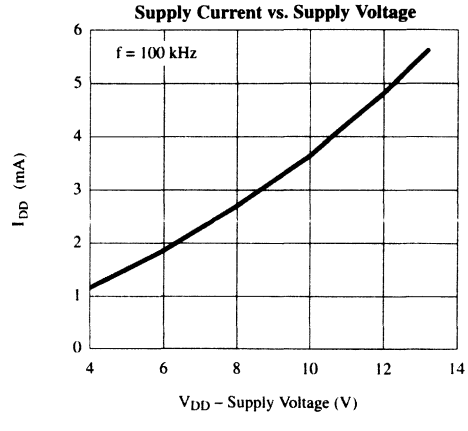
Output Low Voltage vs. Output Current



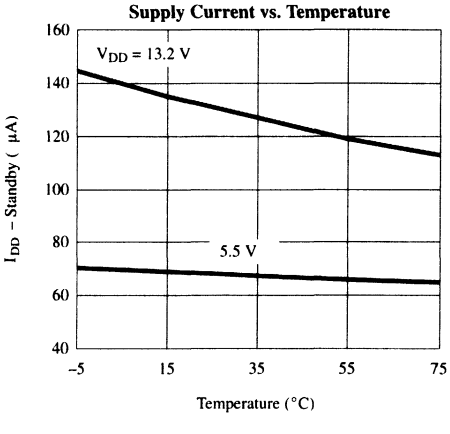
Supply Current vs. Supply Voltage



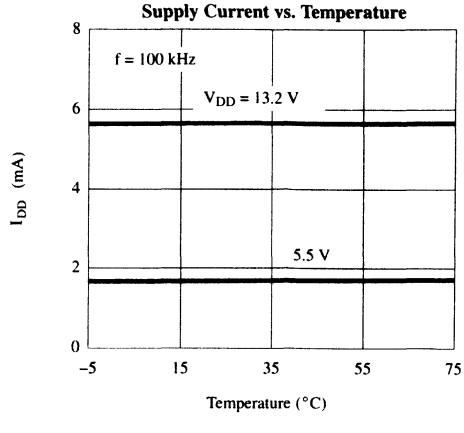
Supply Current vs. Supply Voltage



Supply Current vs. Temperature

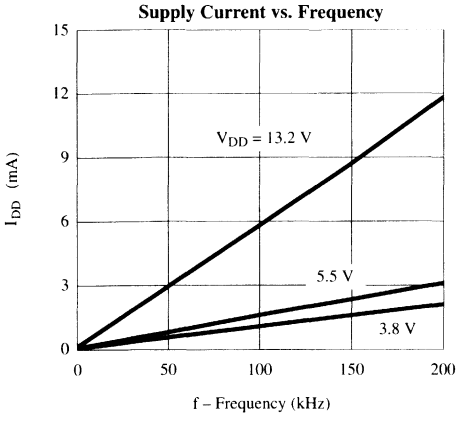


Supply Current vs. Temperature

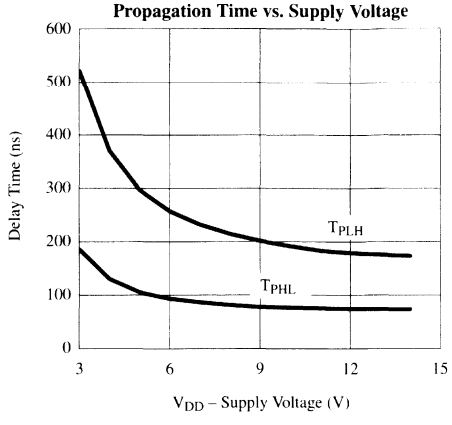


Typical Characteristics (25°C Unless Noted)

Supply Current vs. Frequency



Propagation Time vs. Supply Voltage



Si9986CY Buffered H-Bridge

Robert P. Harshberger Jr.

Introduction

The Si9986CY is a buffered H-bridge that will eliminate all the external discretes that are normally needed to prevent shoot-through in low-voltage brushed motor, stepper motor, and actuator applications. Key features include the following:

- The output FETs are complementary, thus requiring no high-side drive power supply.
- Built-in shoot-through protection prevents both FETs on the same side of the H from being on at the same time. This protection ordinarily would require several external components or additional logic.
- The low-side sources are brought out separately for either single-ended or differential current sense.
- Operating range is 3.8 to 13.2 V, making the Si9986CY ideal for the common PC supply voltages of 5 and 12 V.
- Built-in logic provides four states controlled by CMOS level commands.
  - — The two on-states where current flows through the load from either terminal (OUT_A to OUT_B or OUT_B to OUT_A).
  - — A brake state where terminals OUT_A and OUT_B of the load are both connected to ground, resulting in a dynamic braking action.
  - — A high impedance state where neither terminal OUT_A nor OUT_B of the load is connected, except through the internal flywheel diodes.
- The inputs may be switched at frequencies up to 200 kHz, allowing PWM operation.
- No additional components are necessary, except for a possible snubber circuit, depending on the load and electrical noise requirements and any feedback signal processors.

Applications

The examples and descriptions that follow refer to the truth table below for the Si9986CY.

Truth Table

State	IN_A	IN_B	OUT_A	OUT_B	Action
0	0	0	0	0	Brake
1	0	1	0	1	+Dir.
2	1	0	1	0	– Dir.
3	1	1	HiZ	HiZ	Open

Figure 1 shows a brushed dc motor operating in a full-on, bi-directional mode. Open loop control could be implemented by appropriate high-speed switching between states 1 and 2. (Refer to the Truth Table.)

Figure 2 shows a brushed dc motor operating in a controlled bi-directional, closed-loop mode. Speed control can be implemented by feeding back the low-pass filtered voltage at the load to control the duty cycle of the high-speed switching between states 1 and 2. (Refer to the Truth Table.)

Torque control can be accomplished by using the current feedback signal (Figure 3) to control the duty cycle of the high speed switching between states 1 or 2 and 3. (Refer to the Truth Table.)

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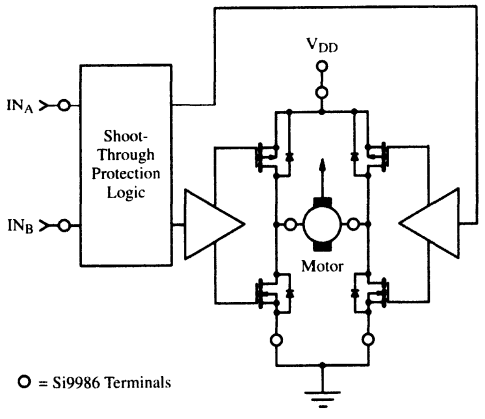

Figure 1. Basic Open Loop

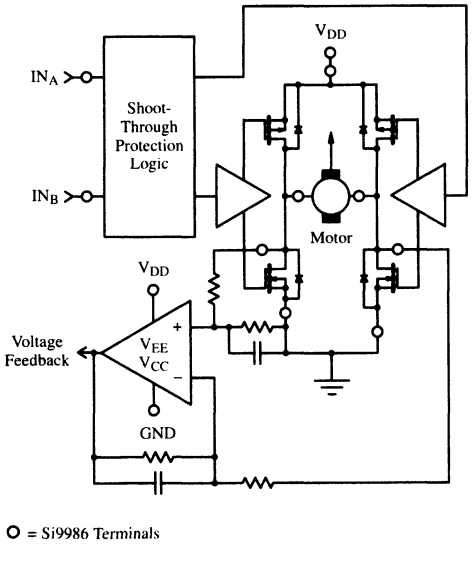

Figure 2. Voltage Feedback for PWM Motor Control

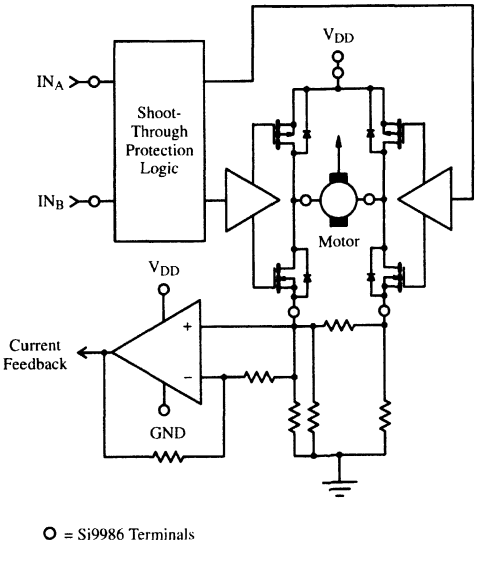

Figure 3. Current Feedback for PWM Motor Control

Feedback Techniques

The Si9986CY uses pulse width modulation (PWM) for proportional control. Linear control requires additional external devices and will not be discussed here. The examples in Figure's 2 and 3 show how to obtain a voltage and a current signal for feedback purposes.

Voltage feedback is used where motor speed is the primary controlled variable. In this case, a low-pass filter is used since the voltage at the load is a high-frequency rectangular wave. The baseband component of this voltage is proportional to the duty cycle of the rectangular wave. The cut-off of the filter is chosen to stop the PWM frequency but pass the lower baseband frequencies required for feedback and control. The rectangular wave switches between the two active states 1 and 2. Switching between these output states tends to give greater control of the voltage and speed, since the output impedance is always low.

Current feedback is used where motor torque or acceleration is the primary controlled variable. A low-pass filter is normally not required, since the motor inductance acts as the filter. If the inductance or the PWM frequency is too low, a low-pass filter may be required. At the output, the rectangular wave switches between active states (1 or 2) and the high impedance state (3). This tends to give greater control of the torque and acceleration, because the output impedance is high when the PWM cycle is off. Motor braking during these periods is thus minimized.

With either feedback technique, state 0 (see Truth Table) will result in motor braking. The analog output of the voltage sense filter or current sense is fed back to the controller input to close the loop. This may be a discrete controller, a microcontroller, DSP, or fuzzy controller. The operation of the controller is beyond the scope of this application brief.

5-V VCM Driver/Spindle Motor Driver

For 1.8- and 2.5-Hard Disk Drives

Features

- On-Board Half-Bridge Drivers
  - — Spindle = 2.3 Ω Total at 1 A
  - — VCM = 3.3 Ω Total at 0.3 A
- Spindle Driver Features:
  - — Back EMF Commutation
  - — Linear Current Control
  - — Internal Current Sense Resistor
  - — Start-Up Current Limit (10% Accurate)

Benefits

- Single 5-V Supply
- Rail-to-Rail Output Voltage Swing
- VCM Driver Features:
  - — Class AB Linear Operation
  - — Externally Programmable Gain and Bandwidth
  - — Programmable Retract Current and Fixed Voltage Clamp

Applications

- Over-Temperature Protection
- System Voltage Monitor
- Undervoltage Head Retract
- Sleep Mode and Idle Mode
- Reference Generator
- Two Uncommitted Amplifiers

Description

The Si9990ACS has a 3-phase brushless dc (spindle) motor driver and a linear transconductance amplifier suitable for driving a voice coil motor (head actuator).

Spindle Motor Driver

The spindle driver features three 1-A, 2.3-Ω (total) all n-channel MOSFET half-bridge output stages. The spindle driver uses internal back EMF sensing circuitry that eliminates the need for hall sensors. An internal charge pump allows rail-to-rail output voltage swing with a nominal 5-V supply. A unique output structure eliminates the need for an external Schottky diode to isolate the system 5-V supply if it fails during operation. This makes the output half-bridge drive capability equivalent to drivers with 1-A, 1.9-Ω specifications in series with the required Schottky diode.

VCM Driver

The VCM driver provides all necessary functions including a motor current sense amplifier, a loop compensation amplifier and a 300-mA power amplifier featuring four MOSFETs in an H-bridge configuration. The output crossover protection ensures no cross-conducting current and Class AB operation during linear tracking. Externally programmable gain switching at the input summing junction increases the resolution and dynamic range for a given DAC. The head retract circuitry can be activated by either an undervoltage condition or an external command. An external resistor is required to set the VCM current during retract. The retract voltage clamp is set at 0.44 V.

A reference generator and two uncommitted amplifiers are also provided for analog interface.

In sleep mode, internal logic initiates a head retract operation followed by spindle brake and shutdown of all analog circuitry except the supply monitor. The standby power dissipation is less than 6 mW. The VCM may also be disabled without disabling spindle operation (idle mode). All controls from the microprocessor are communicated via the serial interface. Additional housekeeping functions of the driver include thermal shutdown and undervoltage lockout.

The Si9990ACS is manufactured using a self-isolated BiC/DMOS process and is available in a 64-pin SQFP package for operation over the commercial (0 to 70°C) temperature range.

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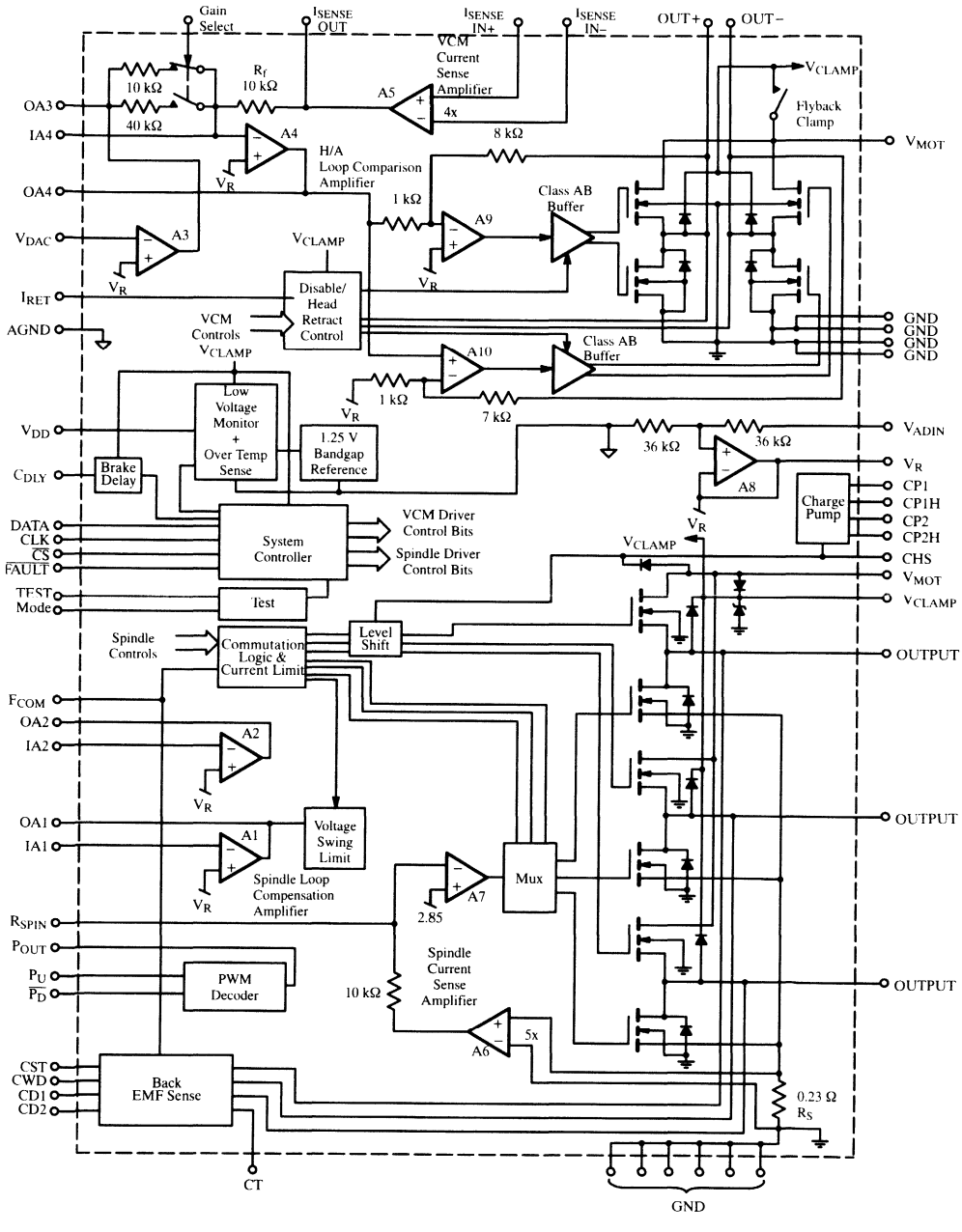
Functional Block Diagram



Absolute Maximum Ratings

Voltages Referenced to Common Pin

V_{DD} Supply Range ..... –0.3 V to 7 V

Pin (Output A, B and C) ..... –0.3 V to V_{CLAMP} + 0.3 V

Pin (Output + and –) ..... –0.3 to V_{MOT} + 0.3 V

Pin (CHS, CP1H, CP2H) ..... –0.3 V to 16 V

Maximum Output Current[1]

Output A, B and C (Peak) ..... 1.2 A
Output A, B, and C (Continuous) ..... 0.4 A
Output + and – (Peak) ..... 0.5 A
Output + and – (Continuous) ..... 0.3 A

Pin (All Others) ..... –0.3 V to V_{DD} + 0.3 V

Maximum Clamp Current[2]

Output A, B and C ..... ± 1.2 A
Output + and – ..... ± 0.5 A
(Pulsed 10 ms at 10% duty cycle)
All Other Pins ..... ± 20 mA

V_{MOT} to V_{CLAMP} Diode (Peak) ..... 100 mA
V_{MOT} to V_{CLAMP} Diode (Continuous) ..... 50 mA
V_{MOT} to CHS Diode (Peak) ..... 50 mA
V_{MOT} to CHS Diode (Continuous) ..... 25 mA

Storage Temperature ..... –65 to 150°C

Operating Temperature ..... 0 to 70°C

Junction Temperature (T_J) ..... 150°C

Power Dissipation[3]

64-Pin SQFP ..... 2.0 W

Thermal Impedance (θ_{JA})[3]

64-Pin SQFP ..... 62.5°C/W

Notes

1. Output current rating is dependent on the system duty cycle, start-up timing and heat dissipation capability.
2. Diode currents depend on power supply start-up transient and bypass capacitor values.
3. Device mounted with all leads soldered or welded to PC board.

Specifications

Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_{ADIN} = V_{DD} = V_{MOT} = 5$ V ± 10% R_S(VCM) = 1.67 Ω R_{SPIN} = 17 kΩ, T_A = 0 to 70°C	Limits Min	Limits Typ	Limits Max	Unit
Supply						
Supply Current	I_{DD} + I_{MOT}	Static, No Load, Sleep Mode		0.9	1.2	mA
		Static, No Load, Normal Operation		20	41	
		Static, No Load, Idle Mode		14	19	
V_{DD}, V_{MOT} Operating Range	V_{DD}, V_{MOT}		4.5	5	5.5	V
Control Logic						
Low Input Voltage (G/S, DATA, CLK, $\overline{CS}$, P_U, $\overline{P_D}$)	V_{IL}		–0.3		1.5	V
High Input Voltage	V_{IH}		3.5		5.3	
Low Input Current	I_{IL}	V_{IN} = 0 V	–1			µA
High Input Current	I_{IH}	V_{IH} = 5 V			1	
Mode Pin Pull Down Current	I_{PD}	V_{IN}= 5 V	5		100	
Low Output Voltage (F_{COM}, $\overline{FAULT}$, P_{OUT})	V_{OL}	I_{OUT} = 500 µA			0.5	V
High Output Voltage	V_{OH}	I_{OUT} = –500 µA	4			
P_{OUT} Off-State Leakage Current		V_{OUT} = 2.5 V	–1		1	µA
EMF Comparator Offset	V_{OS}		20	40	70	mV
Maximum EMF Comparator Input Common Mode Voltage				4.3		V

Specifications (Cont'd)

Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_{ADIN} = V_{DD} = V_{MOT} = 5\ V \pm 10\%$ $R_S(VCM) = 1.67\ \Omega$ $R_{SPIN} = 17\ k\Omega$, $T_A = 0$ to $70°C$	Limits Min	Limits Typ	Limits Max	Unit
Control Logic (Cont'd)						
CST Current	I_{CST}	Charging or Discharging		5		µA
CD Current (CD1 or CD2)	I_{CD1} or I_{CD2}	Charging		10		µA
		Discharging		–20		
I_{CD} (Discharging)/I_{CD} (Charging)		C_{D1} or C_{D2}		2.0		
CWD Current	I_{CWD}	Charging		5		µA
		Discharging		–25		
CWD Threshold Voltage	V_{TL}			0.5		V
	V_{TH}			2.50		
Spindle Transconductance Amplifier (A_1)						
Voltage Gain	A_V	$R_{LOAD} = 50\ k\Omega$ to V_R (See Note a) Measured at 1.2 to 2.9 V		60		dB
Gain-Bandwidth	F_o	$R_{LOAD} = 50\ k\Omega$, $C_{LOAD} = 100\ pF$ to V_R		1		MHz
Slew Rate	SR		0.5			V/µs
Output Voltage Swing	V_{OUT}	$R_{LOAD} = 50\ k\Omega$ to V_R Bits D_2 D_3 = 00 to 11	0.8		3.1	V
Input Bias Current	I_b				50	nA
Offset Voltage	V_{OS}				10	mV
Power Supply	PSRR	f = 10 kHz		50		dB
Spindle Transconductance Amplifier (A_6 and A_7)						
Transconductance	G_{ms}	$R_{LOAD} = 4\ \Omega$ to V_{MOT}	0.4	0.5	0.6	A/V
Output Current Limit Accuracy			–20		20	%
–3 dB Bandwidth	F_o	$R_{LOAD} = 4\ \Omega$ to V_{MOT}, $C_{LOAD} = 100\ pF$		70		kHz
Slew Rate	SR			1		V/µs
Output Current Cutoff Voltage		Measured at OA1 with respect to GND	2.70	2.85	3.0	V
Spindle Half-Bridge						
On Resistance (Sink or Source)	$r_{DS(on)}$	$I_{OUT} = -1\ A$		0.6		Ω
		$I_{OUT} = 1\ A$ including $0.23\ \Omega\ R_S$		0.7		
		(Sink + Source), $I_{OUT} = 1\ A$			2.3	
Ouptut Leakage Current	$I_{DS(off)}$	$V_{OUT} = V_{MOT}$			100	µA
		$V_{OUT} = 0\ V$	–100			
Clamp Diode	$V_{f(on)}$	$I_{OUT} = 1\ A$	–1.5			V

Specifications (Cont'd)

Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_{ADIN} = V_{DD} = V_{MOT} = 5$ V ± 10% R_S(VCM) = 1.67 Ω R_{SPIN} = 17 kΩ, T_A = 0 to 70°C	Limits Min	Limits Typ	Limits Max	Unit
VCM Transconductance Amplifier (A_3, A_4, A_5, A_9, A_{10} and DMOS FETs)						
Transconductance	G_{MVH}	Gain Select = High, I_{OUT} = ±300 mA	142	150	158	mA/V
	G_{MVL}	Gain Select = Low, I_{OUT} = ±75 mA	35.6	37.5	39.4	
Output Offset Current, High Gain	I_{OS}, HG	Gain Select = High	−5	0	+5	mA
Output Offset Current, Low Gain	I_{OS}, LG	I_{OS} (G/Sel = High)–I_{OS} (G/Sel = Low)	−5	0	+5	
Output Compliance	V_{OH}	I_{OH} = 0.3 A, V_{MOT} = 4.5 V, ± Output	3.9	4.2		V
	V_{OL}	I_{OL} = 0.3 A, V_{MOT} = 4.5 V, ± Output		0.2	0.4	
Clamp Diode Voltage	V_{CL}	I_F = 0.3 A			1.5	
Feedback Resistance	R_F	From $I_{SENSE(OUT)}$ to IA4		10		kΩ
3 dB Bandwidth A_4, A_5				1		MHz
3 dB Bandwidth A_9, A_{10}				0.4		
PSRR		@ 10 kHz		50		dB
Output Swing A_3, A_5		R_{LOAD} = 50 kΩ to V_R	0.2		V_{DD} −0.2	V
Output Swing A_4		R_{LOAD} = 50 kΩ to V_R	1.2		V_{DD} −1.2	
Reference Generator (A_8)						
Input Resistance		Measured at V_{ADIN} Pin		72		kΩ
Output Voltage	V_R	I_{OUT} = ±2 mA	2.37	2.5	2.63	V
Power Supply Monitor						
V_{DD} Undervoltage Threshold			3.7	3.9	4.1	V
Hysteresis				70		mV
Overtemperature Protection						
Trip Point				165		°C
Hystersis				20		
Head Retract Function (Undervoltage Or Sleep Mode; C_{DLY} tied to V_{CLAMP})						
I_{RET} Bias Voltage	V_{RET}	$I_{RET} = \frac{V_{RET}}{R_{RET}}$, $I_{OUT} = -(200 \times I_{RET})$		0.25		V
Retract Output Current Limit	I_{OUT+}	R_{RET} = 2.5 kΩ, V_{OUT+} = 0.2 V	14	20	26	mA
Retract Output Voltage Limit	V_{OUT-}	I_{OUT-} = −20 mA	0.31	0.44	0.5	V
Emergency Retract Supply Current	I_{CLAMP}	V_{CLAMP} = 3 V, R_{RET} = 2.5 kΩ V_{DD} = 0 V, Static, No Load		2	4	mA
Retract Supply Voltage Range	V_{CLAMP}		1.41	5	5.5	V
CHS Leakage	I_{CHS}	V_{DD} = 0 V, V_{CLAMP} = 3 V, V_{CHS} = 10 V			2	µA
dc to dc Converter (Charge Pump)						
Output Voltage	CHS	I_{CHS} = −5 mA, V_{DD} = V_{MOT} = 4.5 V	11			V

Specifications

Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_{ADIN} = V_{DD} = V_{MOT} = 5$ V ± 10% R_S(VCM) = 1.67 Ω R_{SPIN} = 17 kΩ, T_A = 0 to 70°C	Limits Min	Limits Typ	Limits Max	Unit
Flyback Clamp						
Flyback Clamp Switch Resistance		Normal Mode, I_{CLAMP} = 0.1 A		4		Ω
Clamp Zener Voltage	V_Z	I_{CLAMP} = 0.1 A		9.1		V
Uncommitted Amplifier (A_2)						
Input Offset Voltage	V_{OS}		−15	0	+15	mV
Input Bias Current	I_B				50	nA
Unity Gain Bandwidth		R_{LOAD} = 50 kΩ, C_{LOAD} = 100 pF to V_R		1		MHz
Slew Rate	SR		1			V/µs
Power Supply Rejection Ratio	PSRR	@ 10 kHz		50		dB
Open Loop Voltage Gain	A_{VOL}	R_{LOAD} = 50 kΩ to V_R, Measured at V_R ± 1.8 V		60		dB
Output Voltage Swing	V_O	R_{LOAD} = 50 kΩ to V_R	0.2		V_{DD} − 0.2	V
Timing						
Chip Select to Clock Setup Time	t_{CS}	See Timing Diagram, Figure 1	160			ns
Data Setup Time	t_{DS}		160			
Data Hold Time	t_{DH}		160			
Head Retract Time-Out (Brake Delay)	t_{DLY}	t_{DLY} = 514 kΩ × C_{DLY}, C_{DLY} = 0.18 µF, V_{DD} = 0 V, V_{CLAMP} = 1.41 to 5.5 V	55	100	240	ms

Notes
a. 50-kΩ load is in addition to the R_{SPIN} load.

Detailed Description

Serial Port

A 6-bit word at the serial port DATA pin is used to program basic operating conditions. The function of each bit is shown in Tables 3 and 2. To write data to the serial port, $\overline{CS}$ is pulled low during CLOCK low. This holds the existing word while new data is written into the shift registers on a positive CLOCK edge. The new data becomes valid on the rising edge of $\overline{CS}$. When $\overline{CS}$ is high, CLOCK is disabled and data cannot be shifted.

D0 is the last bit written to the serial port. It enters sleep mode (D0 = 0) upon power up. When D0 is written "0", a head retract is automatically initiated and t_{DLY} applies following the next $\overline{CS}$ rising edge.

The Mode pin is used for production testing only. It should be tied low during normal operation.

Detailed Description (Cont'd)

Table 3: Serial Port Definitions

Bit	Name	Function	
		0	1
D0	Sleep Mode/System Enable	Sleep Mode: VCM retracted, spindle and VCM brake applied after period t_{DLY}	Normal Operation
D1	Spindle Brake	Normal Operation	Spindle Disabled and Brake Applied, VCM Enabled
D2	Spindle Current Limit	See Table 2	
D3	Spindle Current Limit	See Table 2	
D4	Idle Mode/VCM Enable	Idle: VCM Disabled and Brake Applied, Spindle Running	Normal Operation
D5	Spindle Step Mode	Normal Operation	Test Pin Becomes Single Step Commutation Clock

Table 4: Spindle Current Limit

D2	D3	Current Limit	Current Limit (R_{SPIN} = 17 kΩ)	Current Limit (R_{SPIN} = 15.7 kΩ)
0	0	1.85 V • G_{ms}	925 mA	1 A
0	1	1.45 V • G_{ms}	725 mA	780 mA
1	0	1.05 V • G_{ms}	525 mA	570 mA
1	1	0.65 V • G_{ms}	325 mA	350 mA

G_{ms} = Transconductance (Refer to (1)VCM Design Equations, page 3-84)

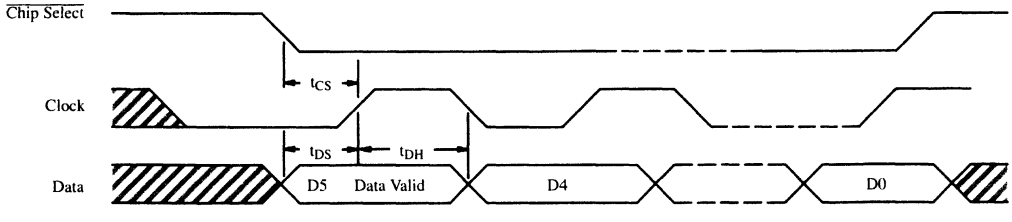


Figure 1. Write Cycle Timing Diagram

Motor Shutdown Sequence

The Si9990ACS executes a motor shutdown sequence whenever V_{DD} drops below 3.9 V (emergency retract), or serial bit D0 is set low (sleep mode). The shutdown sequence is terminated by a programmable one-shot (brake delay). During the time-out (t_{DLY}), both the spindle and VCM outputs are turned off. Simultaneously, a separate VCM retract circuit is activated. As shown in Figure 2, the all-bipolar design enables retract function all the way down to a supply of 1.41 V at V_{CLAMP} pin. The retract current typically is 20 mA, adjustable with an external resistor, R_{RET}. To limit retract velocity, a fixed clamp limits the voltage across VCM to no more than 440 mV. After the time-out, the retract circuitry is shut off while the spindle motor and VCM brake is activated by turning on all low-side DMOS drivers. To brake faster (i.e., with lower impedance short across the motor windings) the low-side drivers are powered by the residual charges on the CHS bypass capacitor.

Detailed Description (Cont'd)

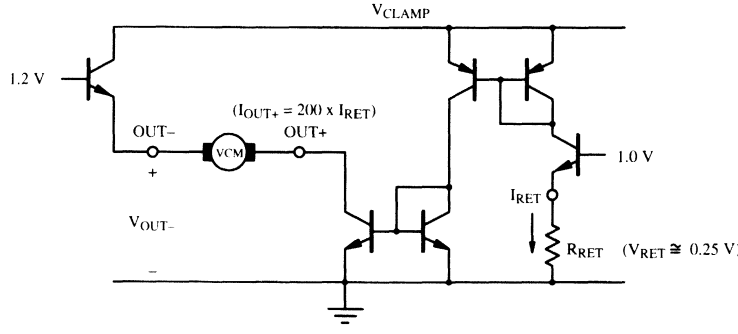


Figure 2. Simplified Retract Circuit

Spindle Driver

Table 5: Spindle PWM Speed Control (Double Integrator)

System State	P_U	P_D	P_{OUT}	State
Run	0	0	1	Decel
Run	0	1	Z	Hold
Run	1	0	Z	Hold
Run	1	1	0	Accel
Spindle Brake/Sleep	X	X	0	Accel

Table 6: Spindle Commutation Sequence

Sequencer State	OUT_A	OUT_B	OUT_C
Reset*	Z	Z	Z
1	High	Low	Z
2	High	Z	Low
3	Z	High	Low
4	Low	High	Z
5	Low	Z	High
6	Z	Low	High

*Reset is the state after exiting sleep or spindle brake mode.

Note: X = Don't Care, Z = High Impedance

Pin Description

Power Supplies

Function	Pin Number	Description
V_{DD}	61	+5-V supply for VCM and spindle controller logic.
V_{MOT}	7, 8, 57, 58	+5-V supply for VCM and spindle motor drivers.
V_{CLAMP}	53	Inductive flyback clamp and emergency head retract power supply. This pin is shorted to V_{MOT} by an on-chip switch during normal operation. The switch eliminates the need for an external Schottky diode.
AGND	24	Low noise ground return for critical analog functions.
GND	3, 4, 11, 12 36, 37, 38, 39 42, 43	Ground return for the entire chip. All ground pins are connected to each other through the die substrate and lead frame. The large number of direct connections to the lead frame lowers thermal impedance and improves power dissipation.
CHS	56	Output of the dc-to-dc converter, used to power VCM and spindle drive MOSFETs. The converter is a 3X charge pump capable of sourcing 5 mA. An external > 0.1 µF capacitor between Pin 56 and ground is necessary.
CP2H	59	Positive side of the external 3X charge pump capacitor.
CP1H	60	Positive side of the external 2X charge pump capacitor.
CP2	54	500-kHz oscillator output, used to drive the 3X charge pump.
CP1	55	Inverted output of the on-chip 500-kHz oscillator, used to drive the external 2X charge pump capacitor.
V_{ADIN}	23	Low noise +5-V supply pin for the on-chip reference generator.
V_R	22	Output of the on-chip reference generator: $V_R = V_{ADIN} / 2$. This is used as the dc reference level for all analog signals.

Voice Coil Motor Driver

Function	Pin Number	Description
GAIN SELECT	2	Input pin used to select VCM transconductance. A high input sets the gain to the maximum and a low input sets the gain to be $^1/_4$ of the maximum.
V_{DAC}	16	Inverting input of servo PWM filter amplifier.
OA3	15	Output of servo PWM filter amplifier. Connect R_C network from this pin to V_{DAC} to set filter bandwidth. A positive OA3 relative to V_R will set V_{CM} output current positive.
IA4	14	Inverting input of V_{CM} loop compensation amplifier.
OA4	13	Output of V_{CM} loop compensation amplifier. Connect lead-lag network from this pin to IA4 to set desired loop bandwidth.
I_{SENSE} IN+	62	Positive input terminal for V_{CM} current sense amplifier. This pin connects to external sense resistor and V_{CM}.
I_{SENSE} IN–	63	Negative input terminal for V_{CM} current sense amplifier. This pin connects to the other side of sense resistor and OUT+ pin.
I_{SENSE} OUT	64	Output terminal of V_{CM} current sense amplifier.
OUT+	5, 6	V_{CM} power amplifier positive output terminal. Current from OUT+ is positive.
OUT–	9, 10	V_{CM} power amplifier negative output terminal. During head retract, V_{CM} output current will be negative, or flowing from this pin into the V_{CM} load.
I_{RET}	1	Control pin for head retract current (nominally 0.25 V). An external resistor is connected to this pin. The current is amplified 200 times at the V_{CM} driver.
C_{DLY}	21	An external capacitor is connected to this pin to set the maximum head retract time, t_{DLY} = 514 kΩ x C_{DLY}. At the end of the delay, the spindle motor is set to brake. A head retract may also be forced, by asserting this pin low.

Pin Description (Cont'd)

Microcontroller Interface

Function	Pin Number	Description
DATA	18	Data input for the serial port.
CLK	19	Clock input for serial port data.
CS	20	Strobe input for data word. System commands are executed at the rising edge of $\overline{CS}$.
FAULT	17	Undervoltage flag output. Forced low if 5-V supply drops below 3.9 V, or the internal power-on reset timer (approximately 0.5 ms) is timing out.

Diagnostic Functions

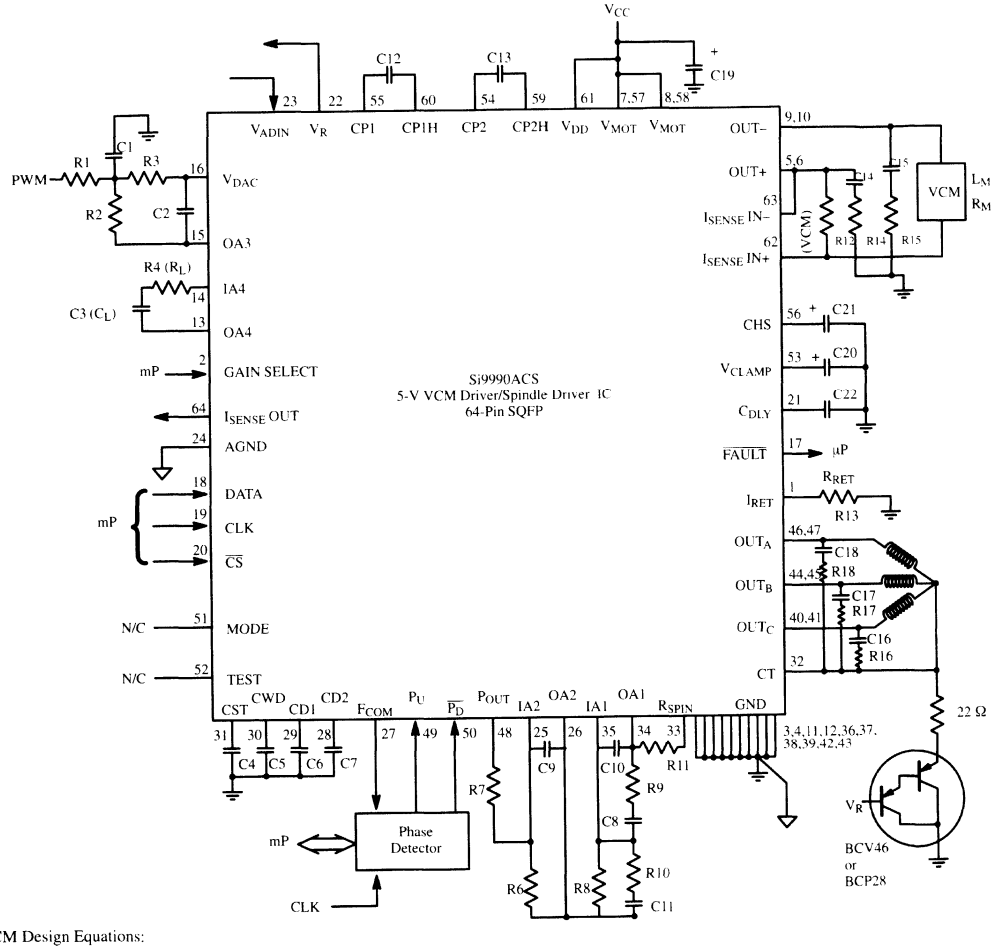
Function	Pin Number	Description
MODE	51	Control input used for manufacture testing only. Grounded or left open during normal operation.
TEST	52	Used as temperature test or step mode clock input. Controlled by serial port.

Spindle Motor Driver

Function	Pin Number	Description
F_{COM}	27	Spindle commutation clock output. A positive going pulse is generated whenever a valid back EMF zero crossing is detected. The external speed control, working in either phase or frequency domain, compares this signal against a reference clock and feedbacks a PWM servo signal to the spindle driver via the PWM decoder and low-pass filter (A_2).
P_U	49	Pulse width modulation pull-up command from speed control.
P_D	50	Pulse width modulation pull-down command from speed control.
P_{OUT}	48	Pulse width modulation output from speed control. This pin is connected to the external integrating resistor of A_2. P_{OUT} is low, or accelerating, if P_U = high and $\overline{P_D}$ = high. P_{OUT} is high, or decelerating, if P_U = low and $\overline{P_D}$ = low. P_{OUT} is tri-state, or holding, otherwise.
IA2	25	Inverting input of spindle PWM low-pass filter amplifier.
OA2	26	Output of spindle PWM low-pass filter amplifier. Connect RC network from this pin to IA2 to set desired cutoff frequency.
IA1	35	Inverting input of spindle loop compensation amplifier.
OA1	34	Output of spindle loop compensation amplifier. Connect RC lead-lag network from this pin to IA1 to set compensation.
R_{SPIN}	33	Connect an accurate external resistor from this pin to OA1 to set spindle transconductance and current limit. The recommended resistance is 17 kΩ.
OUT_A	46, 47	Spindle phase A output terminal.
OUT_B	44, 45	Spindle phase B output terminal.
OUT_C	40, 41	Spindle phase C output terminal.
CST	31	An external capacitor connected to this pin will generate commutation pulses to start up the spindle motor.
CWD	30	An external capacitor connected to this pin will disable the back EMF comparators during diode recirculation, detect incorrect motor rotation or stall.
CD1	29	Connect at this pin one of the two external capacitors used to generate the ideal commutation point from the back EMF zero crossing points.
CD2	28	Connect a second capacitor identical to CD1 at this pin to generate the optimum commutation delay.
CT	32	Spindle motor center tap input for back EMF sensing.

Application

64-Pin SQFP test board for typical $2^1/_2$" or smaller HDD (shown with external phase detector for spindle speed control and external PWM for VCM DAC)



VCM Design Equations:

(1) Transconductance (G_{mv})

→ High Gain = $\frac{1}{4\ R_S}$; G/SEL = High

→ Low Gain = $\frac{1}{16\ R_S}$; G/SEL = Low

(2) Output Retract Current

$$I_{OUT} = 200 \times I_{RET} = 200 \times \frac{0.25\ V}{R_{RET}}$$

(3) Transconductance Loop Compensation

$$\text{Closed-Loop BW} = \frac{4\ (16)}{2\ \pi\ (10\ K)\ C_L}\left(\frac{R_S}{R_M + R_S}\right)$$

or

$$\left\{\begin{array}{l} C_L = \dfrac{64}{2\pi\ (10\ K)\ BW}\left(\dfrac{R_S}{R_M + R_S}\right) \\ R_L = \dfrac{L_M}{C_L\ (R_M + R_S)} \end{array}\right\}$$

R_M = Motor Resistance
L_M = Motor Inductance

Spindle Design Equation: Transconductance (G_{ms}) = $\frac{8700}{R_{SPIN}}$

(4) Refer to AN93-1 for all servo equations.

Application

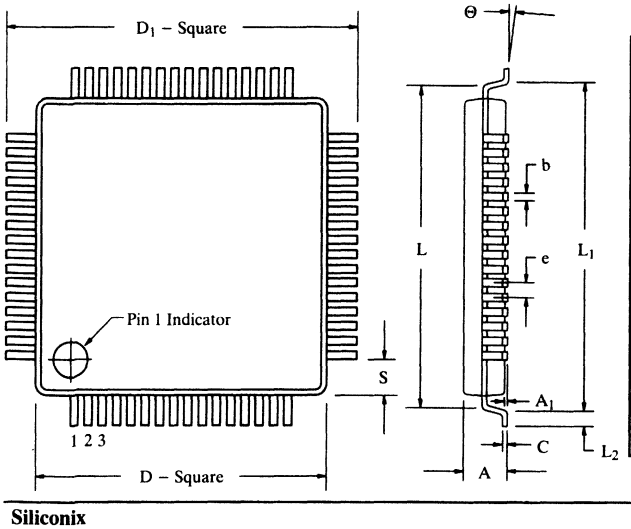
Table 7: Components for Test Board

Name	Value	Comments
R1	100 k	VCM PWM Low Pass Filter
R2	100 k	VCM PWM Low Pass Filter
R3	100 k	VCM PWM Low Pass Filter
R4	2.61 k	VCM Transconductance Amplifier Compensator
R6	39 k	Spindle PWM Low Pass Filter
R7	110 k	Spindle PWM Low Pass Filter
R8	5.6 M	Spindle Speed Control Lead-Lag Compensator
R9	910 k	Spindle Speed Control Lead-Lag Compensator
R10	470 k	Spindle Speed Control Lead-Lag Compensator
R11	17 k	R_{SPIN} Resistor
R12	1.67	VCM Sense Resistor
R13	2.5 k	VCM Retract Bias Resistor (R_{RET})
R14	30	VCM Snubber Resistor
R15	30	VCM Snubber Resistor
R16	62	Spindle Snubber Resistor
R17	62	Spindle Snubber Resistor
R18	62	Spindle Snubber Resistor
C1	1.2 nF	VCM PWM Low Pass Filter
C2	100 pF	VCM PWM Low Pass Filter
C3	18 nF	VCM Transconductance Amplifier Compensator

Name	Value	Comments
C4	27 nF	Spindle Start-Up Capacitor
C5	680 pF	Spindle Watch-Dog Capacitor
C6	1.8 nF	Spindle Commutation Delay Capacitor #1
C7	1.8 nF	Spindle Commutation Delay Capacitor #2
C8	0.22 nF	Spindle Loop 'Zero' Capacitor
C9	2.7 nF	Spindle PWM Low Pass Filter
C10	2.2 nF	Spindle Speed Control Lead-Lag Compensator
C11	10 nF	Spindle Speed Control Lead-Lag Compensator
C12	82 nF	Charge Pump Capacitor #1
C13	82 nF	Charge Pump Capacitor #2
C14	100 nF	VCM Snubber Capacitor
C15	100 nF	VCM Snubber Capacitor
C16	180 nF	Spindle Snubber Capacitor
C17	180 nF	Spindle Snubber Capacitor
C18	180 nF	Spindle Snubber Capacitor
C19	≥ 0.1 µF	Bypass Capacitor
C20	≥ 0.1 µF	Bypass Capacitor
C21	≥ 0.1 µF	Bypass Capacitor
C22	180 nF	Brake Delay Capacitor (C_{DLY})
Note:	These values are entirely dependent on motor characteristics.	

Package Outline

■ SQFP 64-Pin



Dim	Millimeters		Inches*	
	Min	Max	Min	Max
A	1.35	1.60	0.053	0.063
A_1	0.04	0.16	0.002	0.006
b	0.14	0.26	0.006	0.010
C	0.117	0.177	0.005	0.007
D	9.90	10.10	0.390	0.398
D_1	11.7	12.3	0.461	0.484
e	0.40	0.60	0.016	0.024
L	–	10.80	–	0.425
L_1	10.80	11.20	0.425	0.441
L_2	0.30	0.70	0.012	0.028
S	–	1.20	–	0.047
Θ	0°	4°	0°	4°

*For Reference Only

HDD Servo Design Using the Si9990CS

Alan Grace

Introduction

Small-form factor hard disk drive (HDD) rotating memories place several difficult constraints on the designers of servo mechanisms for head positioning and spindle motor drives. The most demanding design constraint is size. There is simply not enough room in a 1.8-inch drive to include separate ICs for the head positioning and spindle servos. The Si9990CS from Siliconix addresses this space problem by combining voice coil motor (VCM) and spindle drive servos in a single 64-pin slim quad flat package (SQFP). The Si9990CS is manufactured using a BiC/DMOS process to achieve maximum integration while minimizing internal power dissipation. Bipolar transistors are used in analog circuits (such as the bandgap reference) and where the lowest operating voltage is required (such as the head retract circuit). CMOS logic allows the quiescent current to be reduced to only 1.2 mA in the sleep mode. DMOS output transistors eliminate the need for external drivers and allow rail-to-rail voltage swing.

While the size of HDDs is continually being reduced, the complexity and performance of the servos is being driven in the other direction by the need to increase areal densities. Reduced track spacing (more tracks per inch) requires greater accuracy, which translates to higher gain and dynamic range for the VCM servo. Also, minimization of the seek time and the hand-over time between seek and track following modes (which directly relate to a drive's access time specifications) requires greater bandwidth for the VCM servo. Loop compensation becomes critical as the gain bandwidth of the system is increased.

To meet the performance needs of the VCM servo, the Si9990CS incorporates a transconductance amplifier with low crossover distortion. Its output stage has four n-channel MOSFETs in an H-bridge configuration which are capable of 300-mA output current and are redesigned for class AB operation. Current feedback and loop compensation amplifiers are also included.

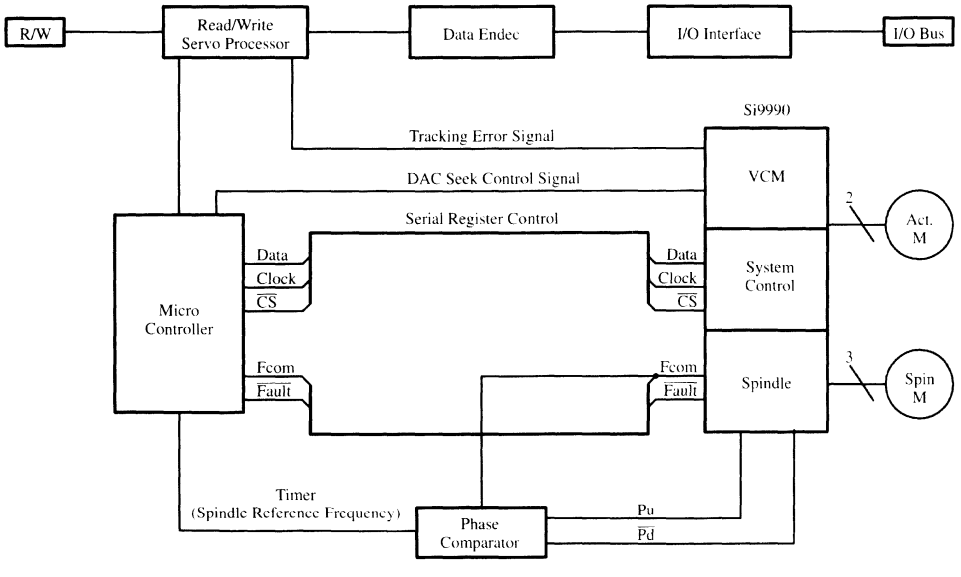


Figure 1. HDD block diagram

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The push to reduce access times has also caused a trend toward higher disk rotation speeds, which places greater accuracy constraints upon the spindle servo. Although the accuracy requirements are increased, spindle position control is a repetitive task which is best accomplished by dedicated hardware. By including spindle control functions and commutation logic in the Si9990CS servo IC, the processor is freed from these tasks and can perform the system control functions for which it is uniquely suited. The Si9990CS includes three n-channel MOSFET half-bridges for driving three-phase brushless dc motors. Phase commutation is based on back-EMF sensing circuitry which eliminates hall sensors and their associated cost and assembly problems.

During normal operation there is no interaction between the spindle and VCM drive circuits: both functions are under the control of the system microcontroller. The one exception to this rule is the head retract. When power is lost, the stored kinetic energy in the spindle can be used to power the VCM and reposition the head to its landing zone. The Si9990CS incorporates an integrated disconnect switch between the upper rail voltage to the spindle and VCM drivers (V_{MOT}) and the head retract circuit's supply voltage (V_{CLAMP}). This not only eliminates an external Schottky diode, but allows both servos to operate directly from the 5-V rail. When a power failure occurs, the disconnect switch prevents the power supply from pulling down V_{CLAMP} , and integrated rectifier diodes feed the motor back-EMF energy directly to the retract circuit.

The system interfaces for the Si9990CS are relatively simple in concept (Figure 1). Microcontroller commands use a serial input bus. The VCM driver receives the tracking error signal from the read/write servo processor and the seek control signal from the microcontroller via either a DAC (digital to analog converter) or PWM (pulse width modulation) signal. H-bridge outputs, OUT+ and OUT-, drive the head actuator. The spindle driver receives two inputs from the phase comparator and feeds two output signals back to the microcontroller. The output signals are F_{COM} from the back EMF commutation circuit and a $\overline{FAULT}$ output which indicates an under voltage condition. The spindle motor is driven by outputs A, B, and C. A detailed block diagram taken from the data sheet of the Si9990CS is shown in Figure 2 for reference. Refer to the data sheet for detailed information on the device specifications.

This application note will address the operation of the Si9990CS using design examples for both the head and spindle servos. First the serial control register will be explained, along with other system control functions. Either classical or state-variable techniques can be used for the loop analysis, and the former is applied here. The track-following loop is designed first, since parameters from this loop must be accounted for in the design of the seek loop. Block diagram reduction is performed to more easily determine the transfer function of the overall loop, while maintaining correspondence to the inner control loops. Having worked out the transfer functions, parameters for a specific example are entered to complete a numerical example. Finally, the design of snubber circuits for the VCM is discussed.

A similar procedure is then followed for the spindle drive: beginning with a description of the circuit, including an explanation of back-EMF sensing. Motor startup sequence problems are covered, and then the control loop is addressed in detail. After the block diagram is reduced, a design example is worked out. Lastly, snubber design for the spindle is covered.

System Control Functions

Serial Register

Refer to tables 1 and 2 in the Si9990CS data sheet and to Figure 13 in this Application Note. The mode control input (serial register) uses three lines: DATA (six bit command word), CLK (data bit clock), and CS/ (chip select input which allows the Si9990C S to latch in the new data word). With the $\overline{CS}$ pulled low, a six-bit word is entered into the data line. Bits D0, D1, and D4 define operating states for the VCM and spindle servos. D2 and D3 program the current limit thresh old for the spindle driver, and D5 is for a factory test mode. After the data has been loaded the $\overline{CS}$ pin should be returned to a high state, at which time the Si9990CS adopts the new operating state. The recommended data loading procedure is as follows:

1. Transition $\overline{CS}$ function to low while the clock is low.
2. Start the data clock and load D5 on the clock's low to high transition.
3. Return the clock low and make the D4 bit available.
4. Load D4 when the clock transitions low to high.
5. Repeat steps 3 and 4 for bits D3 through D0.
6. Return the clock to low.
7. Return the $\overline{CS}$ pin to a high level to activate the new data.

The serial register may be reloaded at any time during normal operation. When $\overline{CS}$ is transitioned to a low state, the present data is held, and the new data (e.g., a new value for spindle current limit) is loaded when $\overline{CS}$ returns to a high level.

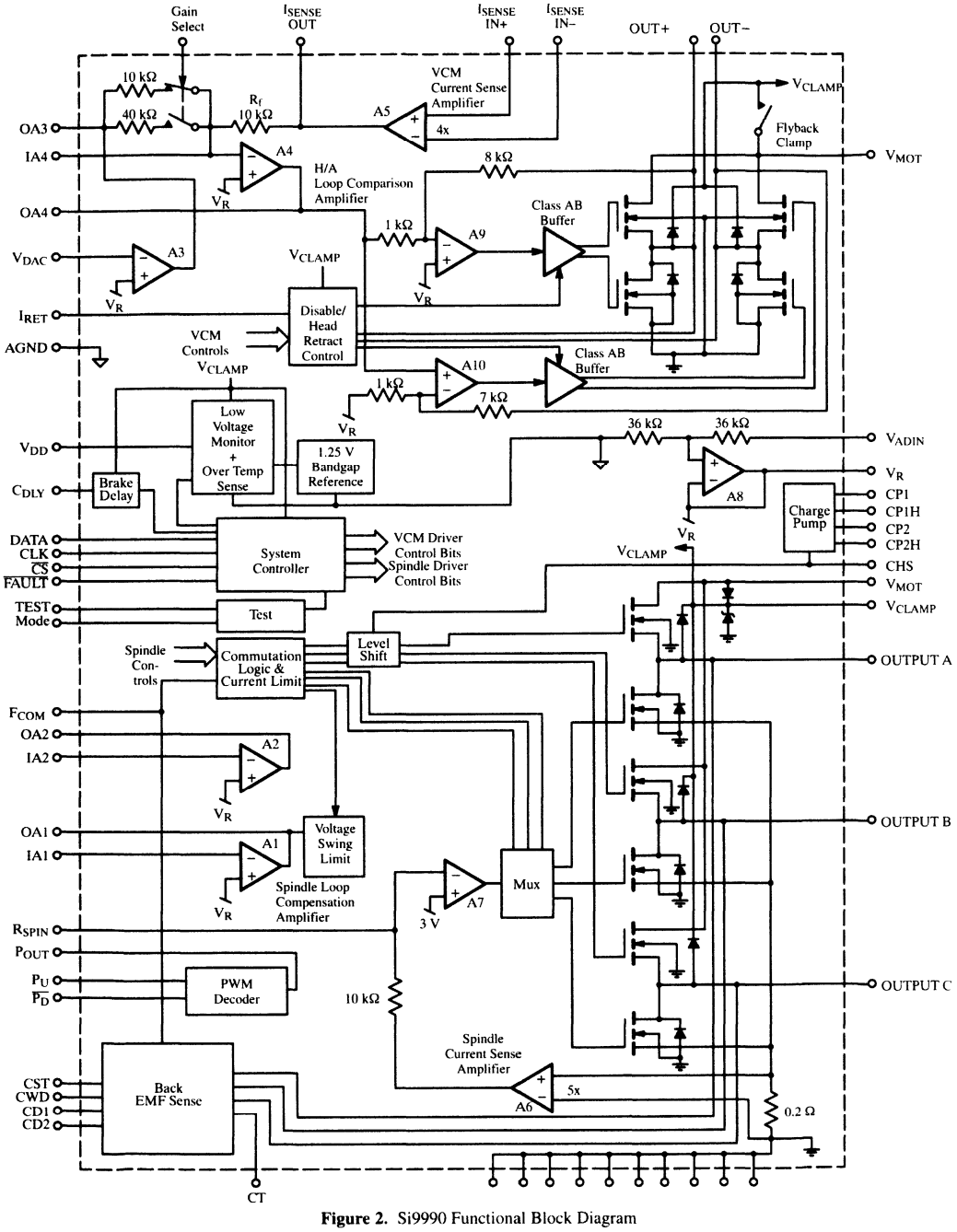


Figure 2. Si9990 Functional Block Diagram

Other Processor Control Functions

In addition to the mode control inputs from the microcontroller, $\overline{\text{FAULT}}$, F_{COM} , and I_{SENSE} OUT signals are provided for monitoring by the system microcontroller. $\overline{\text{FAULT}}$ is the under voltage flag which will be pulled low whenever the 5-V supply drops below 4.1 V typical (3.9 V minimum and 4.3 V maximum). F_{COM} pulses from the spindle drive commutation logic give position feedback to the microcontroller, which is used to determine when it is OK to read or write data. F_{COM} pulses occur N times per revolution of the spindle motor, where $N = N_{pl} \times N_{ph}$. N_{pl} is the number of motor poles and N_{ph} is the number of phases. I_{SENSE} OUT is the output from the VCM current sense amplifier, A5. It may be used for trajectory calculation in the seek mode, and it has a value of $4R_S$ volts/amp, where R_S is the actuator current sense resistor.

Voice Coil Motor

VCM Overview

The simplified schematic diagram of the VCM driver is given in Figure 3, with reference designations which are consistent with the detailed block diagram in Figure 2. The H-bridge, together with the class AB buffer drivers and amplifiers A9 and A10, comprise a transconductance amplifier with a differential gain of 16. This has been simplified to a single amplifier, A_G. The inverting input to A4 is the summing node for the track-following and seek control loop inputs, only one of which should be present at any given time. For track-following operation the parameter being controlled is the angular position, Θ (theta), and this is interchangeably referred to as the position loop. The track-following loop receives its error signal, shown as V_3, from the Read/Write Servo Processor. R_L, C_L, R_C, C_C, and R_2 form a feedback network around A4 to produce lead/lag compensation during operation in track-following mode.

A second input, V_{DAC} , to the inverting input of A3 is used for velocity control in the seek mode. The seek loop is also referred to as the velocity loop. Either a DAC or a PWM input from the microcontroller can be used for the control input during seek mode operation (Figure 4). The Si9990CS develops a reference voltage, V_R, equal to one half of the supply voltage. This buffered reference is used as the dc bias point for amplifiers A3 and A4, and is provided as an output from the Si9990CS. The DAC and tracking error signals must be referenced to this voltage. Gain switching in the transition between seek and track-following modes is accomplished using the Gain Select pin.

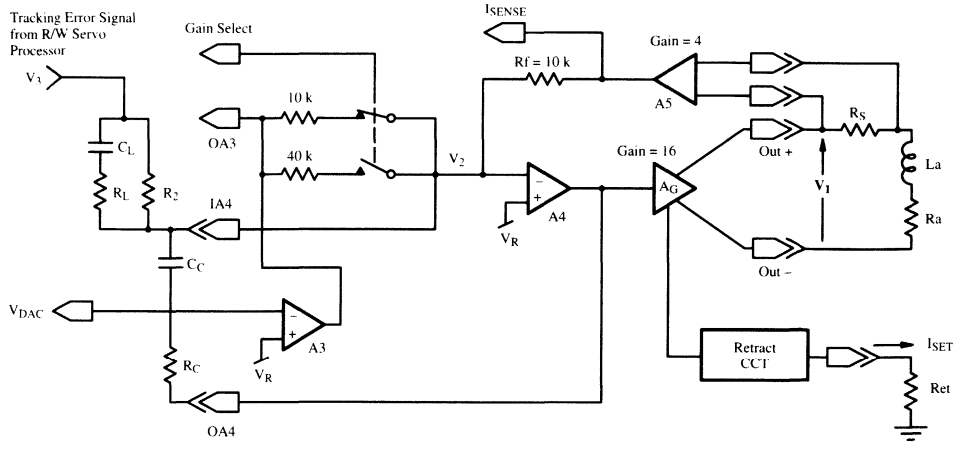


Figure 3. Simplified VCM Schematic

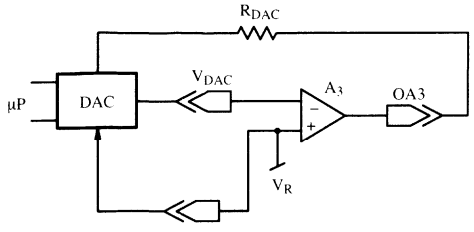


Figure 4 (a).
VCM Seek Input From The Microcontroller Using DAC

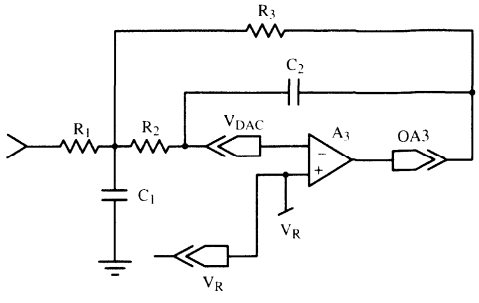


Figure 4 (b).
PWM Input to Velocity Loop (Seek Mode)

The servo design approach presented here first determines the compensation for the track-following loop. This will fix the values for R_C and C_C, which place a zero in the transfer function to cancel the higher of two poles from the motor back-EMF loop. These values then remain fixed, and are entered into the minor loop compensation block (Figure 5), which is common to both loops. With two integrations plus a first order lag in the position loop, a lead/lag compensation network is required. However, the velocity loop has only one integration, and the first order pole previously chosen in the analysis of the position loop is placed more than an order of magnitude above its crossover frequency. Thus, the loop is inherently stable for all usable crossover frequencies, and a simple feedback resistor is adequate for closing the loop around A3 (Figure 4 (a)).

We have not attempted here to provide algorithms for the seek routines, although we do perform an analysis to determine the gain parameter of the velocity loop for a given bandwidth. Realization of this gain will be a combination of hardware (a resistor) and calculations implemented in firmware. Nyquist considerations are mentioned below, but system armature resonance is not. Both of these considerations, however, will limit usable system bandwidth.

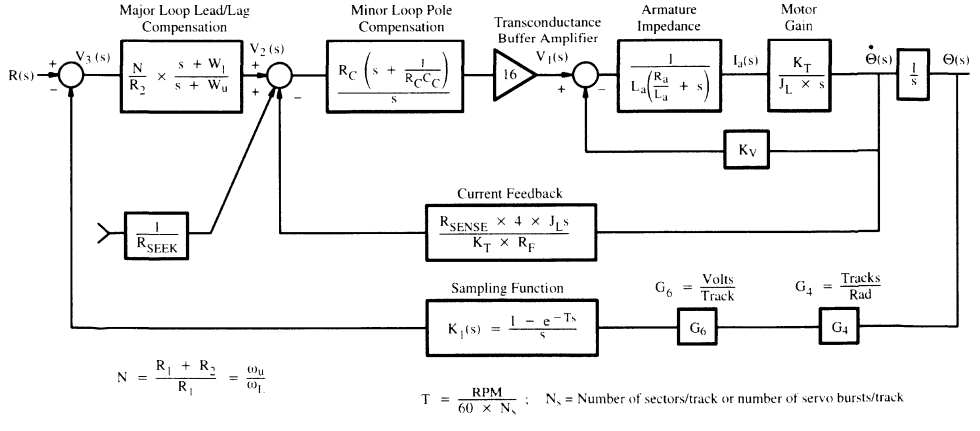


Figure 5. VCM Control Block Diagram

It does appear that sine (rather than sawtooth) profiles used in seek algorithms have a lesser tendency to excite armature resonances. The crossover performance exhibited in the Si9990CS VCM driver section addresses the often severe requirements imposed by the "flex circuit" mechanical bias, and linearity of control is maintained during transitions between velocity and position control modes.

During seek mode, the gain of the servo may be switched via the Gain Select pin. When this pin is in the high state, the gain is at its maximum value, and the voltage transference is given by

$$\frac{I_{SENSE}\ OUT}{OA3\ OUT} = 1\ \frac{A}{V}.$$

When the Gain Select pin is low, this gain is 0.25 A/V . In actuator current command terms, these gains represent $1/4R_S$ and $1/16R_S$, respectively, where R_S is the actuator current sense resistor. If needed, the I_{SENSE} OUT pin makes the actuator acceleration available for processing. The voltage out of the current amplifier is V_o , which is given as $V_o = 4 \times I_a \times R_s$ V/A, where I_a is the armature current. The acceleration, α, is given by

$$a = V_o \cdot K_t/(4R_s J_L) Rad/s^2.$$

Our control loop analysis proceeds with the development of the model for the plant, after which the block diagram is reduced for the position loop. Parameters for a typical example are inserted into the resulting transfer function to further illustrate the design method.

Plant Description

The plant of the VCM system consists of the load inertia, J_L, the torque and back EMF constants, K_t and K_v, and the winding electrical parameters, L_a and $R_a \times J_L$ is a function of the geometry and mass of the actuator arm. K_t and K_V are functions of the design strategy for the armature, which must produce the required force and acceleration and yet provide counter EMF values contained within the available supply voltage. The inductance, L_a, is determined by the magnetic field distribution in the armature winding, and R_a is the electrical resistance of the armature winding. Three parameters used in the analysis are derived as follows: $G_1 = K_t/J_L$, $G_2 = 1/L_a$, $\omega_a = R_a/L_a$. The actuator arm is modeled as a two-pole system, with the terminal voltage, $V_1(s)$, as the input and the velocity, $\dot{\Theta}$ (s), as the output (Figure 6(a)).The transfer function of the armature is given by Equation 1.

$$\frac{\dot{\Theta}(s)}{V_1(s)} = \frac{G_1G_2}{s^2 + s\omega_a + G_1G_2K_v}$$

The denominator normally represents an over-damped second-order equation with two well-separated poles, a and b. Factoring the denominator gives equation 2.

$$\frac{\dot{\Theta}(s)}{V_1(s)} = \frac{G_1G_2}{(s + a)(s + b)}$$

The pole at a is typically at a fraction of a Hertz, and the high-frequency pole at b occurs at a frequency on the order of 1 kHz. The phase lag of the high-frequency pole must be compensated by a zero in the forward gain block. This will be the first step in the design of the track-following loop.

Track-Following Loop

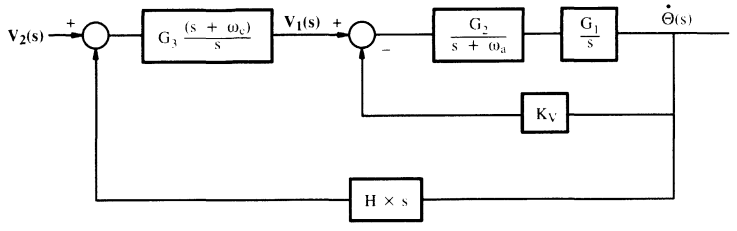
The next step is to determine the gain from $V_2(s)$ to $\dot{\Theta}$ (s). A forward compensator (Minor Loop Pole Compensation Block in Figure 5) places a zero to cancel the higher frequency pole (i.e., $\omega_c = 1/(2\pi R_C C_C) = b$). This cancels the second first order lag, thus allowing a smaller compensation capacitor value to be used. Terms are defined as follows for the Current Feedback Block. R_f is the internal 10-kΩ feedback resistor through which the output from the current amplifier, A5, is summed into the control loop amplifier. R_{SENSE} is the current sense resistor. $H = R_{sense} \times G_5/(R_f \times G_1)$, G_3 is the gain to be solved for pole placement (Figure 6(a)). With cancellation of the pole at "b", the resulting forward block of the current loop then reduces to:

$$\frac{G_1G_2G_3}{s(s + a)}$$

Overall minor loop block then, reduces to

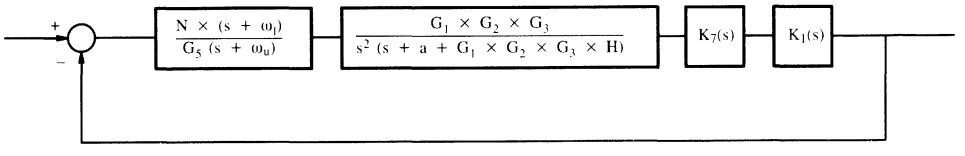
$$\frac{\dot{\Theta}(s)}{V_3(s)} = \frac{G_1G_2G_3}{s(s + a + G_1G_3H)}$$

The position (track following) loop shown in Figure 6(b) includes the lead/lag compensation, gains, and the final integration. To complete the overall loop the following parameters are defined. ω_u is the pole and ω_l is the zero of the lead/lag compensation network. N is the gain ratio of this network. K_1 is the sample function gain, which is unity for normal choices of sampling frequency. K_7 is the conversion gain of the output function, which converts radians to number of tracks and the number of tracks to volts/track. R is the arm radius; TPI is the tracks per inch; V_{tt} is the volts/track.



$G_3 \triangleq R_c \times 16$; $G_2 \triangleq \frac{1}{L_a}$; $G_1 \triangleq \frac{K_t}{J_L}$; $H \triangleq \frac{R_{SENSE} \times G_3}{G_1 \times R_F}$ $G_5 \triangleq$ Sense Amp Gain ; $R_{SENSE} \triangleq$ Current Sense Resistor

Figure 6(a). VCM Current Control Loop Block Diagram



$\frac{\#Tracks}{Inch} \times \frac{Inches}{Radian} \times \frac{Volts}{Track} = K_7$ Volts/Radian Position – Track Following Loop

Figure 6(b). VCM Block Diagram Reduction—Unity Feedback Form

$$K_1 = \frac{(1 - e^{-sT})}{S}; \quad K_7 = R \times TPI \times V_{tt}$$

Assuming that the sampling frequency is adequate, K_1 can be neglected. The compensator gain, K_n includes K_7, G_5 and N, which is defined below. We can further simplify by including the final integration in the compensator block, and then evaluate each block separately. The transfer function for the compensator block then becomes

$$\frac{K_n(s + \omega_1)}{s(s + \omega_u)}$$

Define ω_x as the crossover frequency. Noting that the system has two integrations and a pole at $a + G_1G_2G_3H$, choose this pole to be at $F\omega_x$. Solving for G_3 gives

$$G_3 = \frac{F\omega_x - a}{G_1G_2H}$$

Substitute for G_3 in equation (4) to give

$$\frac{\dot{\Theta}(s)}{V_2(s)} = \frac{F\omega_x - a}{H \times s(s + F\omega_x)}$$

To guide the following parameter choice, it is necessary to evaluate the open loop transfer function at ω_x, with the condition that the gain is unity at this radian frequency. Choose N to maintain a phase margin of 45 degrees at crossover. Remember that the sampler may well introduce some phase lag, depending on the ratio of the sampling frequency to ω_x. Also, any noise filter, together with a peak detector filter, will contribute further phase lags. Thus N may need to be higher. A good minimal choice for N is 10. This will probably give the desired phase margin without sacrificing system noise performance.

With ω_x and N chosen, a solution for G_5 may be found. H could be minimally changed, as can the value of the summing resistor for the K_7 function. However, a solution for G_5 will be found with the example values given below. Set the open loop gain to unity at ω_x.

Combining (5) and (7)

$$\text{Mag.}\ \frac{K_n(s + \omega_1)(F\omega_x - a)}{H \times s^2(s + \omega_u)(s + F\omega_x)} = \text{Unity}$$

Substitute for "s," and solving for K_n at ω_x:

$$K_n = \frac{H\omega_x^2\left(j + N\frac{1}{2}\right)(j + F)}{\left(j + \frac{1}{N\frac{1}{2}}\right)\left(F - \frac{a}{\omega_x}\right)}$$

VCM Design Example (cgs units)

Motor Torque Constant	K_t	=	6
Back EMF constant	K_v	=	0.024
Arm. Inertia	J_L	=	$6.3e^{-4}$
Arm. Inductance	L_a	=	$4.7e^{-3}$
Arm. Resistance	R_a	=	12
Current Sense	R_s	=	1
Sense Feedback Res.	R_f	=	$1e^4$
Sense Amp Gain	G_s	=	4
Lead Network Ratio	N	=	10
Cross-Over Freq.	ω_x	=	400 × 2π
Actuator Arm Radius	R	=	2 ins
Tracks/Inch	TPI	=	2500
Volts/Track	V_{tt}	=	2.5

$G_1 = 9.523e^3$; $G_2 = 213$; $G_1G_2 = 2.026e^6$;
$K_7 = R*TPI*V_{tt} = 1.25e^4$;

$K_n = K_7*N/G5$; $K_n = 1.25e^5/G5$; $H = 4.2e^{-8}$

The transference of the back EMF loop is:

$$\frac{2e^6}{s^2 + s \times 2.55e^3 + 4.8e^3}$$

Factoring

$$\frac{2e^6}{(s + 18.96)(s + 2.53e^3)}$$

Use $b = 2.5e^3$ (smaller C_x); a = 18.96

Next solve for the current feedback loop. Since first order pole should be absolute minimum of 10 ω_x, make F = 20.

Then $G3 = 5.98e^5$; $R_c = G_3/16 = 36.9k$;
$C_c = 1/(Rc*b) = 0.01\ \mu F$.

From 9 Solve for K_n:

$$K_n = \frac{4.2e^{-8} \times 6.31e^6(j + 3.16)}{(j + 0.316)(20 - 7.54e^{-3})} = 0.8748$$

$R_2 = G_5 = 1.25e^5/0.8748 = 142$ k, with N = 10,
$R_1 = 142\ k/9 = 15.6$ k

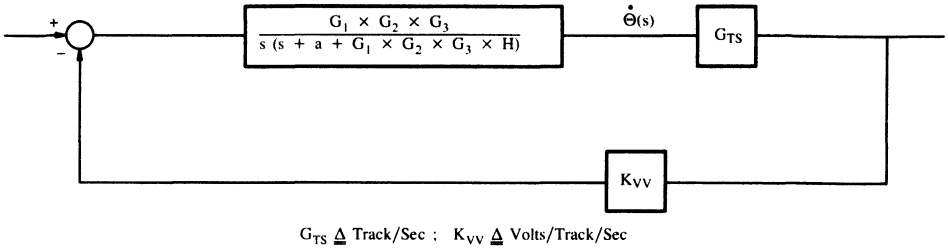
Then lead/lag capacitor is
$C_1 = 1/(3.16 \times 400 \times 2 \times \pi \times 15.6e^3) = 8.2$ nF

VCM Seek Loop

Figure 7 shows VCM velocity loop block diagram .

The lead/lag network is not needed for loop compensation. The input from either a DAC or a PWM signal, is via A3 at Vdac input (Figure 3) . Two methods shown in figures 4 (a) and (b) indicate the needed circuitry to accommodate the two methods. The transference of the network in Figure 4(b) is:

$$\frac{\Theta o(s)}{\Theta i(s)} = \frac{1}{\frac{s^2}{\omega n^2} + ((s \times 2\xi)/\omega n) + 1}$$



$G_{TS} \triangleq$ Track/Sec ; $K_{VV} \triangleq$ Volts/Track/Sec

Figure 7. Velocity Control Loop Block Diagram (VCM Seek Mode)

$\omega_n = \sqrt{[1/(R_2 \times R_3 \times C_1 \times C_2)]}$;
$\xi = \omega_n \times C_2 \times [R_2 \times (1 + R_3/R_1) + R_3]/2$

A good choice for this network is to set ξ to 0.707 and ωn to a minimum of 10 times the position loop cross-over frequency.

Seek Mode/Actuator Gain

Gain: Command gain ≡ Iactuator/V(OA3) = 0.25/Rs Amps/Volt.

V(OA3) is either the PWM filter or the DAC output and Rs is the Current sense resistor.

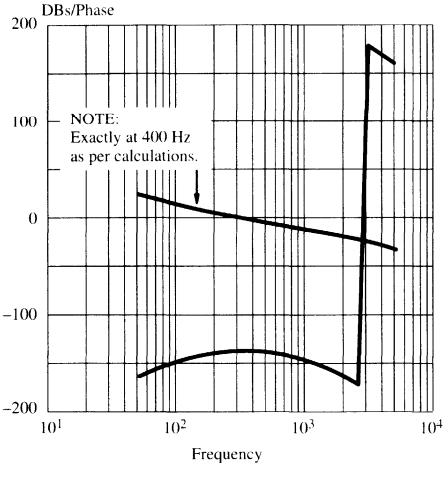


Chart 1. VCM Open Loop Plot.

Snubber Design

Actuator inductive load compensation.

Refer to data sheet for the Si9990CS Page 10.

Four components (C_{14}, C_{15}, R_{14}, and R_{15}) are shown connected from outputs OUT+ (pins 5 and 6) and OUT- (pins 9 and 10). An alternate configuration may be used. For example, a series combination of a resistor and capacitor can be connected between the out put terminals (in parallel with the actuator load).

These components compensate for the inductive behavior of the actuator load with increasing frequency. These components are important in that they suppress any tendency of the output driver to oscillate.

To choose the components, the suggested rules are as follows:

1. Choose compensating capacitor C_{14}, to resonate with the actuator inductance La at a minimum of 20 times servo cross-over frequency.
2. Choose compensating resistor $R_{14} = \sqrt{(4 \times La/Cc)}$. This choice ensures that damping will be critical.

Example: La = 4 mH and servo cross-over is 450 Hz.

Then:

$$C_{14} = \frac{1}{(2 \times \pi \times 20 \times 450)^2 \times 4e^{-3}} = 068\ \mu f$$

$$R_{14} = \sqrt{(4 \times 4e^{-3}/0.068e^{-6})} = 240\ \Omega$$

Note: If four components are used, two from each output to ground Cc' value must be doubled and each Rc halved.

Spindle Motor Drive

The commutation function in the Si9990CS uses an integrated solution requiring no intervention on the part of the processor to maintain spindle function. By using a combination of digital and analog techniques, the level of noise masking performance is excellent.

Status signals, Fcom and $\overline{\text{FAULT}}$, are output to the controller. Fcom indicates spindle condition in either acquisition or phase locked modes, and $\overline{\text{FAULT}}$ indicates a low-voltage condition.

Finally, the Spindle phase locked loop is controlled by an external phase comparator whose outputs (Pu and $\overline{\text{Pd}}$) control an internal charge pump, and inputs comprise a reference frequency from the processor and Fcom (motor feedback position signal).

Spindle velocity mode operation can be implemented by the processor without using the phase comparator, if the control signal is applied to IA2 via a resistor.

Commutation and Back-EMF Sensing

The method of commutation is referred to as "Back EMF Commutation." A clocked state machine advances one "state" after each back EMF zero crossing. This clock is produced by a "Back EMF" comparator which compares

the selected "off" phase induced voltage, with respect to the winding center tap.

The state machine's outputs are decoded to switch the selected upper MOSFET transistor, and one end of the phase pair connected to it, and a lower, linear controlled MOSFET, connected to the other end of the phase pair (Figure 9 (f-h)). Note that switching only occurs to one end of the phase pair at any one time. Inspection of Phase A at the center of the On (High) interval corresponds with Phase B going off.

Figures 9 (a) and 9 (c) indicate a 30-degree lag between the comparator clock pulse and the phase switching pulses initiating the next state. Align Zc, during A(off) period. (See Figure 9 (a) and the commencement of the ramp down in Figure 9 (c).)

Capacitors CD1 and CD2 are alternately charged (positive slope) and discharged (figures 9 (b) and 9 (c)). CD1 and CD2 are caused to commence their discharge, alternately, at each zero crossing. See Zc on Figure 9 (a).

The capacitors are charged with 10 µA and discharged with 20 µA. Thus, each capacitor charges from a fixed threshold for 60 electrical degrees at 10 µA. The charge is then held at the onset of the phase switching pulse until the next back EMF pulse, at which time it discharges at 20 µA and a new phase switching pulse occurs when the fixed threshold is reached. This pulse is thus delayed 30 electrical degrees after the back EMF pulse which initiated its discharge.

When this threshold is reached, the capacitor begins to repeat the previous cycle, charging at 10 µA. The other delay capacitor is in the hold mode at this time, and in turn, will commence its discharge when the next back EMF pulse arrives.

It should be noted that the state machine produces a switching pulse only when either of the delay capacitors reaches its discharge threshold.

Motor Startup Sequence

At start, clock pulses are provided by a start oscillator until back EMF pulses are available.

Starting Conditions.

Three conditions prevail during a start operation:

1. The motor does not move. Since there is an entirely arbitrary correspondence between the state of the state machine and the motor pole/winding, inadequate torque may be produced to allow the motor to start. In this case, after a given time, another oscillator pulse advances the state machine.
2. The motor reverses. The polarity of the slope of the next Back EMF is anticipated by the state machine. If it is incorrect, the state machine is advanced after a suitable delay.
3. The motor starts and the anticipated Back EMF pulse occurs. The oscillator is inhibited, and commutation proceeds normally.

Cases 1 and 3 are straightforward. In Case 1, the oscillator continues to advance the state machine until Case 3 occurs.

Case 2, however, is not so quite so straightforward. Refer to Figure 10 (c) - (f).

In normal operation (Figure 10 (a) and (b)) the fly-back pulse **crosses** and **uncrosses** the zero crossing threshold. The next zero crossing is the "wanted" pulse. The fly-back pulse, which returns the stored armature inductive energy ($1/2\ La*Ia^2$), to the power supply, must still occur, but its trailing edge merges with the "off" winding induced voltage, which, in this case, is the same potential at which the fly-back pulse was clamped (Figure 10 (c)).

The operation of capacitor CWD is shown in normal operation, ramping down after the trailing edge of the fly-back pulse (Figure 10 (e)). In reverse operation, it continues to charge to a fixed potential and then to discharge at the next zero crossing to its onset value, at which time a state clock pulse is output to continue commutation (Figures 10 (f) and (g)).

In the normal case, where the motor is running in the desired direction, the fly-back pulse is caused to return to its onset potential, i.e. the potential of the Back EMF wave form.

For each occurrence of a zero crossing, the start oscillator is inhibited from clocking the system. If the motor does not move, then the start oscillator will output a further pulse to advance the state machine and continue commutation until zero crossings are available.

Choosing the Start Oscillator Frequency

The torque on the motor is a Sine function of the angle between pole and the winding and the applied current.

Since all positions of pole to winding angle are possible, the average torque will be used, as shown below.

Torque: $Tm = Ip \times Kt/\pi$ (1)

Acceleration (include total inertia) $\alpha = Tm/Jl$ (2)

It is necessary to find the motor radian distance between states of the state machine, and to determine how long it takes the rotor to move this distance in response to applied current step.

Radian distance: $r = 2\pi/(Npl \times Nph)$ (3)

(Npl # of poles, Nph # of phases)

Time: $tl = \sqrt{(r \times 2/\alpha)}$ (4)

Thus, the maximum frequency of the start oscillator is given by:

$Fs = 1/tl$ (5)

In practice Fs should be a little lower than this.

Using the motor torque constant Kv find back EMF for motor speed at the end of one pulse.

Back EMF volts:

$V_b = Kv \times tl \times \alpha$ (6)

An example. (Units in CGS).

$Kt = 1$, $Kv = 8e^{-3}$, $Npl = 12$, $Nph = 3$, $Jl = 7.5e^{-4}$, $Ip = 0.5$ A

$\alpha = 0.5/(\pi \times 7.5e^{-4}) = 212$ Rad/sec^2

$tl = \sqrt{(4\pi/(36 \times 212)} = 0.0405$ sec

$Fs = 1/tl = 25$ Hz

$Vb = 8e^{-3} \times 0.0405 \times 0.212 = 0.0686$ V

Choose CD1 and CD2.

Calculate the time between states at the running speed of the motor.

Time between states:

$Ts = 60/(RPM \times Npl \times Nph)$

Do not use this time directly in subsequent calculations, because the motor will overshoot the running speed and it is necessary to maintain a linear system, even in the acquisition mode.

A suitable figure would be a 140% overshoot. Use Ts/1.4. Use a delta v (charge) of 2 V at 10 μA.

Therefore:

CD1 and CD2 = $(10e^{-6} \times Ts/(1.4 \times 2)$ Farads.

Start Capacitor CST.

Choosing Values for the start oscillator capacitor.

CST is charged and discharged at 5 μA, from 0.5 to 2.5 V. Thus the value of CST for 25 Hz (calculated earlier) is:

Start Capacitor value:

$CST = 5e^{-6}/(2 \times 25 \times 2) = 47$ nF.

Delay Capacitor CWD.

See Figures 10 (e) and 10 (g).

In normal operation CWD is charged with 5 μA until the "fly-back" switching pulse uncrosses the zero crossing, at which time discharge is initiated at 25 μA.

In a reverse rotation condition, the fly-back does not uncross the zero crossing, so CWD continues charging towards 2.5 V. A discharge at 25 μA is initiated either when the back EMF voltage crosses zero or when the charging voltage reaches 2.5 V. At the completion of discharge, a clock pulse is output to advance the state machine.

Thus, normal clock pulse generation only occurs, for a zero crossing, after CWD has completed its discharge. Otherwise a clock only occurs after CWD has discharged from a potential of 2.5 V or from a zero crossing of a reverse rotation wave form.

To take an example, let us assume that start oscillator frequency, the period to traverse the distance between states, is:

$tl = 0.0405$ seconds.

Obviously this will also be true for reverse rotation, since CWD charges at 5 μA from 0.5 to 2.5 V. Using a delta of

2 V and Ic of 5 μA and, assuming that zero crossing will occur in one half this distance, then the time will be:

$tl/\sqrt{(2)} = 0.028$ seconds.

Thus:

$CWD = 5e^{-6} \times 0.028/2 = 68$ nF.

Spindle Overview

We present here a servo design procedure which uses a conditionally stable servo, i.e. an integrator with a zero.

We have included a set of considerations to aid in the choice of crossover frequency. When these guidelines are followed, the resulting servo has a bandwidth on the order of 10 Hz. For systems using a single platter with diameters of two and a half inches and below, motor gain is very high (Torque/Inertia ratio). In order to achieve cross-over frequencies in the region of 10 Hz, gain reducing techniques are needed. The simplest method is to design with a very low dc gain, although this approach poses some significant problems:

1. The reference for the transconductance amplifier is 3-V source, whereas all other op amp references are $V_{DD}/2$. The 3-V value is chosen in order facilitate control of the current limit and to provide a reasonable dynamic range of the input signal to the transconductance amplifier. This input commands armature current in only one direction, so any input more positive than the reference has no effect, and the voltage range above the reference is wasted! The approximate half-volt differential between $V_{DD}/2$ and 3 V forces significant error voltage offsets from the phase comparator. A dc gain of 0.25 would yield a 2-V offset, and the phase comparator output would be at 4.5 V.

2. The tri-state output at Pout (phase comp charge pump) has the upper switch connected to V_{DD}. Thus, modulation of the power supply impedance, significant value with battery powered laptops, is present at Pout. However, it is also present at $V_{DD}/2$; so if Pout's operating point is at $V_{DD}/2$ (high gain system), this modulation is common moded out.

For these reasons, use of an integrator is recommended. A second option is available, but cancellation of the power supply impedance effect is less complete. This alternative method is to divide the Fcom pulses by, for example, up to 36 for a three-phase twelve-pole motor. This method may require some rather large time constant. With an operation speed of 60 RPS (3600 RPM), cross-over frequencies of 5 Hz might be used.

Phase Comparators

The very well known phase comparator using dual D flip flops and a nand gate for reset, or similar versions thereof, can provide problems in acquisition. When out of the phase lock region, the average output is a function of the beat frequency between the reference and tach (Fcom) frequency. Under these conditions, a velocity mode prevails, an integration is lost, gain goes up, and the system oscillates near the frequency of the first-order filter about one order above the designed cross-over frequency.

This problem will tend to be more likely if high ratios of lead/lag break frequencies are used. Designs following suggestions outlined later in this note have not exhibited this problem thus far. If processor control of the Pu and $\overline{Pd}$ signals is available, and a window around the desired Fcom period is used to hold either of these signals appropriately, acquisition time is greatly improved and the potential for a "velocity" mode problem, as described above, no longer exists.

Advantages of the Si9990CS

1. VCM and Spindle functions are implemented in a small 64-pin SQFP, requiring minimal board space.

2. The full H-bridge function in the VCM, and the half bridge functions in the Spindle section, have drivers which fully utilize Siliconix expertise in power MOSFET technology. The resulting, fully integrated package results in shoot-through protection, together with switching regimes, ensuring safe operation with the inductive loads.

3. The Clamp in the VCM circuit eliminates the need for a diode, with its attendant voltage drop, thus providing more voltage during retract operation when using the stored energy (back EMF) from the Spindle Motor.

4. A very robust method is used for back EMF commutation. An effective masking operation renders the Spindle control circuitry immune to noise spikes.

5. Very low cross-over distortion performance is available in the VCM section. This feature is necessary for proper operation, when the transition from seek to track following mode occurs, where distortion currents must produce torques significantly lower than the "Flex circuit" bias.

6. The ability to provide internally all VCM and repetitive, commutation functions, the processor is thus freed to address more important functions, i.e. seek and read/write control. These latter needs fully exploit the processor's computational ability.

Spindle System Block Diagram

The inputs to spindle controller are via PU and $\overline{PD}$. These are outputs from a phase comparator of the edge controlled type. The output from such a comparator in the phase locked mode are short pulses alternately positive (Ground to V_{CC}) and negative (V_{CC} to Ground). They are thus low-energy pulses and easy to filter. This the case for a high gain system, typically one with an integrator.

These outputs are input to a tri-state switch via (PU and $\overline{PD}$) which provides a further reduction in noise, i.e. when the error is small the signal at the switch output (Pout) is in a tri-state condition. Further, when the system is either above or below the required velocity, the outputs are pulsed either from Vr to V_{CC} or Vr to ground. Thus there is no ambiguity in the dc level with respect to Vr. This ensures that a lock condition may only occur at the frequency of the reference and not a multiple or sub-multiple thereof.

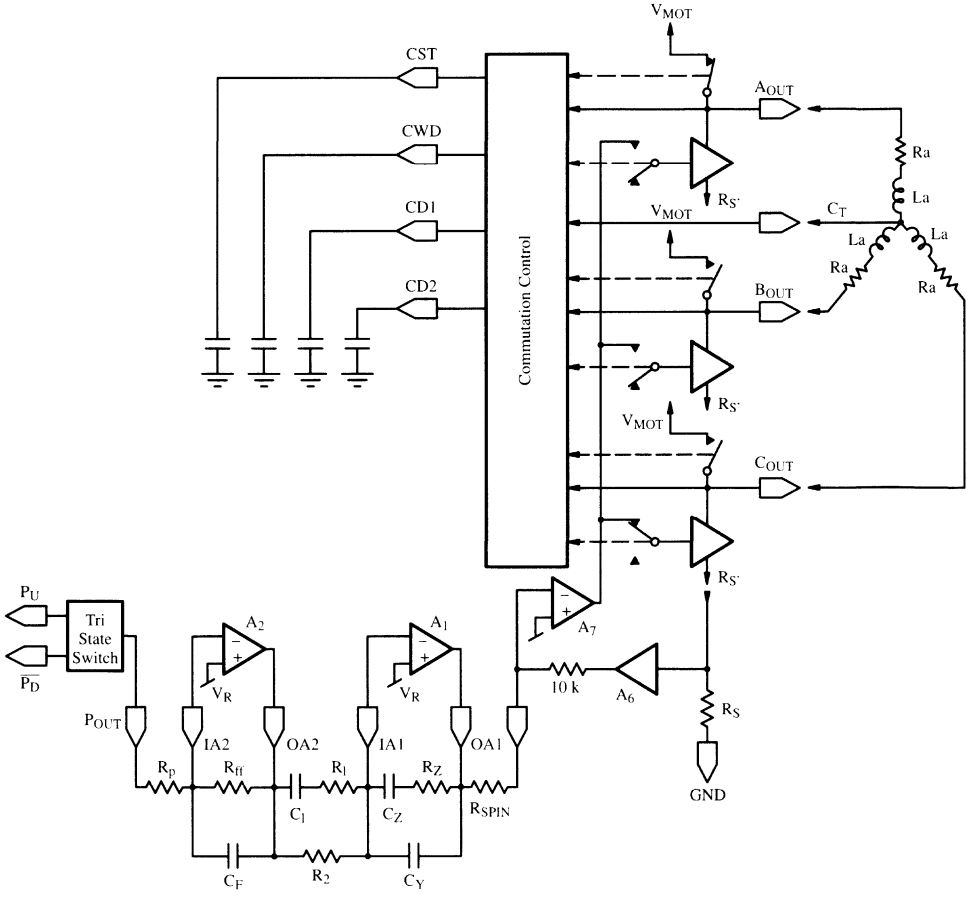


Figure 8. Spindle Driver Simplified Block Diagram

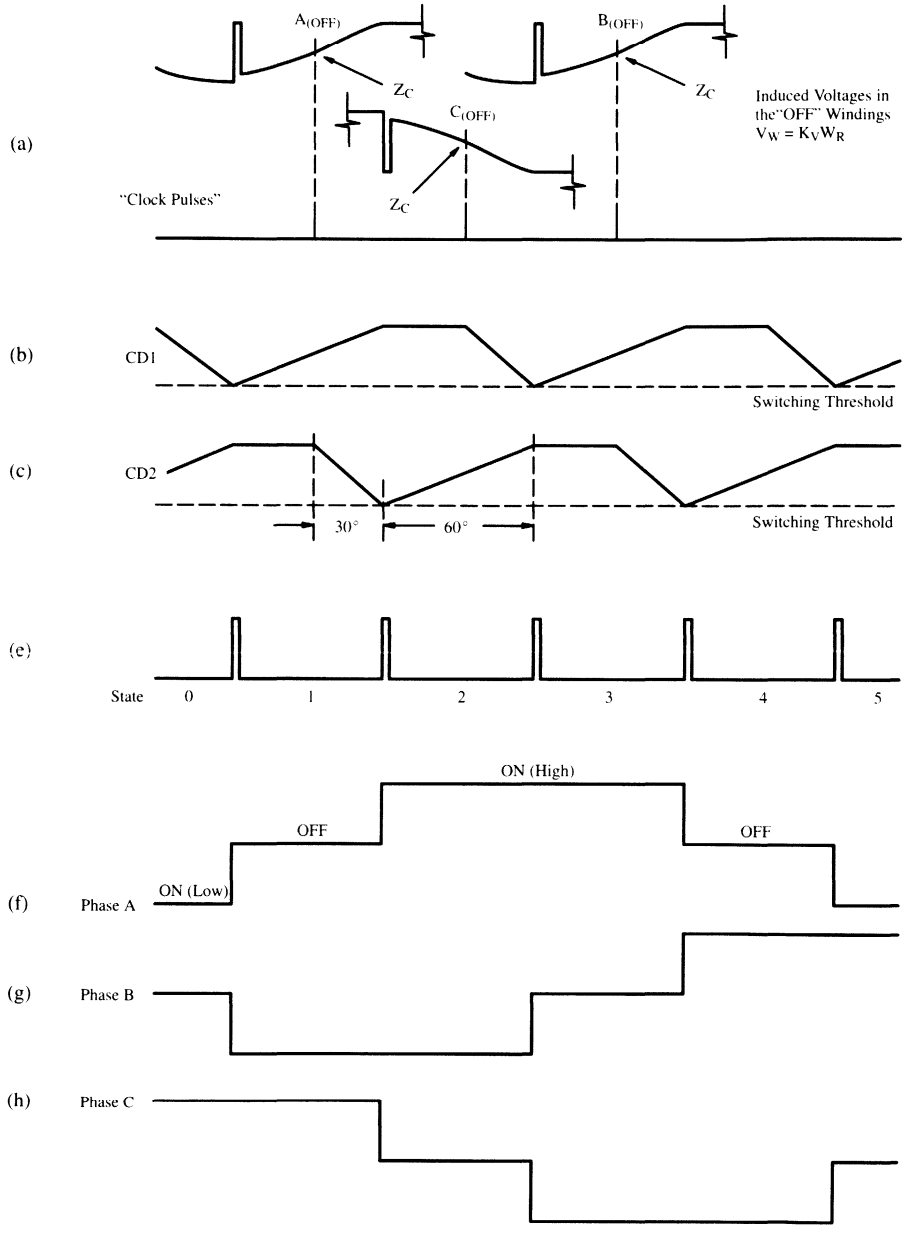


Figure 9. Spindle Driver Waveforms—Normal Operation

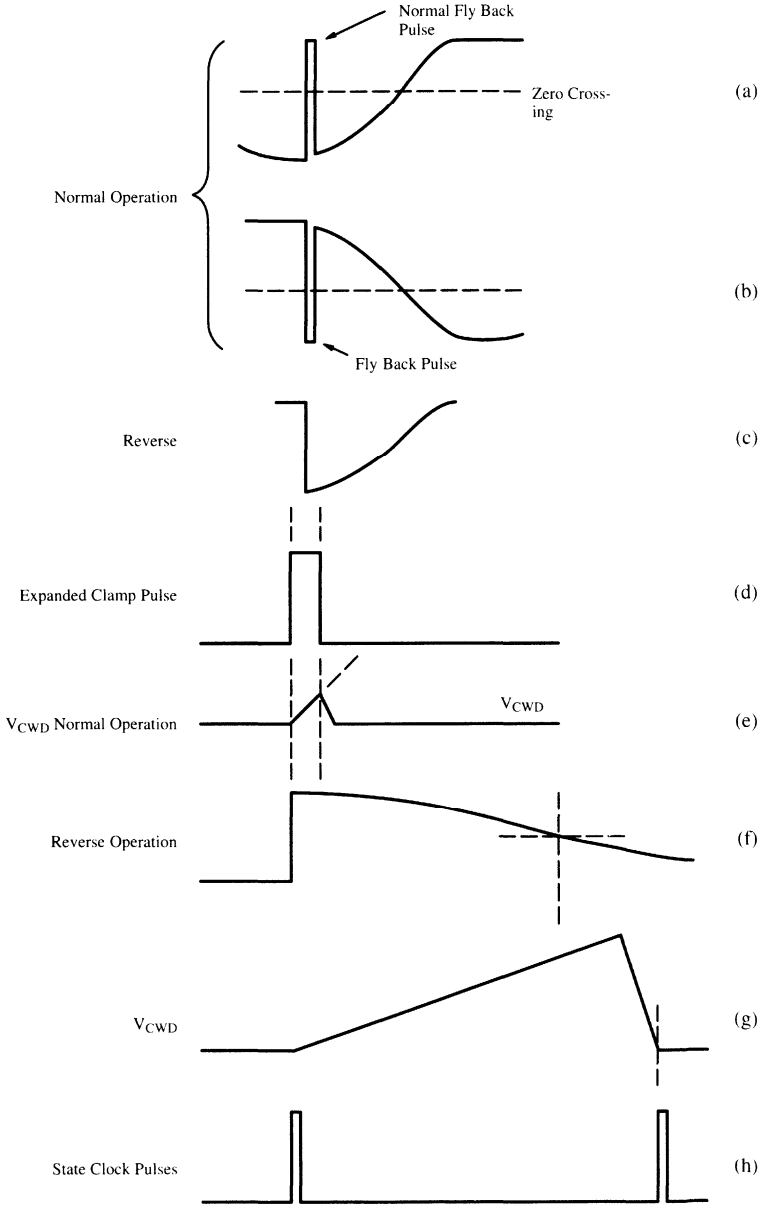


Figure 10. Spindle Driver Waveforms—Startup Operation

The output at Pout is applied via Rp and IA2 to amplifier A2. This amplifier is configured as a low pas filter. Note that there are no frequency-dependent components in the input circuit. As indicated above, when using a high gain system, the error at Pout will be essentially at V_R. Thus, voltages developed across the power supply source impedance by spindle and VCM current demands will be **common moded** out, since both the tri-state switch and V_R are supplied from V_{DD}. Between OA2 and IA1, components R_2, Cl and Rl form the Lead/Lag network series compensator for the loop. The closure components for A1, Cz, Rz, and Cy form an integrator with zero, and a second low pass filter.

The output from A1 is fed via Rspin, to the transconductance amplifier A7. Here the output of the current sense amplifier (A6) is mixed via Rf, an internal component, with the inputs through Rspin, to set the transconductance gain . Rs (the current sense resistor) is also internal. By excellent ratiometric matching, the transconductance gain is accurately set by Rspin.

In Figure 8, the output of A7 is multiplexed to one of three output drivers. The output from the selected driver (Cout is shown in the diagram) linearly controls the "sink" current through the two series connected phases to an upper switch (Aout is shown in the diagram).

Spindle Servo Design Procedure

Design of a Conditionally Stable Servo

Suggested Rules:

(a) Cross-over Frequency = ω_x

1. Make integrator zero $\omega_z = \omega_x/10$

2. Lead n/w gain ratio $N = \omega_u/\omega_l$

3. Make lag n/w break $\omega_u = (\sqrt{N}) \times \omega_x$

4. Make lead n/w break $\omega_l = \omega_x/\sqrt{(N)}$

Choose N(12 - 14). Choose Noise Filter poles, ω_p and ω_q as 10 ω_x and 15 ω_x. Since ω_p and ω_q introduce additional lags at ωx, N is chosen to provide needed compensation for an overall phase margin of 45 degrees (Figure 12 (d)).

(b) Rewrite Transfer Function in terms of ω_x, i .e $(s + \omega_l)$ goes over to $(s + \omega_x/\sqrt{(N)})$.

(c) Equate the Transference of all blocks, Fig 12 (e), evaluated at ω_x, to unity.

(d) Solve for ω_y.

(e) Evaluate component values for Fig 8.

Spindle Servo

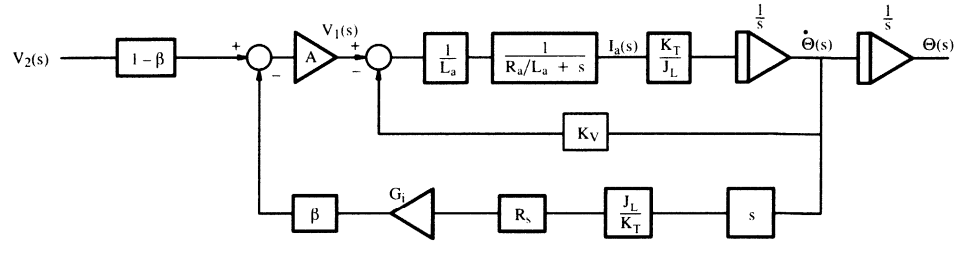
Plant

The plant for the Spindle servo comprises the motor with the following parameters:

Torque Constant Kt; Back EMF Constant Kv;
Armature Inductance La; Armature Resistance Ra;
Rotor and Load Inertia J_l

Define: $G1 = K_t/J_l$; $G2 = 1/L_a$; $\omega a = R_a/L_a$

The suggested procedure is to reduce the minor loops from Figure 11 to an equivalent block (Figures 12 (a), (b) and (c)).



$$G_1 = \frac{K_T}{J_L} \; ; \; G_2 = \frac{1}{L_a} \; ; \; H = \frac{G_i \times R_s \times \beta}{G_1} \; ; \; \omega_a = \frac{R_a}{L_a}$$

Figure 11. Spindle Control Loop Block Diagram

Rather than using the simplification of ignoring the back EMF and inductance parameters of the motor and simply using the transconductance gain times the error volts and the motor torque constant, the entire loop is included in this analysis for completeness.

The reduction to block (c) in Figure 12 results in a transference which may appear to be influenced by the variability of the open loop gain of the transconductance amplifier. If, however, an evaluation of the function magnitude is made at omega (ω) = to unity, it will be evident that the magnitude function, changes imperceptibly when A, the open loop gain, varies from, say, 10 K to 50 K.

The current feedback loop uses sensed motor current with the "pick off" point moved forward to the velocity output $\dot{\Theta}(s)$. The inverse of the forward functions traversed to this point are then inserted in the return loop. For example, K_t/J_1 and 1/s in the forward loop go over to $s \times J_1/K_t$ in the return loop.

The reduction of the Back EMF block becomes a quadratic function yielding an over-damped solution, with a pole well above a normal spindle servo bandwidth, and a sub-radian pole, approximating a first order lag if the high-frequency pole is disregarded.

Block Diagram Reduction

Reference Figure 12 (b).

Back EMF Loop.

$$\frac{\dot{\Theta}(s)}{V1(s)} = \frac{G_1G_2}{s^2 + s\omega_a + G_1G_2Kv}$$

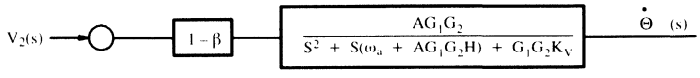


Figure 12(c). Spindle Control Loop Block Diagram Reduction – Step 3

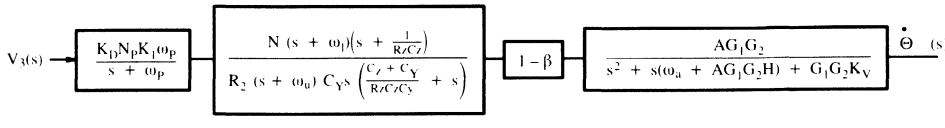


Figure 12(d). Spindle Control Loop Block Diagram Reduction – Step 4

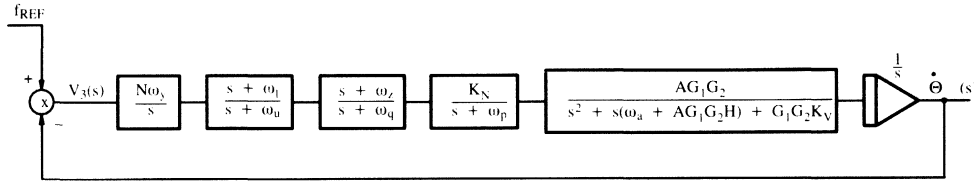


Figure 12(e). Spindle Control Loop Block Diagram Including Final Integration and Phase Comparator

Current Loop

Defining further parameters:

Current Sense resistor Rs; current sense amplifier Gi; and current loop summing ratio β; the ratio of Rspin to the internal feedback resistor Rs:

β = Rspin/(Rspin + Rf); Transconductance amplifier open loop gain = A;

$H = Gi \times Rs \times \beta / G_I$;

$$\frac{\dot{\Theta}(s)}{V2(s)} = \frac{AG_1G_2}{s^2 + s(\omega_a + G_1G_2AH) + G_1G_2Kv}$$

Spindle Design Example

Example.:

Design a servo (conditionally stable type) to run a motor at 3600 RPM with a cross-over frequency of 10 Hz. Motor has 3 phases and 12 poles, thus there are 3 × 12 = 36 pulses per revolution.

The most significant perturbating sources in the motor will at the running frequency RPM/60 and, for a three phase motor, at three times the running frequency.

The upper bandwidth choices are limited by the sampling frequency and the need to attenuate the third harmonic of the running frequency. This harmonic is seen as a POSITION pulse disturbance, thus some method of averaging out this component is mandatory. Thus the bandwidth may not be chosen to be above the running frequency, in an attempt to enclose the once around disturbance because there will not be adequate attenuation of the third harmonic.

In choosing a cross-over frequency below the once-around frequency, said frequency must be low enough to attenuate the once-around adequately. Too low a choice will result in an inadequate rise time (approximately; Tr = .35/Fxver) and will also require large time constants with attendant large capacitors.A cross-over of 10 Hz will provide approximately 31 dB of attenuation to the fundamental running frequency and give a rise time of 35 ms.

Values (CGS Units)

Torque constant	$Kt = 1$
Back EMF constant	$Kv = 8e^{-3}$
Phase Det. gain	$Kd = 0.35$
Load Inertia	$J_l = 7.5^{e-4}$
Armature resistance	$Ra = 4$
Armature Inductance	$La = 4e^{-3}$
Sense Amp feedback	$Rf = 10k$
Sense resistor	$Rs = 0.2$
Attenuation 1st stage	$K_1 = 0.2$
Sense Amp. gain	$Gi = 5$
Transconductance Gain	$A = 2e^4$
Number Of Pulses/Rev.	$Np = 36$
Transconductance input	$Rspin = 2e^4$
Lead/lag Ratio	$N = 14$

Therefore $\omega_u/\omega_l = 14$;

Making $\omega_x = 62.8$. Using ratios suggested above:

$Kn = KdNpK_1(1 - \beta)\omega_p \times \omega_q \times N/\omega_z$

Figures 12 (a) and 12 (b);

$G_1 = 1.33e^3$; $G_2 = 250$; $G_1G_2 = 3.3325e^5$; $H = 5e^{-4}$; $\beta = 0.66$;

$\omega_a = 1e^3$; $\omega_p = 628$; $\omega_q = 942$; $\omega_z = 6.28$; $\omega_l = 16.$; $\omega_u = 235$

$Kn = 1.185e^6$; Sub. Values in (3):

$$\frac{1185e^6(s + 16.784)(s + 6.28) \times \omega_x}{s^2(s + 942)(s + 628)(s + 235)}$$

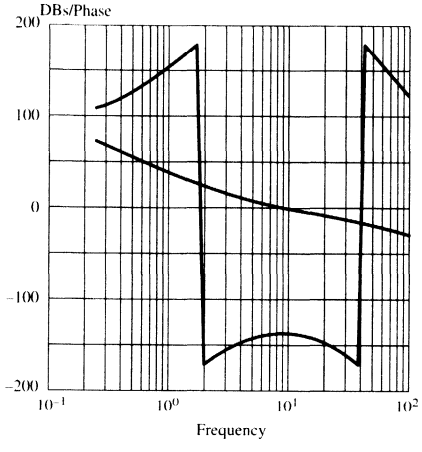
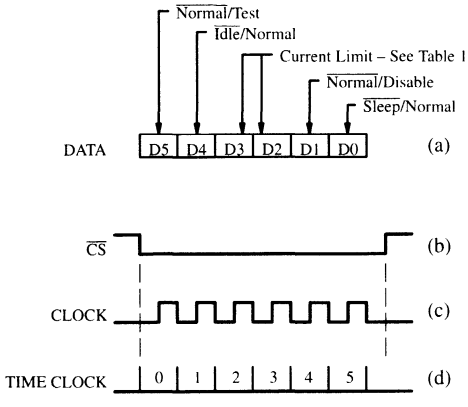


Chart 2. Spindle servo open loop plot.



(e)

Table 1.

D3	D2	Current
0	0	1 A
0	1	0.6 A
1	0	0.8 A
1	1	0.4 A

Rules
1. D5 is first bit Clock (0)
2. $\overline{CS}$ goes low when Clock is low
3. $\overline{CS}$ goes high, latches data in

Figure 13. Serial register timing diagram

Summary

An approach has been presented for the analysis, and subsequent design, of servos for the head actuator arm and spindle motor control, using a Siliconix combination VCM and spindle motor driver IC, the Si9990CS.

Some guidelines, together with explanations, have also been included for design and choice of auxiliary functions, i.e. snubbing, and the components required for acquisition and proper commutation of the spindle motor.

Open loop plots have been included (see chart 1 and chart 2). These indicate a confirmation of performance using the suggested design rules.

12-V VCM/Spindle Motor Driver for Large Capacity HDD

Features

- 12-V Motor Supply
- Blocking Schottky Diode Replaced by External Synchronous Rectifier
- Spindle Motor Driver Features:
  - External LITTLE FOOT® Drivers for High Current/Power Application
  - Constant Off-Time PWM Current Drive Minimizing Power Dissipation
  - Sensorless Motor Commutation Immune to PWM Noise
  - Externally Controlled Start-Up/Run Function
  - Low-Jitter Commutation Output for External Speed Control
  - Level Shifting Buffer Amplifier for PWM DAC
  - Adjustable Output Slew Rate Control
  - Unique Commutation Driver Minimizing Audible Noise
  - Programmable Phase Advance for High Speed Motor
  - Speed Triggered Motor Brake for Enhanced Reliability
- Voice Coil Motor Driver Features:
  - External LITTLE FOOT Drivers for High Current/Power Application
  - Low Crossover Distortion in Linear Mode (Class AB)
  - Selectable Constant Frequency PWM or Linear Operation
  - Programmable Retract Voltage Clamp
  - Level Shifting Buffer Amplifier for PWM DAC
  - Direct VCM Retract Control Input
  - Current Sense Output for Enhanced Servo Control
  - Fixed PWM Output Slew Rate Limit
- System Manager Features:
  - Power-On Reset Generator
  - Adjustable System Voltage Monitor
  - 2.3/5.0-V ± 5%, 150 ppm/°C Reference Output for External PWM DAC
  - ProgrammableTimer for Head Retract and Spindle Brake Delay
  - Built-In Test Ability
- 3-Wire Synchronous Serial Data Interface
- Internal Registers and Address Decoding with Full Readback Capability

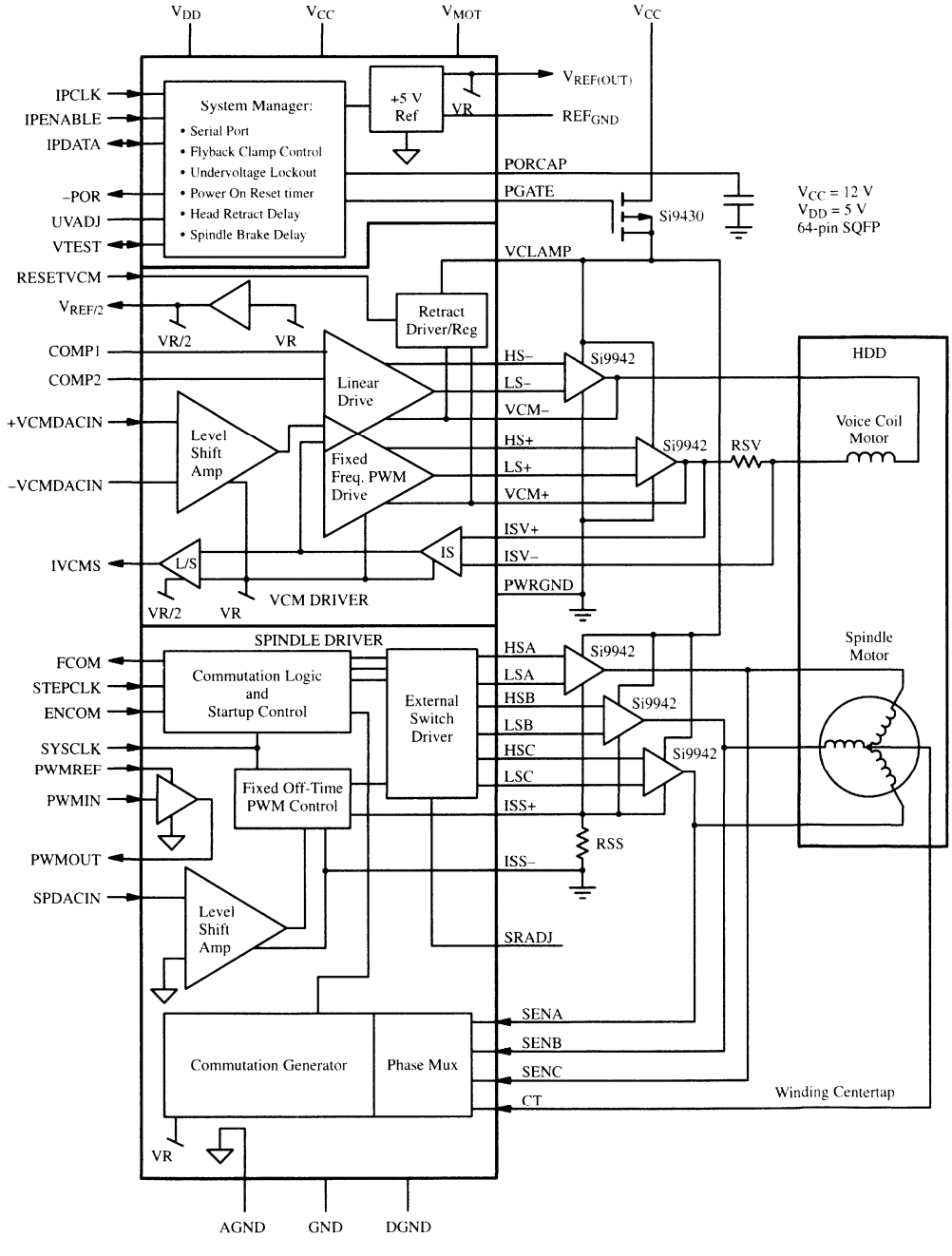
Description

The Si9993CS consists of a 3-phase brushless dc motor (spindle) PWM controller and a linear/PWM transconductance stage suitable for driving a voice coil motor (head actuator). To meet the power handling capability required for a high capacity hard disk drive, both drivers utilize external LITTLE FOOT half-bridges (Siliconix Si9942 recommended). A separate LITTLE FOOT PMOS switch (Si9430) is used as a synchronous rectifier in place of the usual Schottky blocking diode.

Si9993CS is manufactured in a junction-isolated BiC/DMOS process (JIBCD15) and is available in a 64-pin SQFP package, specified to operate over the commercial (0°C to 70°C) temperature range.

This product is currently in development. Inquiries regarding the status of this product should be directed to Siliconix Marketing.

Functional Block Diagram



Pre-Release Information

Absolute Maximum Ratings (T_A = 25°C)*

Voltage Referenced to GND Pin
V_{DD} Supply Range ..... –0.3 to 7 V
V_{CLAMP} Supply Range ..... > (V_{CC} – 0.3 V) and > (V_{DD} –0.3 V) to 14 V
V_{CC}, V_{MOT} Supply Range ..... –0.3 to 14 V
AGND, DGND, PWRGND to GND ..... –0.3 to 0.3 V
SENA, SENB, SENC, CT, VCM+, VCM-Pin ..... –1.0 to V_{CC} + 1.0 V
$\overline{POR}$, FCOM, STEPCLK, ENCOM, SYSCLK, PWMIN, PWMOUT, RESETVCM, IPCLK, IPDATA and IPENABLE pins ..... –0.3 to V_{DD} + 0.3 V
All Other Pins ..... –0.3 to V_{CC} + 0.3 V
Maximum Current (All Input Pins) ..... ± 20 mA
Storage Temperature (T_{stg}) ..... –65 to 150°C
Operating Temperature (T_A) ..... 0 to 70°C
Junction Temperature (T_J) ..... 150°C
Power Dissipation ..... 2 W
Thermal Impedance (Θ_{JA}) ..... 6.25°C/W

* *Exposure to Absolute Maximum rating conditions for extended periods may affect device reliability. Stresses above Absolute Maximum rating may cause permanent damage. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum rating should be applied at any one time. Device mounted on one-inch square FR4 Board.*

Specifications

Operating Conditions: $V_{CC} = V_{MOT} = 12$ V ±10%, $V_{DD} = 5$ V ±10%, $V_{REF(IN)} = V_{REF(OUT)}$ RSS= RSV = 0.2 Ω ±1%, R_{SRADJ} = 20 kΩ ±1%, Si9942/Si9430 LITTLE FOOT Driver, F_{SYSCLK} = 5 MHz, T_A = 0 to 70°C

Parameter	Symbol	Specific Test Conditions		Limits Min[a]	Limits Typ[b]	Limits Max[a]	Unit
Power Supply							
Supply Current	I_{DD}	Normal Operation, Serial Port Idle			0.2	1.2	mA
		D7D6(REG0/5) = 00, All Clocks Disabled			0.02	0.1	
	$I_{CC} + I_{MOT} + I_{CLAMP}$	Normal Operation No Load at $V_{REF(OUT)}$	With VCM Load		40	65	
			Without VCM Load		25	40	
		D7D6(REG0/5) = 00, All Clocks Disabled			4	6	
Control Logic							
Low Input Current	I_{IL}	V_{IN} = 0 V		–1			µA
High Input Current	I_{IH}	$V_{IN} = V_{DD}$				1	
Low Input Voltage (All Digital Inputs)	V_{IL}					0.8	V
High Input Voltage (All Digital Inputs)	V_{IH}			2.0			
Low Output Voltage ($\overline{POR}$)	V_{OL}	I_{OUT} = 4 mA				0.4	
High Output Voltage ($\overline{POR}$)	V_{OH}	I_{OUT} = –4 mA		4.1			
Low Output Voltage (FCOM, PWMOUT)	V_{OL}	I_{OUT} = 2 mA				0.4	
High Output Voltage (FCOM, PWMOUT)	V_{OH}	I_{OUT} = –2 mA		4.1			
IPDATA Setup Time to Rising IPCLK Edge	t_1	See Timing Diagram, Figures 1 and 2		15			ns
Rising IPCLK Edge to IPDATA Hold Time	t_2			15			
IPDATA Clock Cycle Time	t_3			100			
IPDATA Hold for IPDATA Driver Turnaround	t_4			70			

Pre-Release Information

Specifications

Parameter	Symbol	Specific Test Conditions		Limits Min[a]	Limits Typ[b]	Limits Max[a]	Unit
Control Logic (Cont'd)							
IPCLK High and Low Time	t_5	See Timing Diagram, Figures 1 and 2		45			ns
IPDATA Propagation Delay WRT IPCLK Falling Edge	t_6	See Timing Diagram, Figures 1 and 2				100	ns
IPENABLE Setup Time WRT IPCLK Rising Edge	t_7			100			
IPENABLE Hold Time WRT IPCLK Rising Edge	t_8			20			
WRT IPCLK Falling Edge to Data Tri-State	t_9				10		
System Manager							
V_{DD} Undervoltage Detection Threshold (High-to-Low)		UV_{ADJ} Unconnected		4.500	4.625	4.750	V
V_{DD} Hysteresis					0.05		
V_{CC} Undervoltage Detection Threshold (High-to-Low)				8.5	9.25	10.0	
V_{CC} Hysteresis					0.2		
POR Timeout	$t_{POR}{}^{\uparrow}$	PORCAP = 0.5 µF		350	500	650	ms
Delay Time from PWR Failure to $\overline{POR}$ Active	$t_{POR}{}^{\downarrow}$				0.8	1.0	µS
POR Charging Current	I_{POR}				2		µA
POR Comparator Hysteresis				1.0			V
Adjustable Internal Spindle Brake Delay Time	$t_{spindly}$	V_{CLAMP} = 3.0 to 13.2 V, $V_{DD} = V_{CC}$ = 0 V	D3D2(REG1) = 01		192		ms
Internal VCM Retract Delay Time	t_{vcmdly}		D5D4(REG1) = 01		8		
V_{TEST} Leakage	I_{VTEST}	V_{CLAMP} = 3.0 V, $V_{DD} = V_{CC}$ = 0 V, V_{TEST} = 10 V				1	µA
5-V Reference Initial Power-On Tolerance	V_{REF}	$V_{REF(IN)} = V_{REF(OUT)}$ (Internal Reference), I_{OUT} = 20 mA to –2 mA		4.75	5.00	5.25	V
5-V Reference Drift from Initial Power-On Tolerance	$\frac{\Delta V_{REF}}{V_{REF}}$			–1.5		1.5	%
VCM Driver							
Transconductance	G_{mVCM}	I_{MOTOR} = 1 A, D5D4(REG0) = 11		1.52	1.60	1.68	A/V
Output Offset Current	I_{OS}	D5D4(REG0) = 11		–25	0	25	mA
DAC Reference Output	$V_{REF/2}$	R_{LOAD} = 100 kΩ		2.09	2.2	2.31	V
VCMDACIN Input Range		+VCMDACIN or –VCMDACIN to GND		0.1		5.0	
VCMDACIN Input Bias Current	I_b(L/S)					50	nA
Feedback Resistance	R_{FB}	Internal Resistor from IVCMS to COMP1			12		kΩ
3-dB Bandwidth		L/S, I/S and Comp Amp			1.0		MHz
		Class B Power Amp			0.4		
CMRR of Current Sense Amplifier		CM Input = 0 to V_{CC}			70		dB
Head Retract Voltage Clamp		I_{MOTOR} = 60 mA, D7D6 (REG1) = 00		0.32	0.4	0.48	V
Short Circuit Head Retract Current				120		180	mA

Specifications

Parameter	Symbol	Specific Test Conditions	Limits Min[a]	Limits Typ[b]	Limits Max[a]	Unit
VCM Driver (Cont'd)						
Current Sense Amplifier Zero Output Voltage	V(IVCMS)	I_{MOTOR} = 0 D7D6 (REG0) = 00, D7D6 (REG5) = 11 I_{MOTOR} = 0 D7D6 (REG0) = 00, D7D6 (REG5) = 11	2.32	2.5	2.68	V
Current Sense Amplifier Output Gain Ratio	V(IVCMS)/ V(RSV)	dc Gain		2.67		V/V
Spindle Motor Driver						
Transconductance	G_{MSPIN} (Start-Up)	I_{MOTOR} = 1 A, D5D4 (REG5) = 11	1.44	1.60	1.76	A/V
Spindle Driver Input Offset Voltage	$V_{(SPDACIN)}$	I_{MOTOR} = 0 A, D5D4(REG5) = 11		40		mV
Current Sense Comparator Input Bias Current	I_B(C/S)				2	µA
PWM Constant Off-Time Stability		D3/D2 (REG5) = 01	3.2		3.4	µs
Spindle Driver Input Bias Current	I_B(L/S)				50	nA
BEMF Detect Input Offset Voltage			–20		20	mV
BEMF Detect CM Input Range			2.5		V_{CLAMP} – 2	V
Power-Down Spindle Motor Brake Threshold		Measured at V_{CLAMP}, D1D0(REG1) = 11	2.4	3.0	3.6	V
PWM Pre-Driver for LITTLE FOOT® (Spindle Motor)						
SRADJ Voltage	V_{SRADJ}	I_{SRADJ} = –50 µA		1.0		V
HSA/B/C Output High Current (OFF)	I_{OH}(HS)	**D2/D1 REG4 = 11**				mA
		$V_{OUT} = V_{CLAMP} - 0.4$ V		–1.6		
		$V_{OUT} = V_{CLAMP} - 3$ V Slew Controlled Range		–1.6		
		$V_{OUT} = V_{CLAMP} - 10$ V		–24		
		D2/D1 REG4 = 00				
		$V_{OUT} = V_{CLAMP} - 3$ V		–13		
HSA/B/C Output Low Current (ON)	I_{OL}(HS)	**D2/D1 REG4 = 11**				
		$V_{OUT} = V_{CLAMP} - 3$ V Slew Controlled Range		1.4		
		D2/D1 REG4 = 00				
		V_{OUT} = 3 V		19		
LSA/B/C Output Low Current (OFF)	I_{OL}(LS)	**D2/D1 REG4 = 11**				
		V_{OUT} = 0.4 V		1.9		
		V_{OUT} = 3 V, Slew Controlled Range		1.7		
		V_{OUT} = 10 V		5.0		
		D2/D1 REG4 = 00				
		V_{OUT} = 3 V		13		

Specifications

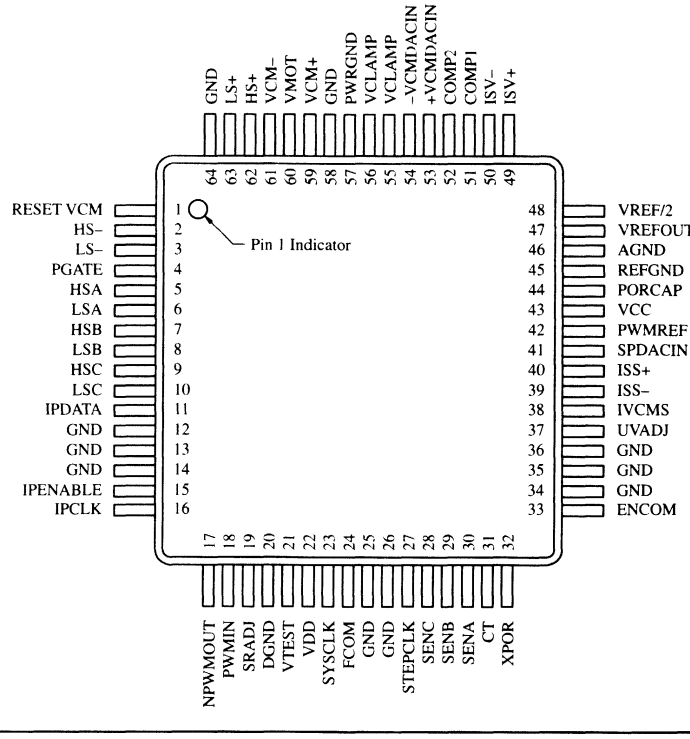
Parameter	Symbol	Specific Test Conditions	Limits Min[a]	Typ[b]	Max[a]	Unit
PWM Pre-Driver for LITTLE FOOT® (Spindle Motor) (Cont'd)						
LSA/B/C Output High Current (ON)	I_{OH}(LS)	**D2/D1 REG4 = 11**				mA
		V_{OUT} = 3 V, Slew Controlled Range		–1.1		
		D2/D1 REG4 = 00				
		$V_{OUT} = V_{CLAMP} - 3$ V		–7		
SENA/B/C and VCM+/– Clamp Diode Voltage	V_{CL}	Measured at I_F = 20 mA and I_F = –20 mA	0.5			V
PWM Pre-Driver for LITTLE FOOT (VCM)						
HS +/– Output High Current OFF	I_{OH} (HS)	**With Slew Rate Control**				mA
		$V_{OUT} = V_{CLAMP}$ –0.4 V		–1.6		
		$V_{OUT} = V_{CLAMP} - 3$ V Slew Controlled Range		–1.6		
		$V_{OUT} = V_{CLAMP}$ –10 V		–24		
		Without Slew Rate Control				
		$V_{OUT} = V_{CLAMP}$ –3 V		–1.4		
HS +/– Output Low Current ON	I_{OL} (HS)	**With Slew Rate Control**				
		$V_{OUT} = V_{CLAMP} - 3$ V Slew Controlled Range		1.4		
		Without Slew Rate Control				
		V_{OUT} = 3 V		3.1		
LS +/– Output Low Current OFF	I_{OL} (LS)	**With Slew Rate Control**				
		V_{OUT} = 0.4 V		1.9		
		V_{OUT} = 3 V, Slew Controlled Range		1.7		
		V_{OUT} = 10 V		5.0		
		Without Slew Rate Control				
		V_{OUT} = 3 V		3.1		
LS +/– Output Hifh Current ON	I_{OH} (LS)	**With Slew Rate Control**				
		V_{OUT} = 3 V, Slew Controlled Range		–1.1		
		Without Slew Rate Control				
		$V_{OUT} = V_{CLAMP}$ –3 V		–1.4		
Upper VCM Slew Rate Threshold	$VCMSR_{th+}$	From Low to High $V_{CC} = V_{CLAMP}$ = 12 V		10.3		V
		Hysteresis		2.3		
Lower VCM Slew Rate Threshold	$VCMSR_{th-}$	From High to Low $V_{CC} = V_{CLAMP}$ = 12 V		1.3		
		Hysteresis		1.7		
VCM Linear Pre-Driver for LITTLE FOOT						
HS +/– Linear High Output Voltage	V_{OH}	I_{OUT} = 0		V_{CLAMP} –0.8		V
HS +/– Linear Low Output Voltage	V_{OL}			1.4		
HS +/– Linear Output High Current	I_{OH}	$V_{OUT} = V_{CLAMP}$ –3 V		–1.4		mA
HS +/– Linear Output Low Current	I_{OL}	V_{OUT} = 3 V		3.1		

Specifications

Parameter	Symbol	Specific Test Conditions	Limits			Unit
			Min[a]	Typ[b]	Max[a]	
VCM Linear Pre-Driver for LITTLE FOOT (Cont'd)						
LS +/– Linear High Output Voltage	V_{OH}	$I_{OUT} = 0$		V_{CLAMP} –1.6		V
LS +/– Linear Low Output Voltage	V_{OL}			0.7		
LS +/– Linear Output High Current	I_{OH}	$V_{OUT} = V_{CLAMP}$ –3 V		–1.4		mA
LS +/– Linear Output Low Current	I_{OL}	V_{OUT} = 3 V		3.1		

Notes
a. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
b. Typical values are for DESIGN AID ONLY, not guaranteed or subject to production testing.

Pin Configuration



Pre-Release Information

Pin Description

Pin No.	Name	Type	Function
1	RESETVCM	Digital, Input	Direct RESET to bit D6 of REG0. Force head retract sequence if in normal operation.
2	HS–	Analog, Output	Connection to gate of negative VCM high-side driver
3	LS–	Analog, Output	Connection to gate of negative VCM low-side driver
4	PGATE	Analog, Output	Connection to gate of external PMOSFET used to isolate VCLAMP during emergency head retract.
5	HSA	Analog, Output	Connection to gate of spindle 0–A high-side driver
6	LSA	Analog, Output	Connection to gate of spindle 0–A low-side driver
7	HSB	Analog, Output	Connection to gate of spindle 0–B high-side driver
8	LSB	Analog, Output	Connection to gate of spindle 0–B low-side driver
9	HSC	Analog, Output	Connection to gate of spindle 0–C high-side driver
10	LSC	Analog, Output	Connection to gate of spindle 0–C low-side driver
11	IPDATA	Digital, I/O	Bi-directional data path for the serial port
12, 13, 14, 25, 26, 34, 35, 36, 58, 64	GND	Supply	Chip substrate ground
15	IPENABLE	Digital, Input	Strobe input for data word. System commands are executed at the falling edge of IPENABLE.
16	IPCLK	Digital, Input	Clock input for the serial port
17	PWMOUT	Digital, Output	Digital output of stand-alone PWM driver
18	PWMIN	Digital, Input	Digital input of stand-alone PWM driver
19	SRADJ	Analog, Input	Spindle Output drive slew rate control
20	DGND	Supply	Digital negative supply
21	VTEST	Analog, I/O	External charge storage node for spindle brake function. Also used as a manufacturer's test pin
22	VDD	Supply	+5 V digital power supply
23	SYSCLK	Digital, Input	System clock input (5Mhz) for onboard timers
24	FCOM	Digital, Output	Commutation clock output for external speed control
27	STEPCLK	Digital, Input	Clock input for spindle commutation state machine, used during spindle start–up only
28	SENC	Analog, Input	Input to BEMF–sense circuitry; connect to 0–C
29	SENB	Analog, Input	Input to BEMF–sense circuitry, connect to 0–B
30	SENA	Analog, Input	Input to BEMF–sense circuitry, connect to 0–A
31	CT	Analog, Output	Center Tap
32	POR	Digital, Output	Power-on-reset pulse for entire drive electronics
33	ENCOM	Digital, Input	Enable input for onboard commutation clock generator
37	UVADJ	Analog, Output	External Undervoltage threshold adjust
38	IVCMS	Analog, Output	VCM current sense output; signal referred to $V_{REF/2}$
39	ISS–	Analog, Input	Negative input to spindle current sense amplifier
40	ISS+	Analog, Input	Positive input to spindle current sense amplifier
41	SPDACIN	Analog, Input	Spindle Input (from PWM DAC Out)
42	PWMREF	Analog I/O	Reference supply input for stand-alone PWM driver
43	VCC	Supply	+12 V analog power supply for the whole chip
44	PORCAP	Analog, Output	Connect to Power–on–reset timing capacitor
45	REFGND	Supply	Critical analog ground reference
46	AGND	Supply	Analog negative supply and ground reference
47	VREF(OUT)	Analog, Output	Reference supply output for stad-alone PWM DAC and VCM common
48	VREF/2	Analog, Output	Reference supply output for external VCM DAC
49	ISV+	Analog, Input	Positive input to VCM current sense amplifier
50	ISV–	Analog, Input	Negative input to VCM current sense amplifier
51	COMP1	Analog, Output	Connection for external VCM R/C compensation
52	COMP2	Analog, Input	Connection for external VCM R/C compensation

Pin Description (Cont'd)

Pin No.	Name	Type	Function
53	+VCMDACIN	Analog, Input	Positive VCM input (from +VCM DAC Out)
54	–VCMDACIN	Analog, Input	Negative VCM input (from –VCM DAC Out)
55, 56	VCLAMP	Supply	+12-V digitl power supply for spindle PWM section; also, inductive flyback clamp and emergency head retract power supply
57	PWRGND	Supply	Ground return referred to external VCM n-channel FETs; used to power VCM class AB stage.
59	VCM+	Analog, I/O	Feedback from the positive output of VCM driver
60	VMOT	Supply	+12-V power supply referred to external VCM p-channel FETs; used to power VCM class AB stage.
61	VCM–	Analog, I/O	Feedback from the negative output of VCM driver
62	HS+	Analog, Output	Connection to gate of positive VCM high-side driver
63	LS+	Analog, Output	Connection to gate of positive VCM low-side driver

Timing Waveforms and Test Circuit

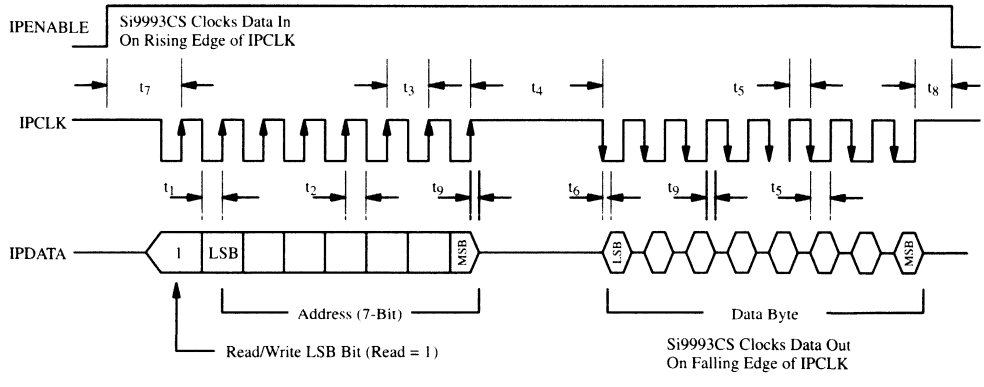


Figure 1. Read Cycle Timing Diagram

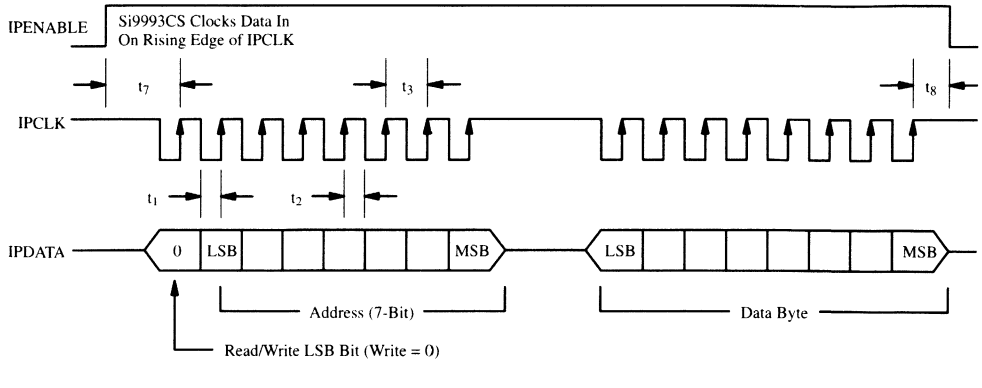


Figure 2. Write Cycle Timing Diagram

Functional Description

Voice Coil Motor Driver

The VCM driver provides all necessary control functions, for a linear transconductance stage, including a motor current sense amplifier, a loop compensation amplifier and a 3-A power amplifier featuring two Si9942's (external) in a full H-bridge configuration. The output half-bridge operates in the Class B mode during seeking. The track following mode is primarily a function of an onboard class AB bipolar driver. The output crossover distortion is kept to a minimum by the combined BiCMOS driver. Two external components (R3 and C3) are required to set the bandwidth of the full transconductance stage. For greater flexibility in interfacing to the external D/A converter, a DAC reference, an input level shifting amplifier and gain select are included. To minimize power dissipation of the power stage during the seek operation, the VCM driver may also be re-configured (via Bit D3/2 of REG0, see Table 2) into a constant frequency Pulse-Width-Modulated (PWM) driver. No additional external components are required for this useful option. The head retract circuitry can be activated by an undervoltage condition, an external command via serial port, or direct control via the RESETVCM pin. The retract voltage clamp is programmable from 0.4 to 1.2 V.

External VCM DAC Operation

The VCM driver of the Si9993CS is designed to interface to an external DAC with an output range from 0.1 V to 4.5 V and uses the internal 2.3 V as the mid-point reference (signal common). Therefore, a differential input of up to ± 2.2 V may be accepted. Depending on the type of DAC chosen, either $V_{REF/2}$ (+2.3 V) or V_{REF} (+5.0 V) can be used as the DAC reference. The inaccuracy of the mid-point reference may be eliminated through calibration by disabling the VCM driver [D7/D6 (REG0) = 00 or 01] and digitizing the VCM current sense output (IVCMS). The digitized value is to be stored in the ASIC or DSP as the VCM current zero scale correction factor. A differential level shift amplifier has been added between the internal 12-V current sense amplifier and the IVCMS pin such that an external ADC operating from a 5-V power supply may be used directly.

Spindle Motor Driver

The spindle driver powers a three-phase brushless dc motor in open drive configuration and utilizing a Hall sensor-less commutation technique. To minimize power stress on the three V30044 (external) half-bridges, the driver operates in full time, constant off-time or variable frequency, PWM current mode. A proprietary BEMF sensing technique, consisting of a filter and a programmable EMF zero crossing comparator and an intelligent commutation delay generator, is used to derive the proper commutation zero crossing in the presence of severe PWM noise. The start-up of the motor is initiated by the microprocessor through the STEPCLK and ENCOM pins. This arrangement allows the user to tailor a start-up algorithm for any given drive. As shown in Table 1, the microprocessor may strobe the STEPCLK pin to force a new motor state sequentially. Multiple clocking will allow any undesired state to be bypassed. At an empirically determined time, the internal commutation clock generation loop may be closed by forcing ENCOM high. For complete interfacing to the microprocessor's PWM DAC, a level shifting amplifier, accepting a wide input range (via D5/D4 or REG5), is also included on chip. To minimize acoustic or EMI noise, the slew rate of the output drivers (via HSA/B/C and LSA/B/C)may be programmed by an external resistor connected through the SRADJ pin. Additional software slew rate controls are available through D2/D1 of REG4.

The speed control signal from the external micro or DSP is fed to the output PWM modulator via an external DAC and the onboard buffer/level shifter. The interface is designed to work with either PWM or linear DAC. Should a PWM DAC be chosen, a stand-alone digital buffer is available to level shift the 5-V signal from the PWM timer (referred to V_{DD}) to a supply independent signal (referred to V_{REF}), before it is fed to the external RC lowpass filter.

Adaptive Commutation Delay Operation*

Inside the spindle controller of Si9993CS, the desired 30 electrical degrees (or 90 degrees for a single phase) of commutation delay is generated by sensing the motor back-emf zero crossing at the unenergized winding with a current-controlled transconductance amplifier and charging an internal capacitor to be programmable threshold with the output current of the amplifier. The delay time generated is proportional to the speed of the motor because the charging current is derived from a motor frequency to current converter. This proprietary analog timing generator, combined with the external low-pass filter (three 200-kΩ resistors), provide excellent immunity to the highly unstable

Table 1: Spindle Commutation Sequence

Sequencer State	HSA	LSA	HSB	LSB	HSC	LSC
Reset*	High	Low	High	Low	High	Low
1	Low	Low	High	High	High	Low
2	Low	Low	High	Low	High	High
3	High	Low	Low	Low	High	High
4	High	High	Low	Low	High	Low
5	High	High	High	Low	Low	Low
6	High	Low	High	High	Low	Low

*Reset is the state after exiting spindle disable or brake mode.

PWM noise. The resulting motor once-around jitter time is comparable to that of a linear drive system. Furthermore, the highly integrated nature of the design has eliminated all external capacitors, representing a significant savings in cost and board space. For maximum flexibility, D2/D1 of REG5 may be used to program the frequency to current converter filter bandwidth. For very high performance drive, D7/D2 or REG3 programs the commutation delay threshold in both negative (phase advance up to 23.5°) and positive (phase delay up to 7.5°) directions.

Quiet Commutation Operation*

Included on the Si9993CS spindle driver is a unique feedback circuit which was developed to control the supply current during the current transfer from one phase of the winding to another. At the proper time of commutation, the ramping down of the previous phase is regulated to match with the ramping up of the next phase, which is fully on initially, until all current has been transferred to the next phase. This not only reduced the constraint on power supply requirements but also eliminated annoying high frequency audible noises generated from second and third harmonics of the commutation frequency. The "quiet commutation" operation is a function of PWM off-time and slew rate control. D7/D4 of REG4 may be used to optimize the circuit performance accordingly.

System Manager

The system manager includes power supply monitor, power-on reset timer, individual motor on/off control, system reference generator and a variety of digital delay timers targeted for PWM and head retract functions. An external 5-MHz system clock is used mainly for the spindle motor PWM timing functions. An onboard RC oscillator is used to generate the timing necessary for the emergency motor shutdown sequence. When a tight microporcessor power supply is sepeified, a pair of external resistors may be used to adjust the V_{DD} undervoltage lockout value via UVADJ pin. Finally, an external capacitor is used to set up the 500-ms power-on reset pulse for the entire drive electronics. All controls from the microprocessor or DSP are communicated via a 16-bit serial port.

Serial Port

A 16-bit word, clocked into the serial interface port of the Si9993CS, provides the means to program basic operating conditions, control the motor configuration and to force testing conditions suitable under the production environment. The serial port is controlled by three signals IPDATA, IPCLK, and IPENABLE. The IPDATA signal is the bidirectional data line, the IPCLK signal is used as the clock to validate the data and IPENABLE enables serial port operation. This serial port can be used with the Intel 80C196, AMD 186 processors or other synchronous serial interfaces.

The serial port allows transfer of a R/W mode bit, seven bits of register address, and eight bits of data. The port is inactive when the IPENABLE line is low, and IPCLK must be high. When IPENABLE is high, the port is active and IPDATA is strobed on the rising edge of IPCLK. The first bit transferred on the IPDATA line to the Si9993CS is the R/W mode bit. As shown in Figure 1, a R/W mode bit of '1' indicates that the data shall be read from the Si9993CS. Otherwise, the data shall be written to the Si9993CS as shown in Figure 2. The next seven bits are the register address. After the transfer of the address, IPCLK must not switch for a minimum of 70 ns to allow the IPDATA line to turn around in case of a read operation. After this pause, one byte of data is transferred to or from the Si9993CS based on the R/W mode bit. Both

*Patent Applications Pending

the address and the data are transferred with the LSB first and the MSB last. IPENABLE must be lowered to deactivate the port before the next byte can be transferred. Note that Si9993CS's six command registers are NOT decoded by unique binary address. Each register is identified by a specific address bit. (i.e. an address of 111111 will access all six registers). The address and function of each command register and the definition of each bit within the register are shown in Table 2. **Note that unused, or open, bits are handled differently. For write operation, the unused bits may be either 0 or 1. For read operation, the first bit to appear at the serial port is the least significant used bit of the register being read. Data appearing after the last valid bit should be ignored. As an example, the data readout sequence for REG1 in time is D2—D3—D4—D5—D6—D7—X—X. Slew Rate Control bits – TBD.**

Emergency Motor Shutdown Sequence

The Si9993CS executes a motor shutdown sequence whenever a valid low supply condition is detected (i.e. POR going from High to Low). The circuitry which controls events within this emergency sequence is powered by spindle motor's kinetic energy (BEMF) via the VCLAMP pin. The critical timing for various events is to be provided by an onboard RC oscillator and digital counters. The timer's value must be programmed by the external microprocessor after the IC is first powered up. Note that a similar "normal" (nominal supply) motor shutdown may be invoked by setting D7/D6 of REG5 (Spindle Command) to "00" state. Individual motor shutdown operation is also possible through the serial port. Refer to Table 2 for a complete description.

Immediately after detection of the undervoltage condition, all spindle drivers are turned off while the VCM's low-side drivers are turned on to stop the head from any previous movement. Additionally, all command resistors, except REG1, are reset. After a time delay, programmed by D5/D4 of REG1, the VCM's retract circuitry is turned on. The spindle drivers remained off. The head is retracted toward the inside diameter of the disk, or (VCM+ – VCM–) is positive. The voltage clamp across the VCM, or the maximum head velocity, is limited by the stored value in D7/D6 of REG1. No programmable current clamp is available on Si9993CS. The minimum short-circuited VCM retract current is 120 mA. Refer to Figure 3 for a simplified schematic.

The head retract time interval, or spindle brake delay time, is programmed via bit D3/D2 of REG1. After the time-out, the VCM drivers are turned off (tri-state) and all bits of REG1 except D1/D0 are reset. The state of the spindle motor low-side drivers are determined by D1/D0) of REG1. Depending on the motor and the number of disk platters, a spindle brake at high speed (BEMF voltage of 6 V or higher) may result in a high amount of energy dissipation in the LITTLE FOOT drivers. One solution to this problem is to use a ultra-low $r_{DS(on)}$ LITTLE FOOT device, such as Sixxxx, should the dissipation limit of the Si9942 be exceeded. In which case, D1/D0 or REG1 should be programmed for immediate brake. A lower cost solution, when feasible, is to allow the motor to spin down to a lower rpm before the low-side drivers are turned on to brake the motor. In such case, the motor speed threshold, which is sensed by measuring the motor BEMF via V_{CLAMP} voltage, is programmed using D1/D0 of REG1. (Figure 4 shows a 3-V threshold being selected.) Also, as shown in Figure 4, once the spindle brake is on, an external pre-charged capacitor connected to the V_{TEST} pin will be switched on to maintain the gate drive to the LITTLE FOOT drivers, even if V_{CLAMP} drops down to zero.

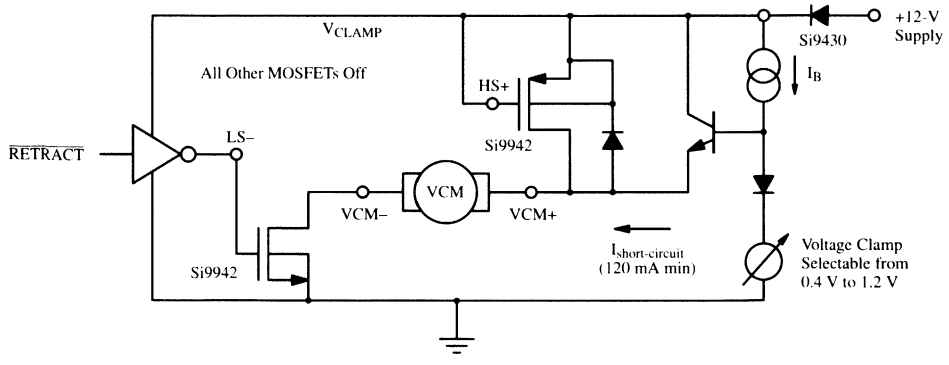


Figure 3. Simplified Retract Circuit

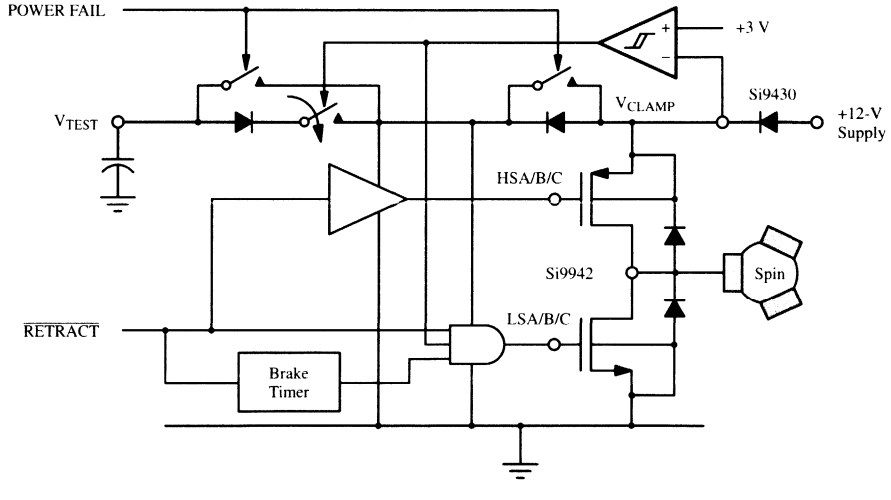


Figure 4. Simplified Spindle Brake Circuit

Power-Up Sequence

The POR timer receives the two supply undervoltage detection outputs and combines them to form one output called PowerFailure. If PowerFailure is low, the POR output will remain low. After the power supplies are deemed safe, PowerFailure goes high and the timer is turned on which holds the POR output low for an additional 500 ms. If PowerFailure goes back low while the timer is active, the POR output must remain low and the timer must reset and wait for PowerFailure to go back high before starting again.

The POR output must drop low within 1 µs from when a power failure is detected. Once the POR output drops low, the timer must also reset. If the PowerFailure output drops low for less than 600 ns, then the power failure is ignored and the POR output remains high and the timer is not reset. The POR output cannot glitch at anytime. If a power failure is detected, then the POR output must stay low for a minimum of 350 ms. A minimum of 1 V of hysteresis exists at the POR comparator which monitors the timer ramp voltage.

Recommended Parameter Setting Hardware Values and Register Contents

Spindle:

In order to perform some applications testing, some of the registers should be preloaded and certain hardware values installed. These are for a first approximation on an average spindle motor and should be adjusted for the particular motor and parameters that will be used.

All registers will default to 0 at power-up. The following register value exceptions should be loaded for an average motor load.

For start-up:
REG3 D7→D0 = 00000011; 8° Phase Advance, 13-µS PWM Off-Time
REG4 D7→D0 = 00000000; 1.4-µS On-Time Blanking, 7/8 Off-Time, Slew Rate Off, Q-COM Off
REG5 D2→D0 = 000; 400-ns F/I Sample Time, F/I Speed-Up On

After reaching speed:
REG3 D7→D0 = 00000001; 8° Phase Advance, 3.4-µS PWM Off-Time
REG4 D7→D0 = 00000111; 1.4-µS On-Time Blanking, 7/8 Off-Time, Slew Rate On, Q-COM On
REG5 D2→D0 = 110; 40-ns F/I Sample Time, F/I Speed-Up On

Hardware values:
Resistor from SRADJ to Ground = 20 kΩ for approximately 1-µS Slew Rate
Capacitor from $V_{REF(in)}$ to Ground = 1 µF

VCM:

The Si9993CS contains a transconductance amplifier to drive the voice coil motor (VCM). For proper operation, this amplifier must be compensated specifically for the VCM being driven. As a first approximation, the torque constant and inertia of the VCM may be ignored although they will have some influence on the final results, especially if large.

The VCM transfer function of this simplified case may be expressed in the s (Laplace) plane as:

$$g_v = \frac{\frac{1}{L_v}}{s + \frac{R_v}{L_v}} \quad (1)$$

Where

R_v = VCM resistance in ohms
L_v = VCM inductance in henrys
s is the Laplace operator

This has a pole at $-R_v/L_v$. It is desirable to cancel this pole in the interest of stability. In order to do this, a compensation amplifier is cascaded with the VCM and its driver. The transfer function of this amplifier is:

$$H_c = A \times \frac{\left(s + \frac{1}{R_L \times C_L}\right)}{s} \quad (2)$$

Where

R_L = compensation amplifier feedback resistor in ohms
C_L = compensation amplifier feedback capacitor in farads
A = compensation amplifier and driver voltage gain at high frequency

If $R_L \times C_L$ is set equal to L_v/R_v, then the combined open loop transconductance in siemens becomes:

$$g_{to} = \frac{A}{s \times L_v} \quad (3)$$

Use these values as the series combination from COMP1 to COMP2. The absolute values should be adjusted for the desired open loop gain and closed loop bandwidth desired.

This has a single pole at the origin and is therefore stable when the loop is closed.

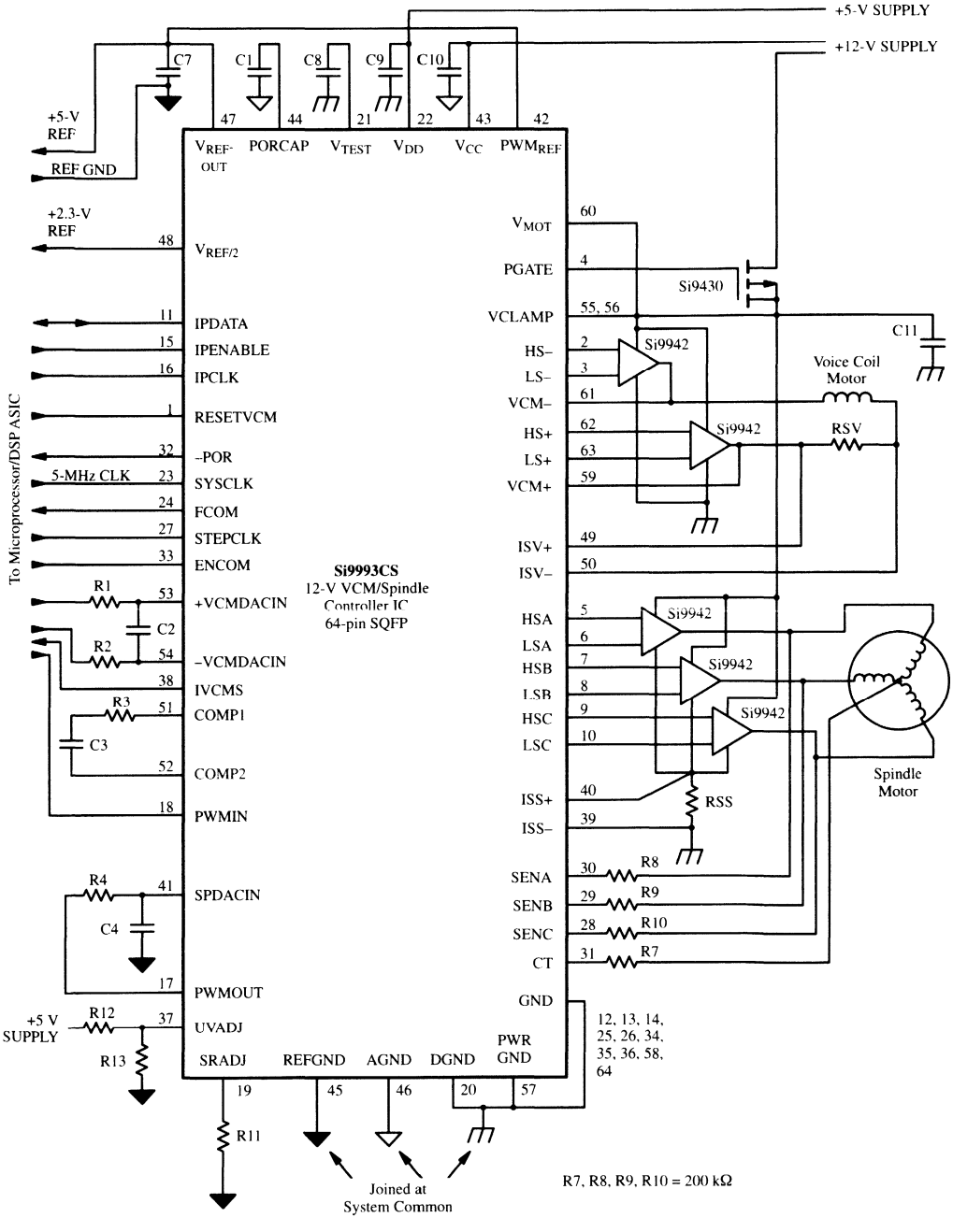
Table 2: Serial Port Definitions (Register Address = $A_6A_5A_4A_3A_2A_1A_0$)

Register	Bit No.	Name	Function
REG0 (xxxxxx1) VCM Command	D7/D6	VCM Control	VCM Enable/Disable Control: "00" = All VCM amplifiers unbiased except those of current sense. VCM output drivers in tri-state. "01" = All VCM amplifiers unbiased except those of current sense. VCM brake always on. "10" = All VCM amplifiers unbiased except those of current sense. Motor shutdown sequence commences with head brake for a period of Tvcmdly, followed by head retract for a period of Tspindly. The VCM returns to tri-state thereafter. Note that this command has no effect on the spindle motor operation, or the content of REG5. "11" = VCM fully enabled for normal operation
	D5/D4	Gmsel(vcm)	VCM Transconductance Select (A/V): "11" = 1.60 "10" = 0.80 "01" = 0.40 "00" = 0.10
	D3/D2	$VPWM_{sel}$	VCM Output State Linear/Constant Frequency PWM Select: "00" = Output operates as a class AB, linear amplifier "01" = Output operated in PWM voltage mode at 31.25 kHz "10" = Output operated in PWM voltage mode at 62.5 kHz "11" = Output operated in PWM voltage mode at 125 kHz
	D1/D0	OPEN	OPEN
REG1 (xxxxx1x) Powerdown	D7/D6	$V_{retract}$	Head Retract Voltage Limit: "11" = 0.4 V "10" = 0.7 V "01" = 1.0 V "00" = 1.2 V
	D5/D4	T_{vcmdly}	VCM Head Retract Delay Time (from power-down detection or command): "11" = Zero Delay "10" = 4 ms "01" = 8 ms "00" = 16 ms
	D3/D2	$T_{spindly}$	Spindle Brake Delay Time (from power-down detection or command, t_{vcmdly} included): "11" = Zero Delay "10" = 144 ms "01" = 192 ms "00" = 384 ms
	D1/D0	V_{SPBRK}	Spindle Brake Threshold Voltage Select (V_{CLAMP} Detect): "11" = 3 V "10" = 4 V "01" = 5 V "00" = Immediate Brake
REG2 (xxxx1xx) Production Test Only	D7 Thru D0		FCOM Pin Configuration Option: "00000000" = FCOM (default) "10000000" = FCOM / 6 **All other combinations are for testing only, no user programmable parameter is available.**
REG3 (xxx1xxx) Spindle Controls	D7 Thru D2	V_{th1}	Spindle Commutation Delay Adjust in Sign-Magnitude: The value programmed controls the motor commutation delay, in electrical degree, from the last BEMF zero crossing via a 6-bit DAC. Each LSB corresponds to $^1/_2$ electrical degree. "011111" = 7.5° Delay : = : "010000" = 0° Neutral : = : "000001" = 7.5° Advance "000000" = 8° Advance, "100000" = 8° Advance "100001" = 8.5° Advance : = : "110000" = 16° Advance : = : "111111" = 23.5° Advance
	D1/D0	Tspinpwm	Spindle Constant Off-Time (f_{SYSCLK} = 5 MHz): "11" = 13 µs "10" = 6.6 µs "01" = 3.4 µs "00" = 1.8 µs

Table 2: Serial Port Definitions (Register Address = $A_6A_5A_4A_3A_2A_1A_0$)

Register	Bit No.	Name	Function
REG4 (xx1xxxx) Driver Controls	D7/D6	Tblank(on)	PWM On-Time Blanking Pulse Adjust (F_{SYSCLK} = 5 MHz): "00" = 1.4 µs "01" = 1.8 µs "10" = 0.6 µs "11" = 1.0 µs
	D5/D4	Tblank(off)	PWM Off-Time Blanking Pulse Ratio: "00" = 7/8 (80 to 88%) of Selected PWM Off-Time "01" = 3/4 (70 to 76%) of Selected PWM Off-Time "10" = 1/2 (48 to 52%) of Selected PWM Off-Time "11" = 3/8 (36 to 42%) of Selected PWM Off-Time
	D3	VCMsr	VCM Output Slew Rate Control Option: "0" = No slew rate limit at outputs —> T(p-ch) = T(n-ch) ≤ 0.1 µs "1" = Slew rate limit enabled —> T(p-ch) = T(n-ch) ≅ 1 µs
	D2/D1	SPINsr	Spindle Output Slew Rate Control Select: "00" = No slew rate limit at outputs —> T(p-ch) = T(n-ch) ≤ 0.1 µs "01" = Slew rate limit enabled —> T(p-ch) = 0.5 x T(SRADJ) T(n-ch) = T(SRADJ) "10" = Slew rate limit enabled —> T(p-ch) = T(SRADJ) T(n-ch) = 0.5 x T(SRADJ) "11" = Slew rate limit enabled —> T(p-ch) = T(SRADJ) T(n-ch) = T(SRADJ) Note: T(SRADJ) = Rise or fall time set by resistor at SRADJ pin
	D0	QCOM	Quiet Commutation (low torque ripple) Option
REG5 (x1xxxxx) Spindle Command	D7/D6	Spindle Control	Spindle Motor Enable/Disable Control "00" = Spindle amplifiers unbiased and state machines reset.. Spindle output drivers in tri-state. "01" = Spindle amplifiers unbiased and state machines reset. Spindle motor brake always on. "10" = All amplifiers unbiased and state machines reset. Motor shutdown sequence commence with tri-state output for a period set by Tvcmdly and Tspindly, followed by a spindle brake. Note this command will force a head retract, but will not affect the content of REG0. "11" = Spindle drivers fully enabled for normal operation
	D5/D4	Gmsel (spin)	Spindle Transconductance Select (A/V): "11" = 1.60 "10" = 0.80 "01" = 0.40 "00" = 0.20
	D3	Direct PWM	STEPCLK Pin Function Select: "1" = Direct PWM Input (steady running state only) "0" = Start-up step clock
	D2/D1	$(F/I)_{tsample}$	Commutation F/I Sample Time: "00" = FCOM/12 400 ns "01" = FCOM/38 133 ns "10" = FCOM/102 50 ns "11" = FCOM/128 40 ns
	D0	$(F/I)_{spdup}$	F/I Speed-Up Circuit Select: "0" = On "1" = Off

Applications



Si9993 – Hard Disk Drive Combination Spindle and VCM Controller

Robert P. Harshberger Jr.
Senior Staff Applications Engineer

Siliconix' Si9993 is a combination spindle motor and VCM (voice coil motor) controller which combines, in a single package, all of the sensorless commutation, pulse-width modulation (PWM), braking, and FET drive circuitry for a hard disk drive spindle motor. It also contains the linear and PWM FET drives, power-down retract, and transconductance compensation for a hard disk drive voice coil actuator.

The Si9993 incorporates many features, some of which are unique for a monolithic device, including:

- Robust, sensorless back-EMF spindle commutation scheme with low jitter
- "Quiet Commutation" for low acoustic noise
- Adjustable PWM slew rate control with enable on-the-fly for low EMI
- Programmable spindle phase advance for high rotational speed operation
- Spindle speed triggered motor brake for reduced driver stress during braking
- PWM *and* linear voice coil drive for accurate track follow, fast access, and low power dissipation
- Unique class AB linear VCM drive for distortion free transfer function, even near zero output
- Automatic actuator braking and power-down retract with programmable timing and velocity clamp
- Extensive programmability, allowing fewer PCB versions for different drive models and a lower external parts count

Other features include:

- Current-mode VCM and spindle operation
- Complimentary FET drive, with no high-side boost voltage required
- Compatibility with LITTLE FOOT® power MOSFETs
- PWM spindle operation
- FCOM once per commutation output for use by servo control
- FET switch for VCM retract isolation, providing low power dissipation
- Undervoltage power-on reset
- 64-pin SQFP package

Si9993 – Hard Disk Drive Combination Spindle and VCM Controller

The Si9993 is capable of PWM drive for both the spindle and VCM. PWM is the only method available for driving the spindle, but the VCM can be driven by either PWM or a linear drive. Compared with a linear drive, PWM reduces power dissipation in the output drive FETs.

There are significant disadvantages to using a linear drive. In linear drive, the driving device acts like a resistor. From Ohm's law we know that the power dissipated in the device is the current through the device times the voltage across it. A maximum occurs when one half the voltage is across the device and one half across the load. Here the power dissipation for the device or the load is VI/2 or $V^2/4R$ where V is the applied voltage, I is the current through the device and the load, and R is the load resistance. This can be quite a large number, especially with the newer high-speed disk drive motors where R is on the order of 1 Ω.

In PWM, the drive device is either on or off. When it is off, there is no current flow and hence no device dissipation. When the device is on, the device dissipation is $I^2r_{DS(on)}$ or $(V/R)^2r_{DS(on)}$, where V, I, and R are the same as in the linear case and $r_{DS(on)}$ is the on-resistance of the device. This is typically less than 0.1 Ω. Thus, maximum dissipation will be much less.

Figure 1 shows a typical PWM waveform. The period is the time for one complete modulation cycle. In the Si9993, the period for the VCM PWM is constant. For the spindle, the off-time shown in Figure 1 is constant. The average voltage over one period of the waveform in Figure 1 is approximately D(V+ – V–) where D is the duty cycle expressed as on-time/period.

Updates to this app note may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70654.

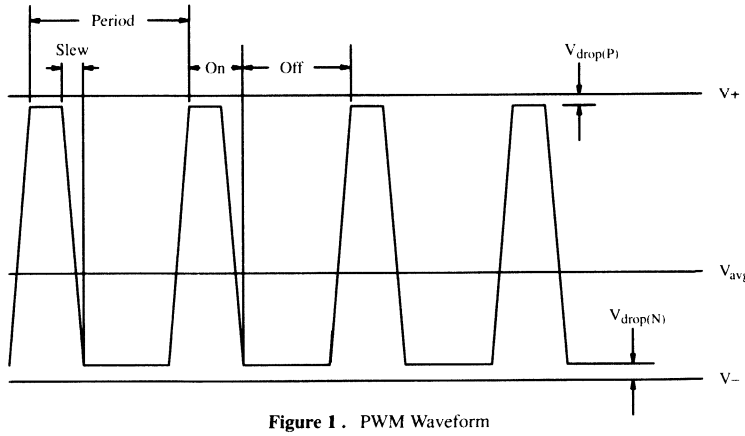


Figure 1. PWM Waveform

Losses are incurred in the V_{drop} areas but these are relatively small. The major power losses are due to the slew. This is the time spent switching from on to off and vice versa. This time is finite and the devices are effectively in the linear mode during this time. Often designers will deliberately increase the slew time, even though increased dissipation results, since shorter slew times generate spurious radiated and conducted frequencies that may interfere with low-level circuits in the system. The shorter the slew time, the wider the bandwidth and the greater the energy contained in these spurious frequencies.

Figure 2 shows a comparison of linear and PWM device dissipation observed during start-up on an actual spindle motor with a typical FET.

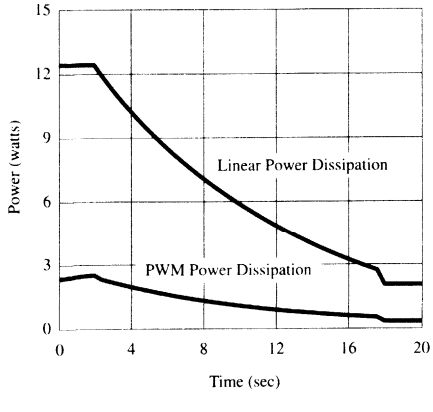


Figure 2. Linear vs. PWM Device Dissipation

The curves represent the dissipation that would occur for each device pair during operation, the upper curve representing linear operation and the lower curve representing PWM operation. These are for identical motor parameters and start-up curves.

During the first two seconds, the motor phase is being located. At this point, there is no motor velocity to speak of. After two seconds, the motor accelerates to its final velocity, which is reached after 17.5 seconds. Dissipation drops during this time because the motor's back-EMF is increasing, leaving less voltage to generate losses. At 17.5 seconds, the motor achieves final velocity. Current is reduced, since acceleration is not now required. Power dissipation thus falls to its steady-state value.

How Current Mode Reduces Power Supply Glitch Effects

Both the spindle and VCM drivers in the Si9993 operate in current mode. Thus for any particular input error voltage, a constant current is delivered to the load. This is accomplished through current feedback derived by a series sense resistor.

At first this may seem inappropriate for the spindle, as the goal is to achieve constant speed. Constant voltage results in constant speed, while constant current results in constant torque. It would seem that voltage-mode control would be preferred.

In the Si9993, the system speed control servo is responsible for the maintenance of constant speed. To minimize effects of power supply glitches on speed, a current mode is used.

Figure 3 shows the spindle speed disturbance that would result from a 0.5-s, 1-V dip in power supply voltage.

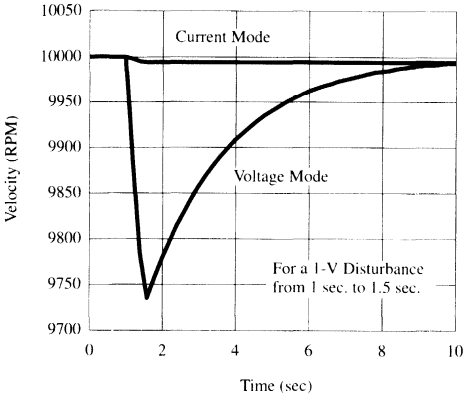


Figure 3 . Power Supply Disturbance

The nearly straight line is for the spindle operating in current mode. It shows a speed error of 0.06%. The curve showing a deeper disturbance represents voltage-mode operation, which has a speed error of 2.7%. These curves are for the same, typical 10,000-rpm spindle motor operating open loop with no system servo speed control.

In actual operation, the system servo must correct for this speed error. At a typical servo bandwidth of 2 to 3 Hz, the servo gain will be about 2.5 at the 1-Hz disturbance. In voltage mode, this would still result in a considerable error of 1.10% while with current mode the error will be corrected to just of 0.024%.

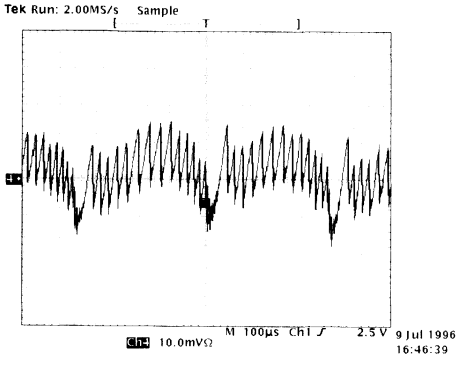
Note that the current sense for both the spindle and VCM use a differential input to monitor both ends of the sense resistor (Figure 12). This is an important feature, since the sense resistor is of low ohmic value, typically 0.2 Ω. Any additional impedance to ground (traces and vias) would result in a large error in the feedback ratio if included in the sensing. Also, these additional impedances are usually shared with other currents, resulting in interference and noise introduction in the feedback. Proper layout will route these sense traces directly to the terminals of the sense resistors. No vias or traces in the motor current path will be shared with the sense lines.

Patented Quiet Commutation Design Reduces Audible Noise

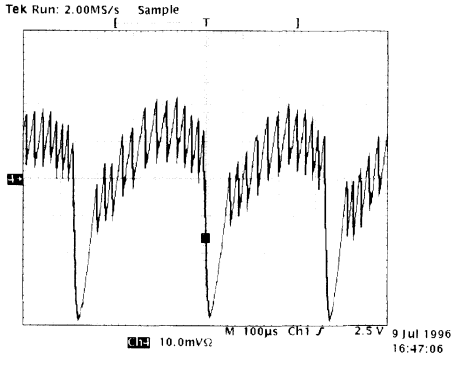
Disk drives need to operate quietly, particularly in an office environment. Commutation noise, because of its single tone nature (1.4 to 4 kHz plus harmonics, depending on the motor characteristics), can be especially annoying. The spindle motor generates this noise as torque ripple arises from phase-to-phase switching. It occurs at the commutation frequency and its harmonics.

The noise amplitude can be reduced by reducing the current ripple (current translates directly to torque by the equation, $\tau = K_t I$).

Figure 4 shows live oscilloscope pictures of the 12-V supply current with the quiet commutation option turned on (left) and off (right). Note the increased ripple amplitude in the right-hand picture. The current ripple in the Si9993 is controlled in a closed-loop manner, unlike some open-loop designs used in competitive devices. The closed-loop design results in more consistent noise reduction under varying motor characteristics.

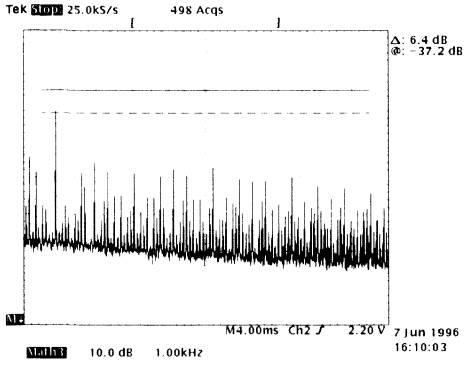


Quiet Commutation On

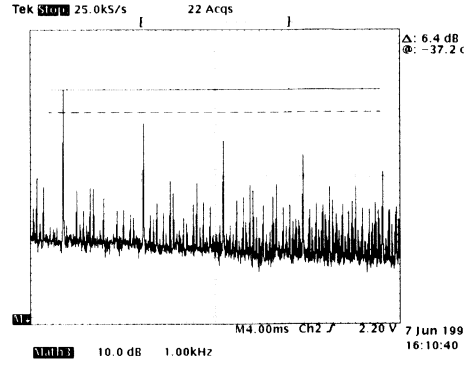


Quiet Commutation Off

Figure 4 .

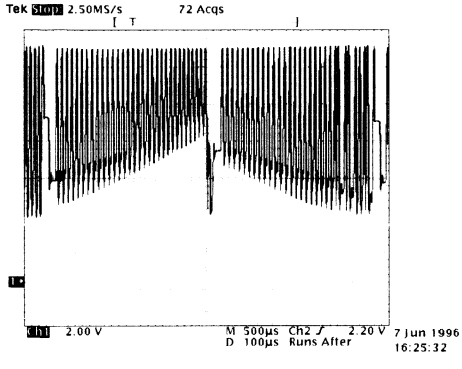


Spectrum with Quiet Commutation On

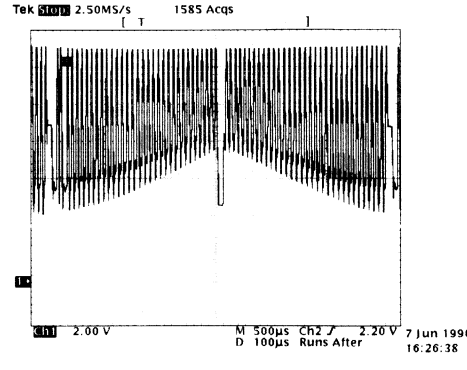


Spectrum with Quiet Commutation Off

Figure 5 .



No Phase Advance



10° Phase Advance

Figure 6 .

Figure 5 shows the spectra of the supply current under the same two conditions. Note the relative amplitudes of the single-frequency peaks at the commutation frequency (2.16 kHz) and its harmonics. The first peak is the fundamental 2.16-kHz commutation frequency, and the subsequent peaks are at the harmonics (4.32 kHz, 6.48 kHz, and so forth).

As the horizontal cursors show, the relative amplitudinal difference of the fundamental is 6.4 dB. *This is an equivalent reduction of 77% in sound power.*

Phase Advance Feature Provides Higher Motor Efficiency

The Si9993 allows phase switch timing to be optimized for greatest efficiency. This involves early phase switching (phase advance) to compensate for the electrical L/R delay.

Figure 6 shows wave forms taken at the center tap of the spindle motor relative to ground. The wave form on the left shows operation with no phase advance. Note the asymmetry of the rising and falling slopes. This asymmetry results in lower efficiency. In the trace on the right, the phase switch has been advanced by ten electrical degrees. Notice that the rising and falling slopes are symmetrical.

How the Si9993 Decreases ISV By Reducing Jitter

Figure 7 is a composite picture of 1552 revolutions. It plots a particular commutation switch as measured exactly one revolution from the same switch one revolution earlier. Once-around jitter here is 4 µs P-P. giving a speed accuracy of 0.024%. This data was taken using a simple first-order PI (proportional-integral) servo speed control loop on a motor running at 7200 rpm.

Figure 8 is a histogram displaying the distribution of the same jitter as in Figure 7 . Once-around timing errors for 32,000 revolutions are shown. Each bar represents the number of revolutions on the Y axis for the time jitter on the X axis. Each bin on the X axis is 200 ns. Here σ (standard deviation) is 0.616 µs.

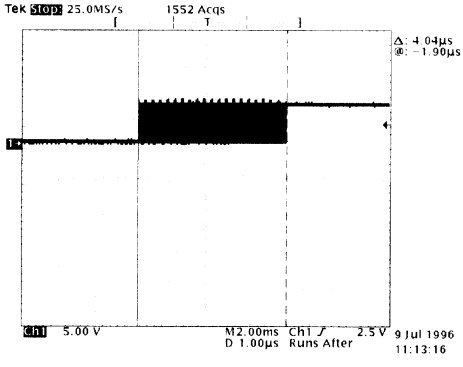


Figure 7 .

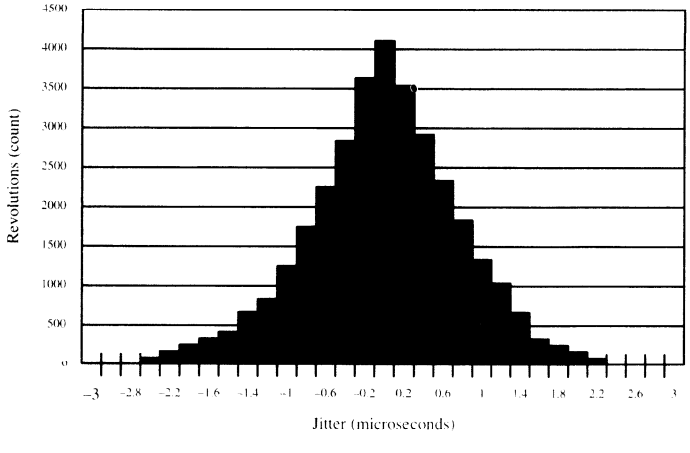


Figure 8 . Jitter Histogram

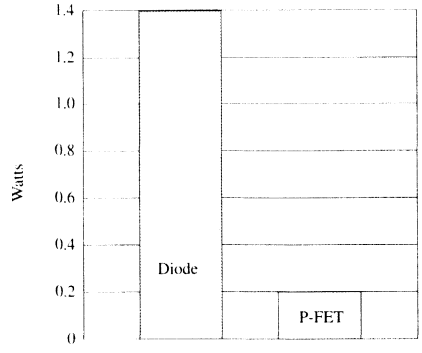


Figure 9 . Power Dissipation in Isolation Device

Power Failure Retract Circuit Provides More Efficient and Reliable Operation

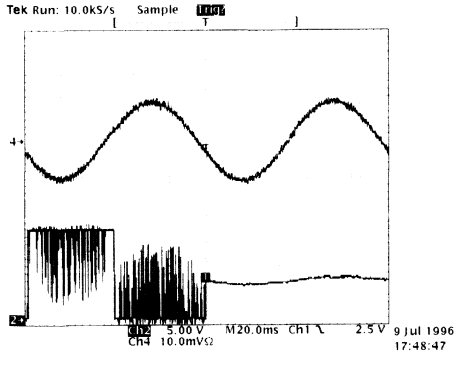
If power fails or is interrupted, the VCM must be retracted such that the heads touch down in the landing zone when the disks are finally stopped. To ensure that this happens, power generated by the kinetic energy stored in the spinning disks is used to drive the VCM. For proper operation, the generated power must be isolated from other circuits which would dissipate the kinetic energy in the disks before the VCM could be retracted. Most designs use a Schottky diode for isolation. The disadvantage of this approach is that the isolation device must pass all the spindle and VCM currents during normal operation. If a 0.7-V diode drop and a total current of 2 A are assumed, power dissipation is 1.4 W (P = VI). The Si9430DY p-channel power MOSFET is recommended for use with the Si9993. On-resistance for the Si9430DY is 0.05 Ω, resulting in a dissipation of only 0.2 W ($P = I^2R$). The two methods are compared in Figure 9. The on/off control of the p-channel MOSFET is performed by the Si9993 chip at the appropriate times.

Dual-Mode VCM Drive Reduces Dissipation During Seek While Maintaining Track-Follow Accuracy

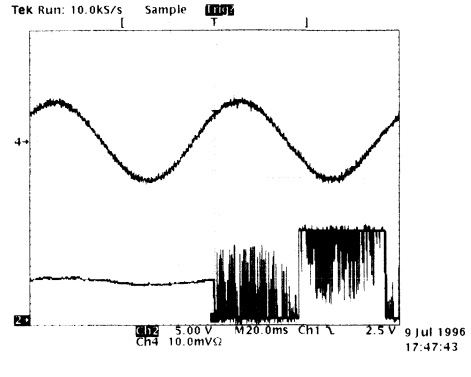
The VCM can also be driven in PWM mode. While the VCM is driven in a constant frequency mode and the spindle in a constant off-time mode, the power savings advantages apply equally for both cases. The VCM PWM mode is used primarily during seeking, where the VCM currents are relatively high. *The ability to attain these high VCM currents with low driver power dissipation allows high acceleration and deceleration profiles. Seek times are thus lower than would be possible with a strictly linear VCM drive.*

When a near on-track condition occurs (track following), the VCM driver is switched to a linear mode. This allows finer position control and lower EMI when critical read operations are required. Current is quite low during this time, hence there is little power dissipation in the drive FETs.

It is important to avoid any discontinuity or distortion in the effective current during the change from PWM to linear mode or vice versa, since acceleration may otherwise be affected. Figure 10 shows the VCM current and VCM voltage, driven from a sinusoidal source, when a switch from PWM to linear (right) and linear to PWM (left) is made. Notice that *there is no distortion of the sinusoidal current wave form during the switch.*



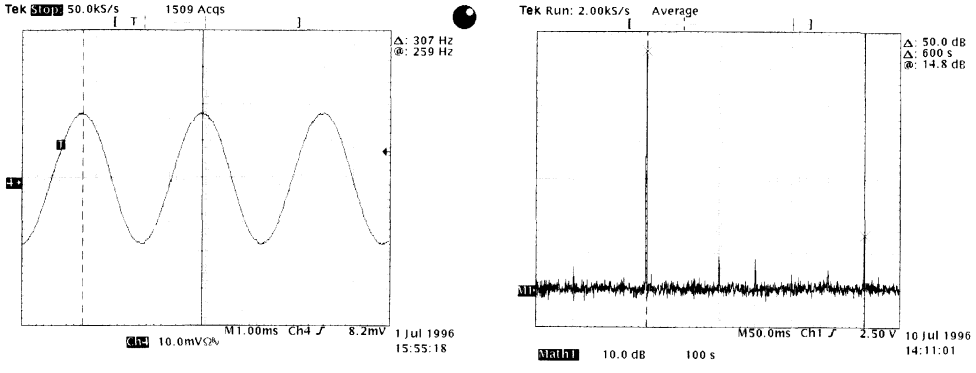
PWM to Linear Switch



Linear to PWM Switch

Figure 10 . VCM Current and Voltage During Drive Mode Switch

3 Motor Control



Time Domain

Frequency Domain

Figure 11 . VCM Crossover Distortion

The linear mode features an ingenious class AB amplifier which does not require trimming to compensate for various output devices. The crossover current near zero is supplied by the Si9993. As the required current departs from a small range around zero, the output devices take over. *This allows relatively distortion-free operation even near zero current.*

Figure 11 shows the time (left) and frequency (right) domain of a 200-mA P-P, 300-Hz sinusoidal linear VCM drive. The odd harmonics (X3 and X5, for example, but primarily the X3 component) are an indication of crossover distortion. In the spectrogram shown, the third harmonic is down 50.0 dB. *This is equal to a third harmonic distortion of only 0.32%.*

Serial Port Provides Flexibility for Different Model HDDs and Reduces External Component Count

Parameters such as spindle transconductance, VCM transconductance, slew rate control off/on, "Quiet Commutation," spindle PWM off time, spindle phase advance, VCM mode (linear/PWM), VCM PWM frequency, and the power down VCM retract/ spindle brake sequence are all programmable via registers accessible through a serial port, compatible with the 80196 protocol. *This allows PC boards to be identical for several models of HDDs, reducing inventory problems. Individual model personalities can then be programmed from the non-user tracks on the HDA written during HDA / PWB assembly or at servo write.*

Register programmability also reduces the number of external passives needed. Only 22 passive parts (Rs and Cs), and six active devices (power FETs) are required for a complete solution.

Figure 12 is a functional block diagram of the Si9993. The upper half is the VCM section; the lower half is the spindle section. Figure 13 is the typical application diagram for the device showing the external components and connections.

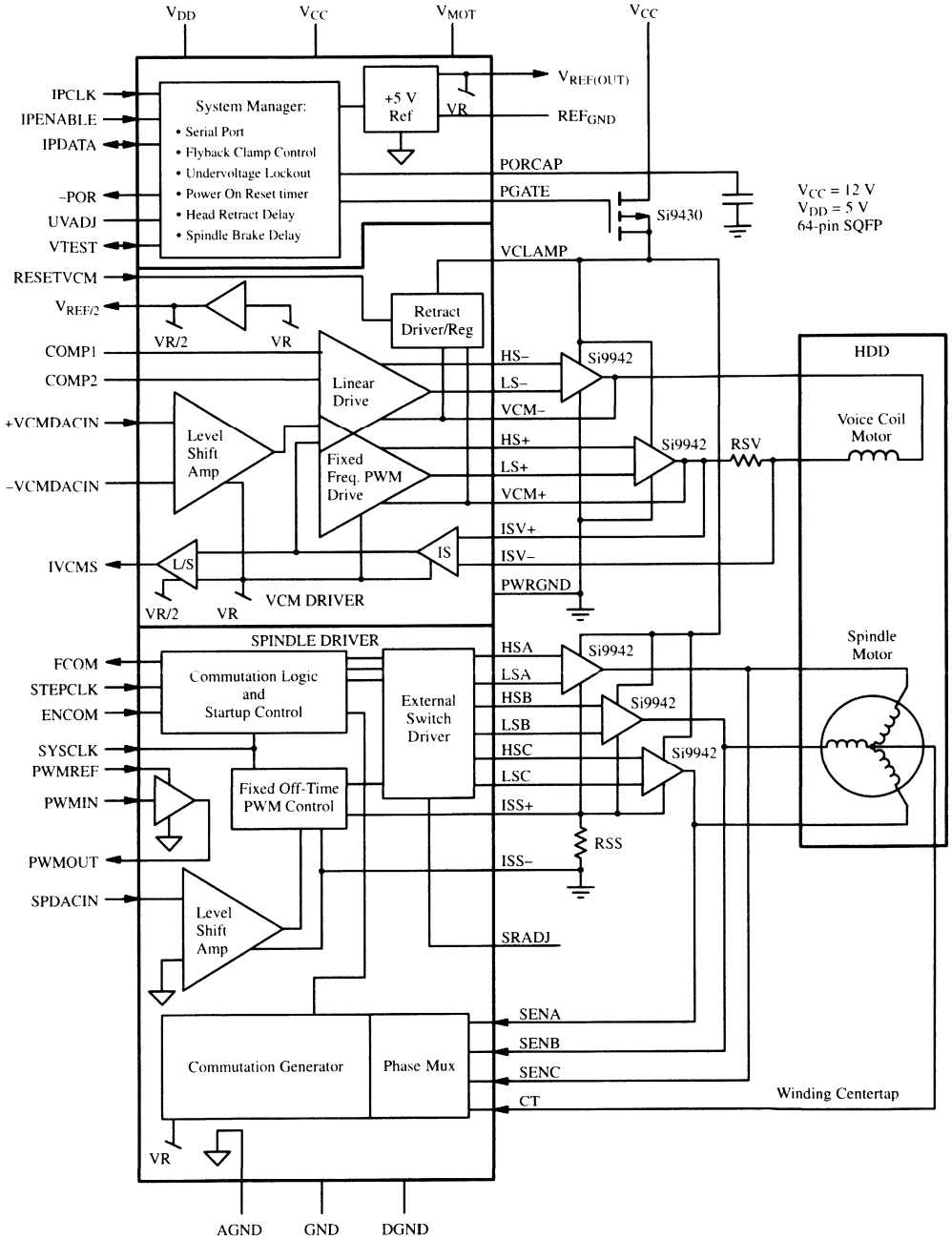


Figure 12 . Functional Block Diagram

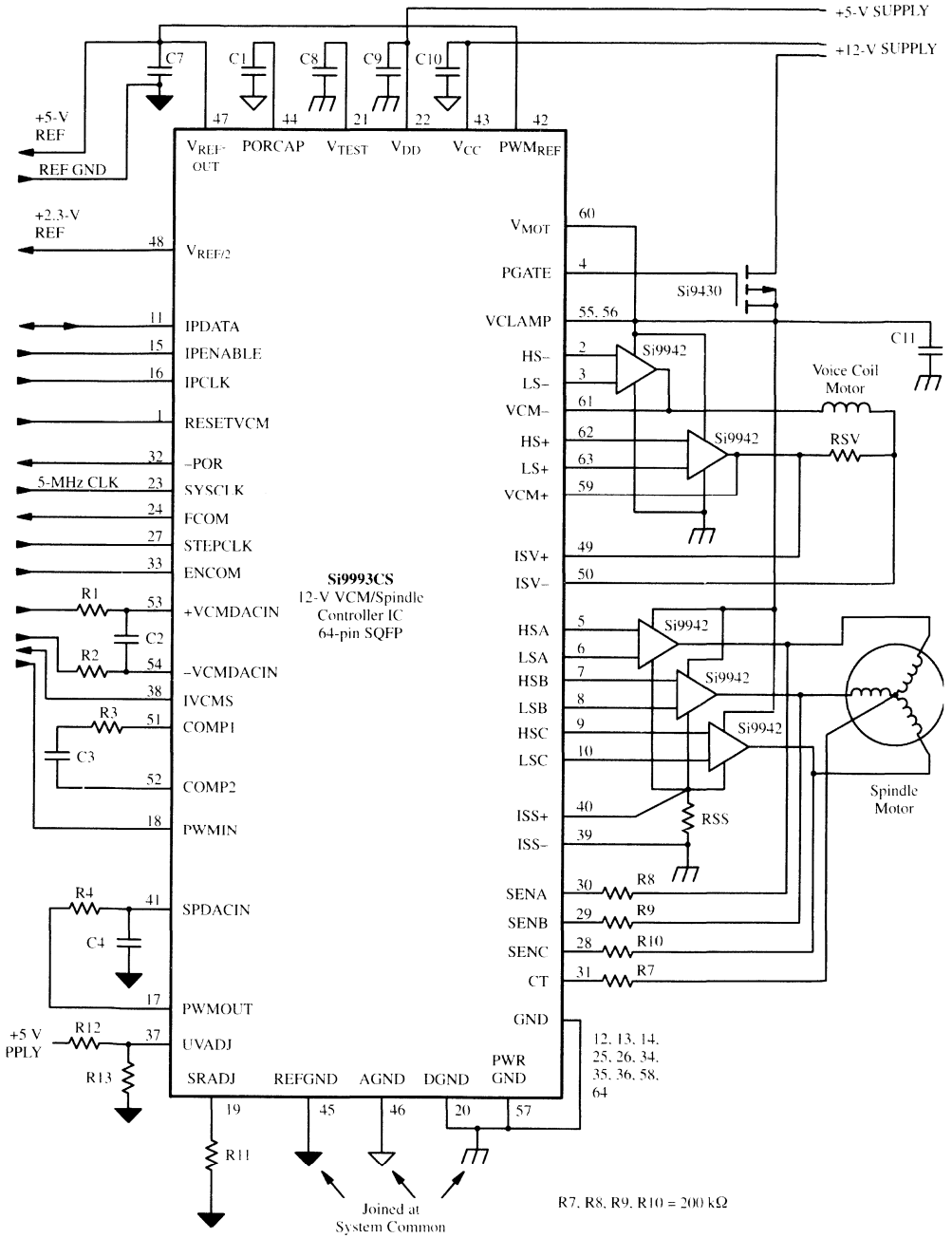


Figure 13 . Application Diagram

Dual H-Bridge Controller

Features

- One IC controls Two Bridges
- Voltage and Current PWM Control
- Separate Enable Input for each Bridge
- SPI Bus Interface
- Over Temperature Protection
- Oscillator Ramp Sync to CLOCK
- Internal Watchdog
- Fault Output (Open Drain)
- Selectable Shoot Through Control
- External or Internal Gate Supply Voltage
- Bootstrap Capacitor High Side
- 40-V Load Dump Protected

Description

The Si9600EY dual H-bridge controller independently controls two H-bridges by serial bus. Each bridge can be operated using current and/or voltage mode control with critical limits (such as maximum current and maximum duty cycle) being set over the serial bus.

Several available built-in modes and diagnostic settings are programmable across the serial bus. The two switching modes are shared switching and lower recirculation only. All switching is done syncronously.

The Si9600EY provides two types of diagnostics. The first monitors temperature, V_{DD}, V_{BAT} and V_{GATE}, and operates countinuously. A second set of diagnostics monitors open load and shorted load to V_{BAT} or GND. This monitoring can be disabled over the bus.

The Si9600EY has several other unique features to help in fine tuning the breadboard design. Shoot-through delay and watchdog time out can be programmed over the serial bus. The Si9600EY can also be configured as four halt bridges.

The Si9600EY is built on TEMIC's BiCD60 process and is packaged in a 48-pin SQFP.

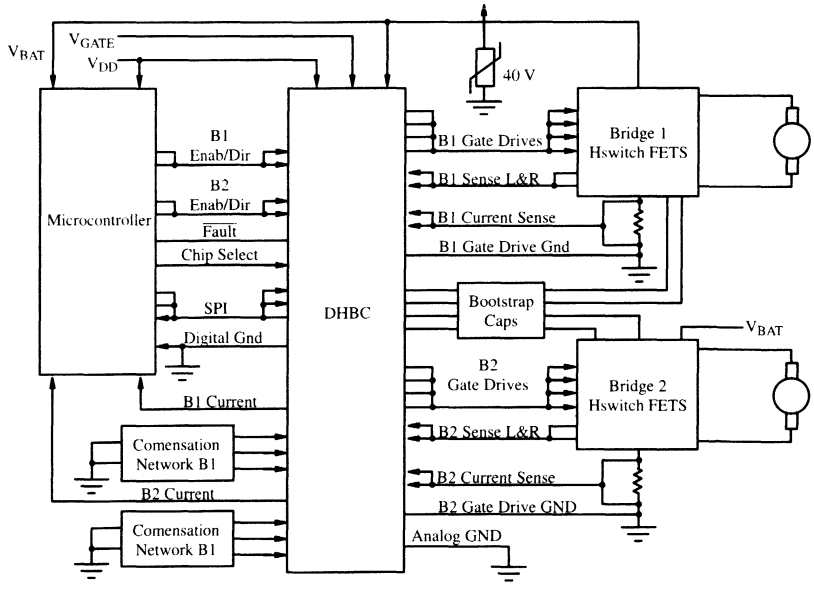


Figure 1. Dual Bridge Configuration

This product is currently in development. Inquiries regarding the status of this product should be directed to Siliconix Marketing.

Pre-Release Information

Absolute Maximum Ratings

Analog Voltages Referenced to AGND
Logic Voltages Referenced to DGND

V_{DD} ..... –0.3 to 7.0 V
V_{BAT} ..... –0.3 to 40 V
V_{GATEX} ..... –0.3 to 15 V
Logic Inputs ..... –0.3 V to V_{DD} + 0.3 V
Bridge Sense Inputs ..... –5.0 V to 40.0 V
Current Sense Inputs:
B1 & B2 CS+ ..... –0.7 V to V_{DD} + 0.3 V
B1 & B2 CS– ..... –0.35 V to V_{DD} + 0.3 V
Storage Temperature (T_{stg}) ..... –55 to 150°C
Junction Temperature (T_J) ..... –40 to 150°C
Thermal Impedance (Θ_{JA})
48-pin SQFP ..... 74°C/W

Exposure to Absolute Maximum rating conditions for extended periods may affect device reliability. Stresses above Absolute Maximum rating may cause permanent damage. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum rating should be applied at any one time

Recommended Operating Range

V_{DD} ..... 4.75 to 5.25 V V_{IH} 0.7* V_{DD}
V_{BAT} ..... 7.0 to 18.0 V
V_{GATEX} ..... 8.0 to 12.0 V
V_{IH} ..... 0.7 * V_{DD} to V_{DD} + 0.3 V
V_{IL} ..... –0.3 to 0.3 * V_{DD} + 0.3 V
T_A ..... –40 to 125°C

DC Electrical Specifications

Parameter	Symbol	Test Conditions 4.75 ≤ V_{DD} ≤ 5.25 V 8 ≤ V_{GATEX} ≤ 12 V 7 ≤ V_{BAT} ≤ 18 V	Limits T_A = –40 to 125°C Min[a]	Typ[b]	Max[a]	Unit
Logic (Digital and Analog) Supply						
Logic Supply Voltage	V_{DD}		4.75		5.25	V
Logic Supply Current	I_{DD}				4.0	mA
External Gate Supply						
External Gate Supply Voltage	V_{GATEX}		8.0		12.0	V
External Gate Supply Current	I_{GATEX}				5.0	mA
External Gate Supply Leakage Current	I_{LEAK}	$V_{GATEX(max)}$ and any of: Bridge Fault, $T_J > T_{J(OT)}$, or V_{DD} , $V_{DD(UV)}$			10	µA
Bridge and Internal Gate Supply						
Protected Battery Voltage	V_{BAT}		7.0	13.5	18.0	V
Protected Battery Current	I_{BAT}				1.0	mA
Protected Battery Leakage Current	$I_{BAT(LEAK)}$	$B_{BAT(max)}$, any Fault			100	µA
Gate Driver Outputs (B1 and B2 UL, UR, LL, LR Gates)						
Output High	V_{OH}	I_{OUT} = 150 mA	V_G – 2.25			V
Output Low	V_{OL}	I_{OUT} = –150 mA			2.25	
Clamp Gate to Ground Voltage	V_{GG}	I_{OUT} = –5 mA, V_{DD} = 0 V			500	mV
Clamp Gate to Source Voltage	V_{GS}	I_{OUT} = –5 mA, V_{GATE} < $V_{GATE(UV)}$			500	
Bootstrap Leakage Current	I_{BSLEAK}	Upper Gate Drives = V_{GATE} R_L = Open			1	µA

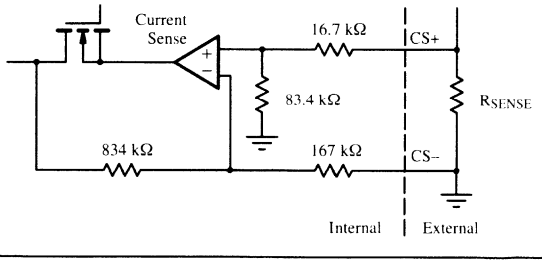
DC Electrical Specifications

Parameter	Symbol	Test Conditions $4.75 \le V_{DD} \le 5.25$ V $8 \le V_{GATEX} \le 12$ V $7 \le V_{BAT} \le 18$ V	Limits $T_A = -40$ to $125°C$			Unit
			Min[a]	Typ[b]	Max[a]	
Logic Inputs (CS, DI, SCLK, B1 and B2 DIR, B1 and B2 ENABLE)						
Input High Voltage	V_{IH}		$0.7 * V_{DD}$		$V_{DD} + 0.3$	V
Input Low Voltage	V_{IL}		–0.3		$0.3 * V_{DD}$	
Input Leakage Current	I_{LEAK}		–1		1	µA
Logic Outputs (DO)						
Output High Voltage: DO	V_{OH}	$I_{OUT} = 2$ mA	$V_{DD} - 0.5$			V
Output Low Voltage: DO	V_{OL}	$I_{OUT} = -2$ mA			0.5	
Current Sense Amplifier (B1 and B2), $R_L = R_{L(min)}$, $C_L = C_{L(max)}$						
Input Differential Voltage	V_{ID}	V(+) – V(–)			350	mV
Input Offset Voltage	V_{IO}	$V_{CM} = 0$ V, $V_O = 0$ V	–3.5		3.5	
Average Temperature Coefficient of V_{IO}	$\Delta V_{IO}/\Delta T$			10		µV/°C
Input Bial Current	I_{IB}				700	nA
Input Offset Current	I_{IO}				300	
Input Common Mode Voltage Range	V_{ICR}		0		100	mV
Amplifier Closed Loop Gain	A_{VCL}	$V_{ID} = \pm 350$ mV	4.90		5.10	V/V
Output Voltage Swing Low	V_{OL}	$V_{ID} = -350$ mV			0	V
Output Short Circuit Current Source	I_{SC}	$V_{ID} = 350$ mV, $V_O = 0$ V	tbd			mA
Output Short Circuit Current Sink		$V_{ID} = 0$ mV, $V_O = 1.75$ V	tbd			
Common Mode Rejection Ratio[c]	CMR		60			dB
Power Supply Rejection Ratio[c]	PSR		60			
Feedback Network Current	I_{FDBK}	$V_{DD} = 0$ V, $V_{ID} = 0$ V R_L = Open, $V_O = 1$ V	0.75		1.25	µA
Load Resistor	R_L		10			kΩ
Load Capacitor	C_L				0.047	µF
Current Output Amplifier (B1 and B2), $R_L = R_{L(min)}$						
Amplifier Gain	A	$V_{ID} = 1.75$ V	1.92		2.08	V/V
Input Offset Voltage	V_{IO}	$V_{CM} = 0$ V, $V_O = 0$ V	–10		10	mV
Output Short Circuit Current Source	I_{SC}	$V_{ID} = 1.75$ V, $V_O = 0$ V	400			µA
Output Short Circuit Current Sink		$V_{ID} = 1.0$ V	100			
Load Resistor	R_L		10			kΩ
Current Error Amplifier (B1 and B2), $R_L = R_{L(min)}$						
Amplifier Open Loop Gain	A_{VOL}	$V_{ID} = 1.75$ V	1000			V/V
Common Mode Rejection Ratio[c]	CMR		60			dB
Power Supply Rejection Ratio[c]	PSR		60			
Load Resistor	R_L		50			kΩ

DC Electrical Specifications

Parameter	Symbol	Test Conditions $4.75 \le V_{DD} \le 5.25$ V $8 \le V_{GATEX} \le 12$ V $7 \le V_{BAT} \le 18$ V	Limits $T_A = -40$ to 125°C Min[a]	Typ[b]	Max[a]	Unit
Voltage DAC (B1 and B2)						
Resolution				7		Bits
Monotinicity			7			
Integral Non-linearity[d]	INL		−1		1	LSB
Zero Scale Error			0		3	
Maximum Scale Error			0		3	
Current DAC (B1 and B2)						
Resolution				8		Bits
Monotinicity			8			
Integral Non-linearity[d]	INL		−1		1	LSB
Zero Scale Error			0		3	
Maximum Scale Error			0		3	
Fault Conditions						
T_J Over Temperature[c]	$T_{J(OT)}$	Rising Through	150		165	°C
$T_{J(OT)}$ Hysteresis	$T_{J(HYS)}$	Falling		10		
V_{GATE} Under Voltage	$V_{GATE(UV)}$	Falling Through	6.50		7.25	V
$V_{GATE(UV)}$ Hysteresis	$V_{GATE(HYS)}$	Rising		0.5		
V_{DD} Under Voltage	$V_{DD(UV)}$	Falling Through	3.25		4.00	
$V_{DD(UV)}$ Hysteresis	$V_{DD(HYS)}$	Rising		0.5		
Short to Supply Detect Voltage	$V_{SUP(short)}$		0.80 * V_{DD}		0.85 * V_{DD}	
Short to GND Detect Voltage	$V_{GND(short)}$		0.15 * V_{DD}		0.20 * V_{DD}	
Saturation Detect Voltage	V_{SAT}		0.45 * V_{BAT}		0.55 * V_{BAT}	
Fault Output MOSFET (Open Drain), $R_L = R_{L(min)}$ (Pull-Up)						
Output Low Voltage	V_{OL}				200	mV
Leakage Current	$I_{DS(off)}$		−1		1	µA
Pull-Up Load Resistor	R_L		2			kΩ

Notes
a. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum.
b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing. In addition, characterization ± 3 sigma limits are to be available for reference.
c. Guaranteed by characterization, not subject to production testing.
d. Integral non-linearity is measured using actual zero and full scale of the DAC.
e. One pin at a time, observing maximum power dissipation limits.
f. Reference diagram for internal connections of current sense amplifier.



AC Electrical Specifications

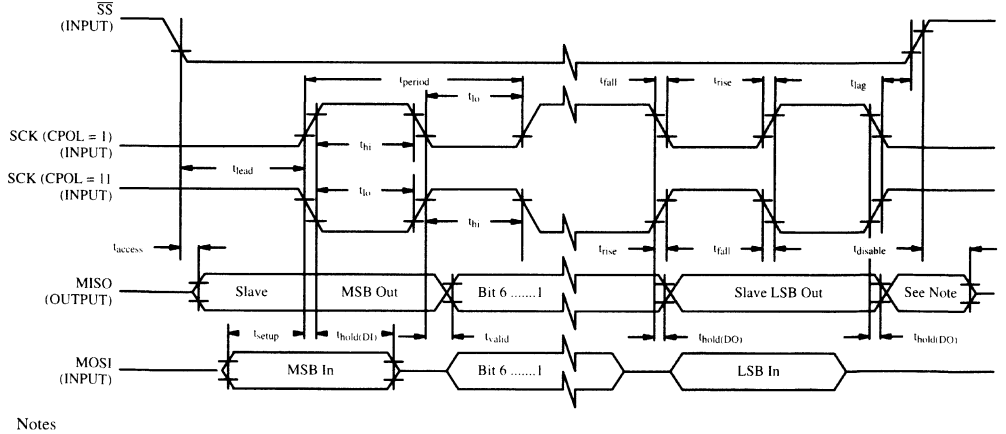
Parameter	Symbol	Test Conditions $4.75 \le V_{DD} \le 5.25$ V $8 \le V_{GATEX} \le 12$ V $7 \le V_{BAT} \le 18$ V	Limits $T_A = -40$ to $125°C$			Unit
			Min[a]	Typ[b]	Max[a]	
Bootstrap Refresh						
Refresh Pulse Off Time	t_{OFF}		45		57	mS
Refresh Pulse On Time	t_{ON}		1.5		3.0	µS
Current Sense Amplifier (B1 and B2)						
Slew Rate Coupled	SR		tbd			V/µS
Slew Rate Decoupled			tbd			
Settling Time	t_S					µS
Gain Bandwidth Product[c]	GBW		100			kHz
Phase Margin[c]	Φ_m		40			Deg
Gain Margin	A_m			4		dB
Current Sense Amplifier (B1 and B2), $R_L = R_{L(min)}$						
Slew Rate Coupled	SR		0.1			V/µS
Gain Bandwidth Product[c]	GBW		500			kHz
Phase Margin[c]	Φ_m		75			Deg
Gain Margin	A_m			4		dB
Gate Drivers						
V_{SAT} Detect Delay 1	t_{dly1}		2.25		4.50	µS
V_{SAT} Detect Delay 2	t_{dly2}		5.25		10.50	
Shoot Through Delay 1	t_{dly1}		3.00		6.00	
Shoot Through Delay 2	t_{dly2}		5.25		10.50	
Gate Rise (20 to 80%)	t_{rise}	$C_L = 4000$ pF, $V_{GATEX} = 12$ V			500	nS
Gate Fall (20 to 80%)	t_{fall}				500	
Logic Inputs (CS, DI, SCLK, B1 and B2 DIR, B1 and B2 ENABLE)						
Input Capacitance[c]	C_{IN}	$-0.3 \le V_{DD} \le 5.25$			20	pF
Oscillator						
Frequency	f_{OSC1}		18		22	kHz
	f_{OSC2}		8.5		11.5	
SPI (DO, DI, SCLK, CS)[d]						
Operating Frequency	f_{sclk}				4	MHz
Operating Period	t_{period}		250			nS
Enable Lead, CS to SCLK	t_{lead}		200			
Enable Lag, SCLK to CS	t_{lag}		200			
Clock High	t_{hi}		85			
Clock Low	t_{lo}		85			
Data Setup, DI to SCLK	t_{setup}		100			
Data Hold Input, SCLK to DI	$t_{hold(DI)}$		100			
Access, Tri-State to Active Data	t_{access}				120	
Disable, Active Data to Tri-State	$t_{disable}$				125	
Data Valid, After SCLK Edge	t_{valid}	$C_L = 200$ pF			105	
Data Hold Output, SCLK to DO	$t_{hold(DO)}$		0			

AC Electrical Specifications

Parameter		Symbol	Test Conditions 4.75 ≤ V_{DD} ≤ 5.25 V 8 ≤ V_{GATEX} ≤ 12 V 7 ≤ V_{BAT} ≤ 18 V	Limits T_A = –40 to 125°C Min[a]	Typ[b]	Max[a]	Unit
SPI (DO, DI, SCLK, CS) (cont'd)[d]							
RiseTime[c]	CS, DI, SCLK	t_{rise}	C_L = 200 pF, 0.2 to 0.7 of V_{DD}			2	µS
	DO					100	nS
FallTime[c]	CS, DI, SCLK	t_{fall}				2	µS
	DO					100	nS
Watchdog							
Microcontroller Operating Timer		COP					mS

Notes
a. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum.
b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing. In addition, characterization ± 3 sigma limits are to be available for reference.
c. Guaranteed by characterization, not subject to production testing.
d. SPI Timing (Dual H-Bridge is a slave only device).

SPI Timing Diagram

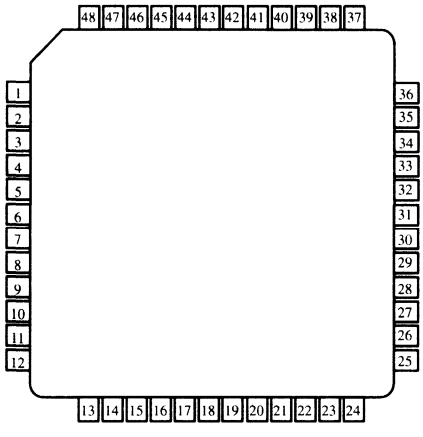


Notes
a. Not defined but normally MSB of character just received.
b. When chip select (CS) is low, the data out (DO) pin must be tri-stated

Figure 2. SPI Timing

Pin Configuration

SQFP-48



Top View

Pinout			
Pin #	**Pin Name**	**Pin #**	**Pin Name**
1	B1_LL_Gate	25	B2_LR_Gate
2	B1_UL_BS	26	B2_UR_BS
3	B1_UL_Gate	27	B2_UR_Gate
4	B1_sense_l	28	B2_sense_r
5	B1_dir	29	B2_GD_GND
6	B1_err_fb	30	B2_error_out
7	B1_error_out	31	B2_err_fb
8	B1_GD_GND	32	B2_dir
9	B1_sense_r	33	B2_sense_L
10	B1_UR_Gate	34	BL_UL_GATE
11	B1_UR_BS	35	BL_UL_BS
12	B1_LR_Gate	36	BL_LL_GATE
13	FLTb	37	B2_ena
14	DI	38	B2_x10_cur
15	SCLK	40	B2_CS+
16	V_{BAT}	41	B2_CS–
17	V_{DD}	42	B2_x5_cur
18, 19, 39, 47	AGND	43	B1_x5_cur
20	DGND	44	B1_CS+
21	V_{GATE}	45	B1_CS–
22	DO	46	B1_x10_cur
23	CS	48	B1_ena
24	NC		

Functional Block Diagrams

The block diagrams illustrate a method for PWM voltage control with a closed-loop current limit.

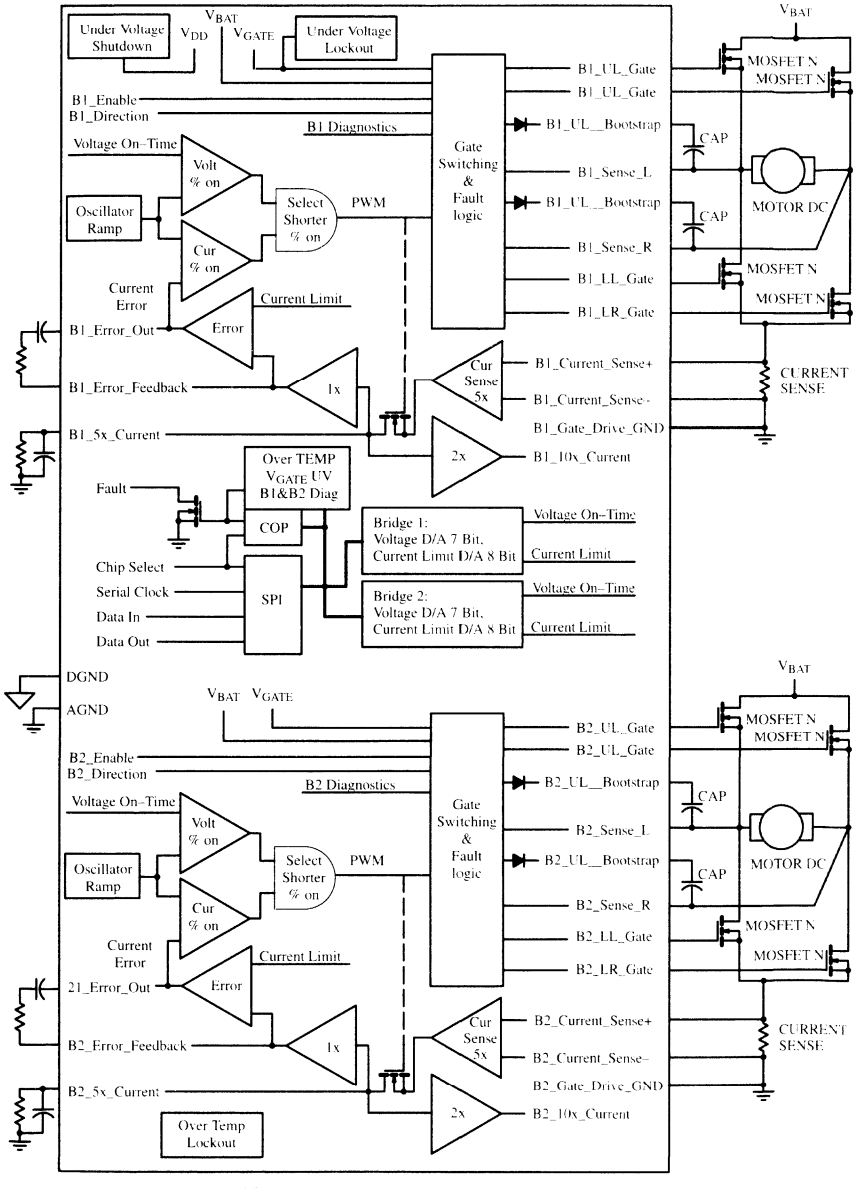


Figure 1. Two H-Bridge Block Diagram

Functional Block Diagrams

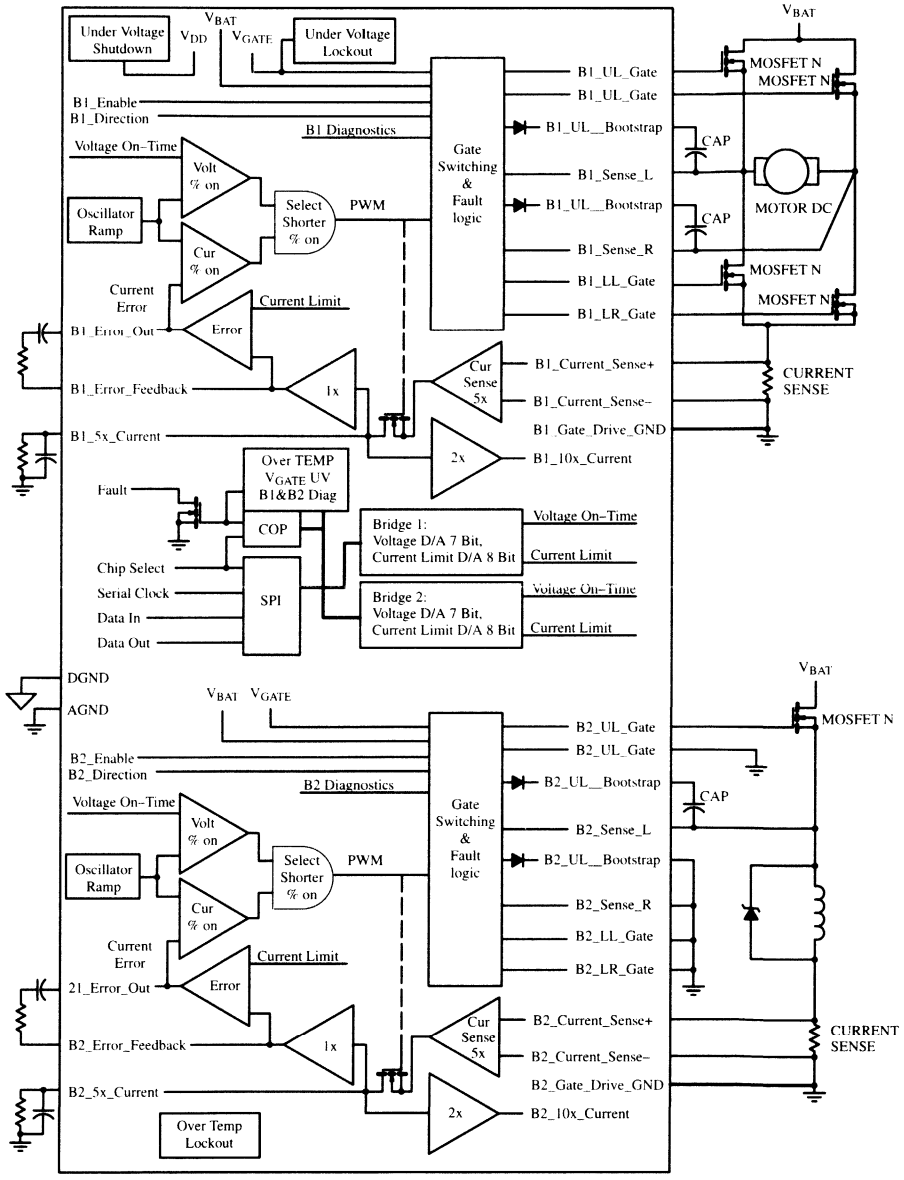


Figure 2. H-Switch and High-Side Driver Block Diagram

Interface ICs

Siliconix offers three bus ICs designed for use in the automotive and industrial market. The Si9241EY and Si9243EY are low cost serial bus drivers, which meet the ISO-9141 standard. These drivers are designed for applications where space and ruggedness are critical. Applications include: engine control (CARB), ABS, window lifts, door locks, security, and keyless entry.

The Si9200EY is a CAN driver designed for high-speed applications where noise immunity, space, and ruggedness are critical. CAN is a differential bus used in real-time applications. Applications include: engine control, ABS, transmission control, industrial robotics, and assembly.

Selector Guide

Part Number	Description	Function	Ambient Temperature	Bus	Features	Package	Page Number
Si9200EY	CAN Bus Driver and Receiver	CAN	–40 to 125°C	Differential	1 Mbit/sec	SO-8	4-1
Si9241EY	Single-Ended Bus Tranceiver	ISO-9141	–40 to 125°C	Singel-Ended	K only	SO-8	4-5
Si9243EY	Single-Ended Bus Tranceiver	ISO-9141	–40 to 125°C	Singel-Ended	K and L	SO-8	4-9

CAN Bus Driver and Receiver

Features

- Survives Ground Shorts and Transients on Multiplexed Bus in Automotive and Industrial Applications
- Single Power Supply
- Compatible with Intel 82526 CAN Controller
- Direct Interface – No External Components Required
- Automotive Temperature Range (–40 to 125°C)

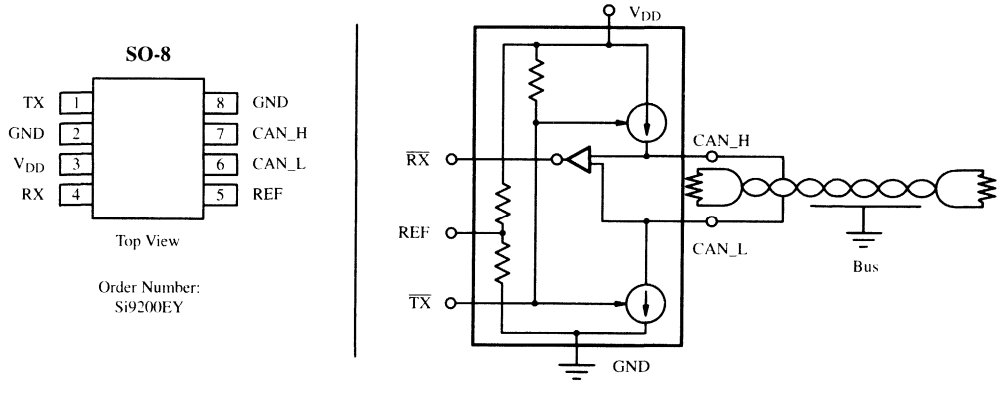
Description

The Si9200EY is designed to interface between the Intel 82526 CAN controller and the physical bus to provide drive capability to the bus and differential receive capability to the controller. It is designed to absorb typical electrical transients on the bus which may occur in an automotive or industrial application, and protect itself against any abnormal bus conditions. The transmitter will be disabled during these conditions and will be re-enabled when the abnormal condition is cleared.

The Si9200EY is built using the Siliconix BiC/DMOS process. This process supports CMOS, DMOS, and isolated bipolar transistors and uses an epitaxial layer to prevent latchup. The bus line pins are diode protected and can be driven beyond the V_{DD} to ground range.

The Si9200EY is offered in the space efficient 8-pin high-density surface-mount plastic package and is specified over the automotive temperature range (–40 to 125°C).

Pin Configuration and Functional Block Diagram



Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70015.

Absolute Maximum Ratings[a]

Operating Temperature (T_A) ..... –40 to 125°C
Junction and Storage Temperature ..... -55 to 150°C
Voltage On Any Pin (Except CAN_H and CAN_L)
with Respect to Ground ..... –0.3 to V_{DD} +0.3 V
Voltage On CAN_H and CAN_L
with Respect to Ground ..... –3 to +16 V
Supply Voltage, V_{DD} ..... –0.3 to 12 V
Continuous Output Current ..... ± 100 mA

Thermal Ratings[b]: $R_{\Theta JA}$ ..... 62.5°C/W (no airflow)

Notes
a. Extended exposure to the absolute maximum ratings or stresses beyond these ratings may affect device reliability or may cause permanent damage to the device. Functional operation at conditions other than the recommended operating conditions is not implied.
b. Mounted on 1-IN^2, FR4 PC Board.

Recommended Operating Conditions

V_{DD} ..... 4.75 to 5.25 V
Bus Load Resistance ..... 60 Ω

Specifications

Parameter	Symbol	Test Conditions Unless Otherwise Specified V_{DD} = 4.75 to 5.25 V		Limits T_A = –40 to 125°C Min[b]	Typ[a]	Max[b]	Unit
Input							
$\overline{TX}$ Input Voltage High	V_{INH}			4			V
$\overline{TX}$ Input Voltage Low	V_{INL}					1	
$\overline{TX}$ Input Current Low	I_{IL}	$\overline{TX}$ = 0 V		–50		–2.0	µA
$\overline{TX}$ Input Current High	I_{IH}	$\overline{TX}$ = V_{DD}		–1.0		1.0	
Output							
Bus Recessive	V_{CAN_HR}, V_{CAN_LR}	$\overline{TX}$ = V_{INH}, R_L = ∞		2	2.5	3	V
	V_{DIF} = V_{CAN_HR} – V_{CAN_LR}			–0.5	0	0.05	
Bus Dominant	V_{CAN_HD}	$\overline{TX}$ = V_{INL}, R_L = 60 Ω		2.75	3.5	4.5	
	V_{CAN_LD}			0.5	1.5	2.25	
	V_{DIF} = V_{CAN_HD} – V_{CAN_LD}			1.5	2	3	
Reference Output	V_{REF}	–25 µA ≤ I_{REF} ≤ 25 µA		0.5 V_{DD} –0.2	0.5 V_{DD}	0.5 V_{DD} +0.2	
Receive Output (Bus Recessive Conditions)	$V_{\overline{RXH}}$	$\overline{TX}$ = V_{INH}, –2.0 V ≤ V_{CAN_H}, V_{CAN_L} ≤ 7 V, –1 V ≤ V_{CAN_H} – V_{CAN_L} ≤ 0.5 V (Bus Recessive)	I_{OUT} = –10 µA	V_{DD} –0.3	V_{DD} –0.05		
			I_{OUT} = –100 µA	V_{DD} –1	V_{DD} –0.2		
			I_{OUT} = –2 mA	V_{DD} –1.75	V_{DD} –1		
Receive Output (Bus Dominant Conditions)	$V_{\overline{RXL}}$	$\overline{TX}$ = V_{INH}, –0.8 V ≤ V_{CAN_H} ≤ 7 V, –2 V ≤ V_{CAN_L} ≤ 5.8 V, 0.9 V ≤ V_{CAN_H} – V_{CAN_L} ≤ 5 V (Bus Dominant)	I_{OUT} = 10 µA		0.05	0.3	
			I_{OUT} = 100 µA		0.2	1	
			I_{OUT} = 2 mA		1	1.75	

Specifications

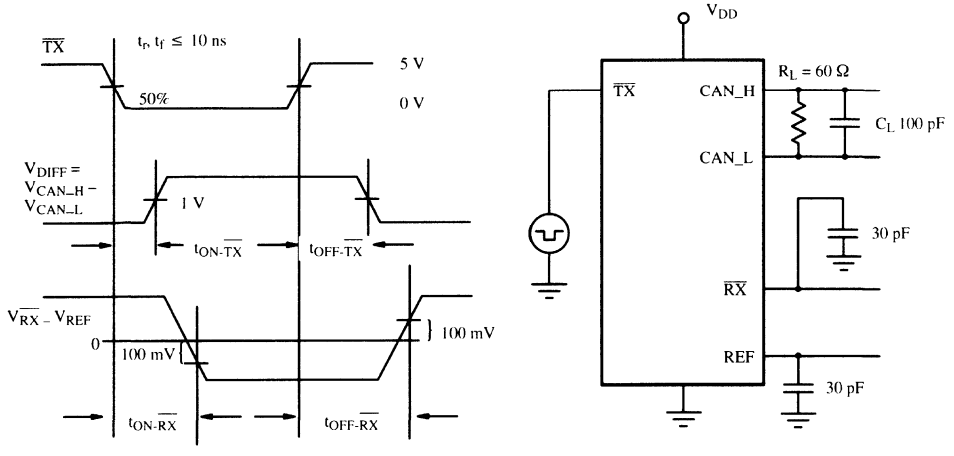
Parameter	Symbol	Test Conditions Unless Otherwise Specified V_{DD} = 4.75 to 5.25 V	Limits T_A = –40 to 125°C Min[b]	Typ[a]	Max[b]	Unit
Output (Cont'd)						
Internal Resistance from Bus Pins	R_{IN}, BUS_L	$\overline{TX}$ = V_{INH} (Recessive)	5		50	kΩ
	R_{IN}, BUS_H		5		50	
	R_{DIFF}		10		100	
Internal Capacitance from Bus Pins[c]	C_{IN} (CAN_H, CAN_L)				50	pF
Dynamic						
Propagation Delay – $\overline{TX}$ to V_{DIFF} High	$t_{ON\ \overline{TX}}$				50	ns
Propagation Delay – $\overline{TX}$ to V_{DIFF} Low	$t_{OFF-\overline{TX}}$				50	
Propagation Delay – $\overline{TX}$ to Receive Low	$t_{ON-\overline{RX}}$				120	
Propagation Delay – $\overline{TX}$ to Receive High	$t_{OFF-\overline{RX}}$				120	
Supply						
Supply Current	I_{DD}	$\overline{TX}$ = V_{INH}, V_{DD} = 5.25 V, R_L = 60 Ω (Recessive)			25	mA
		$\overline{TX}$ = V_{INL}, V_{DD} = 5.25 V, R_L = 60 Ω (Dominant)	40		75	
Transient[c]						
Electrostatic Discharge Human Body Model	V_{ESD}	C_L = 100 pF, R_L = 1500 Ω MIL-STD-883D, Method 3015		2000		V
Bus Transient Voltage	V_{TRANS}	R_S = 1000 Ω, 1 msec	–60		60	
Protection						
Thermal Trip Point[c]	T_{TRP}		150	165	180	°C
Thermal Hysteresis[c]	T_{HYS}		10	20	30	

Notes
a. Typical values are for DESIGN AID ONLY at T_A = 25°C, not guaranteed nor subject to production testing.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum.
c. Guaranteed by design, not subject to production test.

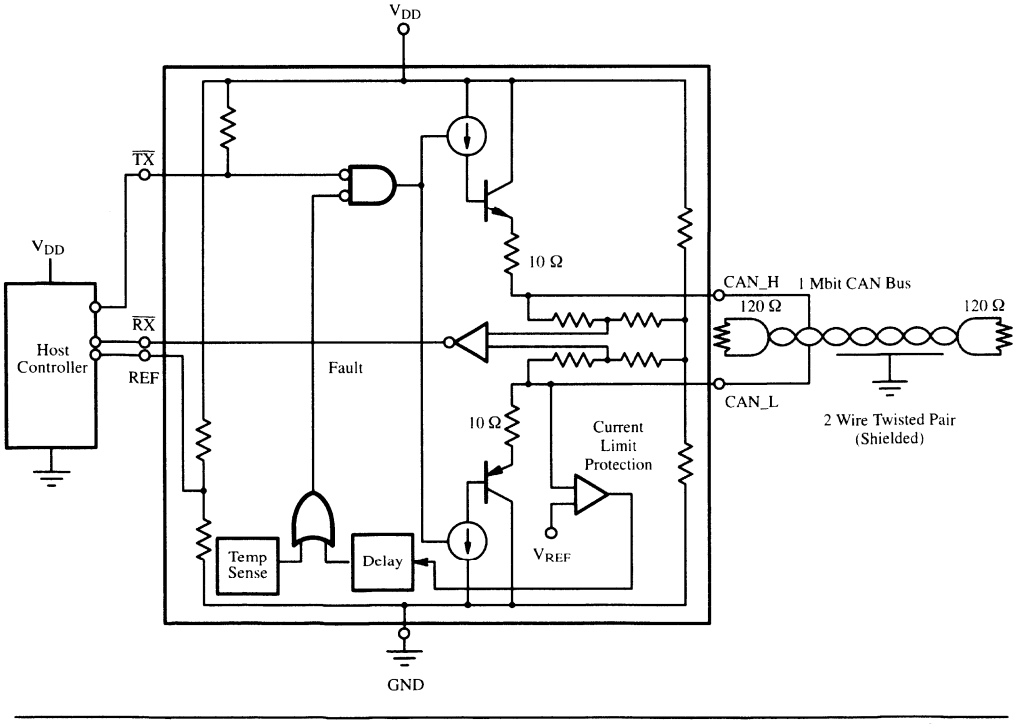
Truth Table

$\overline{TX}$	Mode	Bus State	CAN_H	CAN_L	RX
Low	Transmit	Dominant	High	Low	Low
High (or Floating)	Transmit and Receive	Recessive	Floating	Floating	High
High (or Floating)	Receive	Recessive	High	Low	Low

Switching Time Test Circuit



Circuit Schematic



Single-Ended Bus Transceiver

Features

- Single-Ended Transceiver
- Survives Shorts and Transients on Automotive Bus
- Wide Power Supply Voltage Range
- ISO 9141 Compatible
- Open Drain Fault Output

Benefits

- Single-Wire Multiplexer Interface
- ISO Diagnosis Bus

Applications

- Automobiles
- Trucks
- Tractors

Description

The Si9241EY is a monolithic bus transceiver designed to provide bidirectional serial communication in automotive diagnostic applications.

The device incorporates protection against overvoltages and short circuits to GND or V_B. The transceiver pin is protected and can be driven beyond the V_B voltage.

A fault output provides an active low in case of a short circuit or an open load. In the event of an over temperature condition, the output is immediately switched off and a fault indicated. This condition can only be reset once the over temperature condition is removed, and $\overline{CS}$ is toggled high.

For bi-directional communication, $\overline{CS}$ must be High for "receive" and Low for "transmit". If $\overline{CS}$ is Low, while IC is receiving data, an incorrect fault signal will occur. To inhibit the open load and short detect, tie $\overline{CS}$ and T_X together.

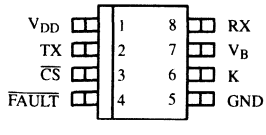
The Si9241EY is built on the Siliconix BiC/DMOS process. An epitaxial layer prevents latchup.

The RX output is capable of driving CMOS or 1 × LSTTL load.

The Si9241EY is available in a space efficient 8-pin SO package. It operates reliably over the automotive temperature range (–40 to 125°C).

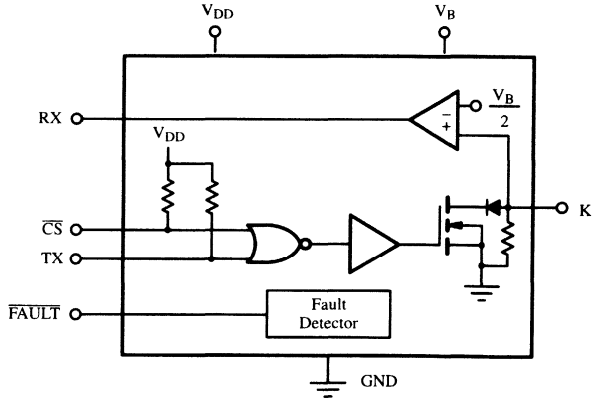
Pin Configuration and Functional Block Diagram

Narrow Body
SO Package



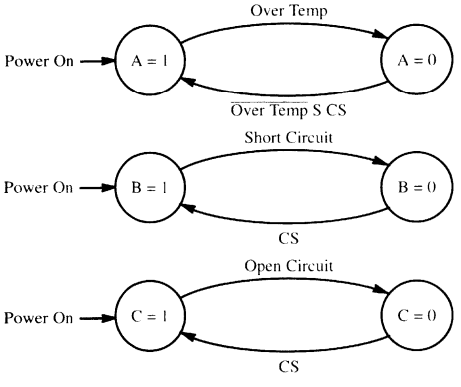
Top View

Order Number:
Si9241EY



Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70013. Application Note AN602 may also be obtained via FaxBack, request document #70573.

Output Table and State Diagrams



Inputs		State Variable			Output Table			
$\overline{CS}$	TX	A	B	C	RX	K	$\overline{FAULT}$	Comments
0	0	1	1	1	0	0	1	
0	1	1	1	1	1	1	1	
X	X	0	1	1	K	HiZ	0	Over Temp
0	X	1	0	1	K	HiZ	0	Short Circuit
0	X	1	1	0	K	HiZ	0	Open Circuit
1	X	1	1	1	0	0	1	Receive Mode
1	X	1	1	1	1	1	1	

X = "1" or "0"
HiZ = High Impedance State

Note: Over Temp is a condition and not meant to be a logic signal.

Absolute Maximum Ratings

Voltage Referenced to Ground
Voltage On V_{BAT} ..... 45 V
Voltage K ..... –16 V to (V_B + 1 V)
Voltage or Max. Current On Any Pin
(Except V_{BAT}, K) ..... –0.3 V to V_{DD} + 0.3 V or 10 mA

Voltage on V_{DD} ..... 7 V
Short Circuit Duration (to V_{BAT} or GND) ..... Continuous
Operating Temperature (T_A) ..... –40 to 125°C
Junction and Storage Temperature ..... -55 to 150°C
Thermal Resistance Θ_{JA} ..... 125°C/W

Specifications

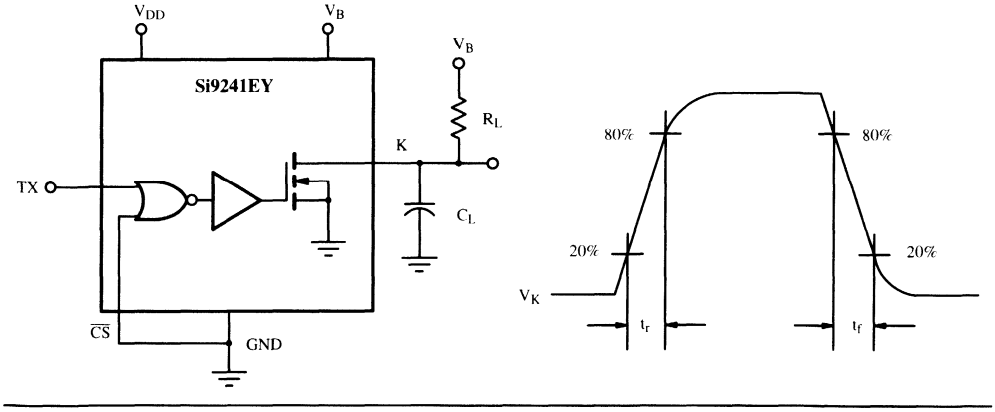
Parameter	Symbol	Test Conditions Unless Otherwise Specified V_{DD} = 4.5 to 5.5 V, V_{BAT} = 7.25 to 35 V	Temp[a]	Limits E Suffix: –40 to 125°C Min[b]	Typ[c]	Max[b]	Unit
Transmitter and Logic Levels							
$\overline{CS}$, TX Input Low Voltage	V_{ILT}		Full			1.5	V
$\overline{CS}$, TX Input High Voltage	V_{IHT}		Full	3.5			
K Output Low Voltage	V_{OLK}	R_L = 510 Ω, C_L = 10 nF V_{BAT} = 35 V, V_{DD} = 4.5 V	Full			4.9	
		R_L = 510 Ω, C_L = 10 nF See Test Circuit	Full			0.2 V_{BAT}	
K Output High Voltage	V_{OHK}		Full	0.91 V_{BAT}			
K Rise, Fall Times	t_r, t_f		Full			9.6	µs
K Output Sink Resistance	Rsi	$\overline{CS}$ = 0 V, TX = 0 V	Full			110	Ω
K Output Capacitance[d]	C_O	$\overline{CS}$ = 0 V	Full			20	pF
TX Input Capacitance[d]	C_{INT}		Full			10	
$\overline{CS}$, TX Input Current	I_{INT}	V_{DD} = 5.5 V, V_{INT} = 1.5 V, 3.5 V	Full	–60		–4	µA

Specifications

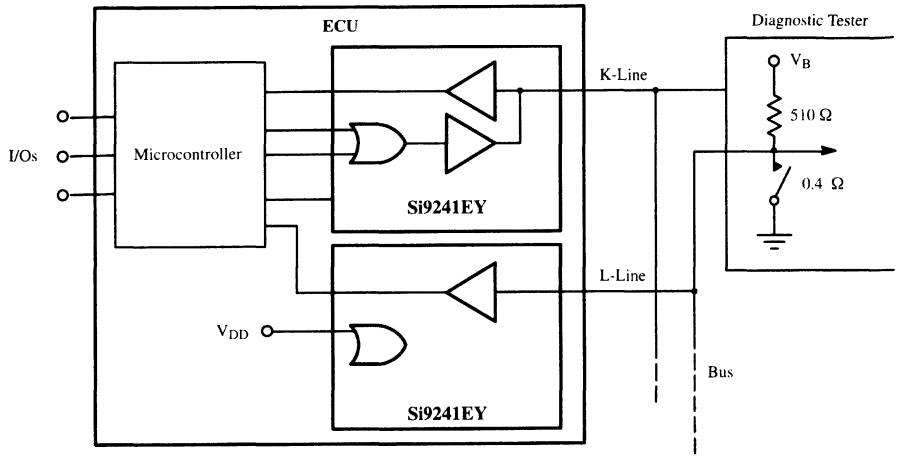
Parameter	Symbol	Test Conditions Unless Otherwise Specified V_{DD} = 4.5 to 5.5 V, V_B = 7.25 to 35 V		Temp[a]	Limits E Suffix: –40 to 125°C Min[b]	Typ[c]	Max[b]	Unit
Receiver								
K Input Low Voltage	V_{ILK}			Full		0.4 V_{BAT}	0.33 V_{BAT}	V
K Input High Voltage	V_{IHK}			Full	0.7 V_{BAT}	0.6 V_{BAT}		
K Input Hysteresis[d]	V_{HYS}			Full	0.1 V_{BAT}			
RX Output Low Voltage	V_{OLR}	$\overline{CS}$ = 4 V	V_{ILK} = 0.33 V_BAT, I_{OLR} = 1 mA	Full			0.4	
RX High Voltage	V_{OHR}		V_{IHK} = 0.70 V_BAT, I_{OHR} = –40 µA	Full	4			
K Input Currents	I_{IHK}		V_{IHK} = V_{BAT}	Full	1.5		20	µA
Supplies								
Bat Supply Current	I_{BAT}	$\overline{CS}$, TX = 1.5 V, K Open		Full		2.7	5.0	mA
Logic Supply Current	I_{DD}			Full		1	3.0	
Miscellaneous								
Baud Rate	BR	R_L = 510 Ω, C_L = 10 nF		Full	10.4			kBaud
Fault Output Low Voltage	V_{OLF}	$\overline{CS}$ = T_X = 0V, K = V_B, I_{OLF} = 1 mA		Full			0.4	V
$\overline{CS}$ Minimum Pulse Width[d, e]	t_{cs}			Full	1			µs

Notes
a. Room = 25°C, Cold and Hot = as determined by the operating temperature suffix.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. Guaranteed by design, not subject to production test.
e. Minimum pulse width to reset a fault condition.

Test Circuit (Transmit Only)



Application Circuit



ECU = Electronic Control Unit

Single-Ended Bus Transceiver

Features

- Single-Ended Transceiver
- Survives Shorts and Transients on Automotive Bus
- Wide Power Supply Voltage Range
- Fault Detection
- ISO 9141 Compatible

Description

The Si9243EY is a monolithic bus transceiver designed to provide bidirectional serial communication in automotive diagnostic applications.

The device incorporates protection against overvoltages and short circuits to GND or V_B. The transceiver pin is protected and can be driven beyond the V_{BAT} voltage.

The Si9243EY contains temperature and short circuit fault detection circuits. In the transmit mode, load shorts and opens are generally detected by the processor monitoring RXK and TX. When the two mirror each other there is no fault, but the Si9243EY will turn off the K output in the event of over temperature or short circuit to V_{BAT} to protect the IC. The fault will be reset when TX toggles "high."

TX is set "high" for receive only.

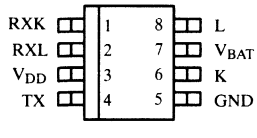
The RX output is capable of driving CMOS or 1 × LSTTL load.

The Si9243EY is built on the Siliconix BiC/DMOS process. This process supports bipolar transistors, CMOS, and DMOS. An epitaxial layer prevents latchup.

The Si9243EY is available in a 8-pin SO package and operates over the automotive temperature range (–40 to 125°C).

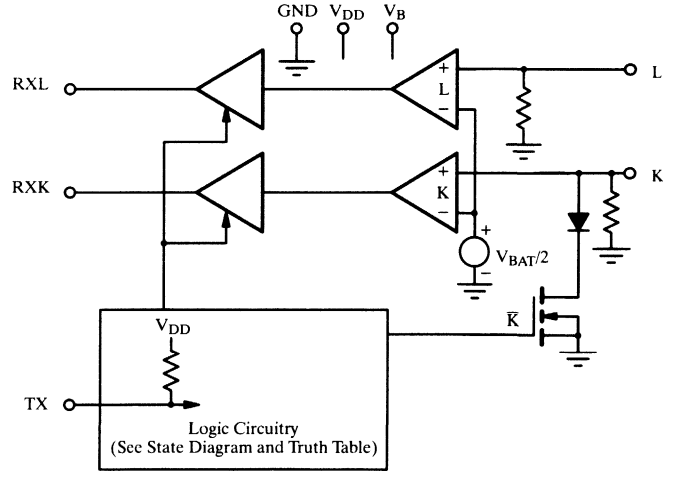
Pin Configuration and Functional Block Diagram

Narrow Body
SO Package



Top View

Order Number:
Si9243EY



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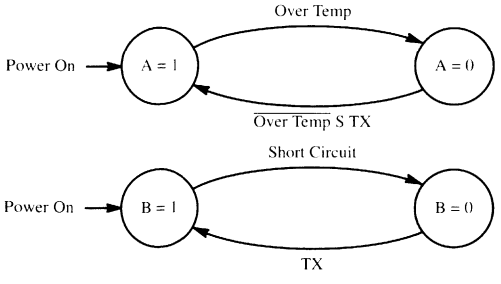
Output Table and State Diagrams



Note: Over Temp is a condition and not meant to be a logic signal.

Inputs	State Variable		Output Table				
TX	A	B	K	RXK	L	RXL	Comments
0	1	1	0	0	0	0	
1	1	1	1	1	1	1	
0	1	1	0	0	1	1	
1	1	1	1	1	0	0	
X	0	1	HiZ	K	L	L	Over Temp
0	1	0	HiZ	1	L	L	Short Circuit
1	1	1	1	1	1	1	Receive Mode
1	1	1	0	0	0	0	

X = "1" or "0"
HiZ = High Impedance State

Absolute Maximum Ratings

Voltage Referenced to Ground
Voltage On V_{BAT} ..... 45 V
Voltage K, L ..... –16 V to V_{BAT} + 1 V
Voltage On Any Pin (Except V_{BAT}, K, L)
or Max. Current ..... –0.3 V to V_{DD} + 0.3 V or 10 mA

Voltage on V_{DD} ..... 7 V
Short Circuit Duration (to V_{BAT} or GND) ..... Continuous
Operating Temperature (T_A) ..... –40 to 125°C
Junction and Storage Temperature ..... -55 to 150°C
Thermal Resistance Θ_{JA} ..... 125°C/W

Specifications

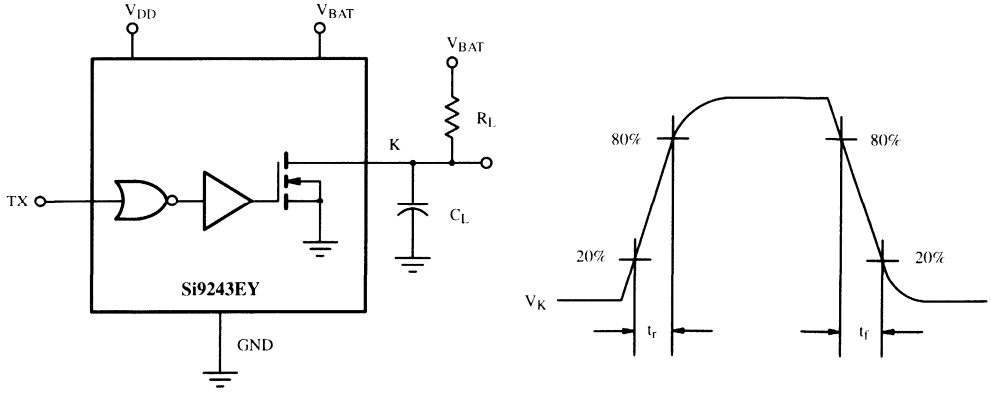
Parameter	Symbol	Test Conditions Unless Otherwise Specified V_{DD} = 4.5 to 5.5 V, V_{BAT} = 7.25 to 35 V	Temp[a]	Limits E Suffix: –40 to 125°C Min[b]	Typ[c]	Max[b]	Unit
Transmitter and Logic Levels							
TX Input Low Voltage	V_{ILT}		Full			1.5	V
TX Input High Voltage	V_{IHT}		Full	3.5			
K Output Low Voltage	V_{OLK}	R_L = 510 Ω, C_L = 10 nF V_{BAT} = 35 V, V_{DD} = 4.5 V	Full			4.9	
		R_L = 510 Ω, C_L = 10 nF See Test Circuit	Full			0.2 V_{BAT}	
K Output High Voltage	V_{OHK}		Full	0.91 V_{BAT}			
K Rise, Fall Times	t_r, t_f		Full			9.6	µs
K Output Sink Resistance	Rsi	TX = 0 V	Full			110	Ω
K Output Capacitance[d]	C_O		Full			20	pF
TX Input Capacitance[d]	C_{INT}		Full			10	
TX Input Current	I_{INT}	V_{DD} = 5.5 V, TX = 1.5 V, 3.5 V	Full	–60		–4	µA

Specifications

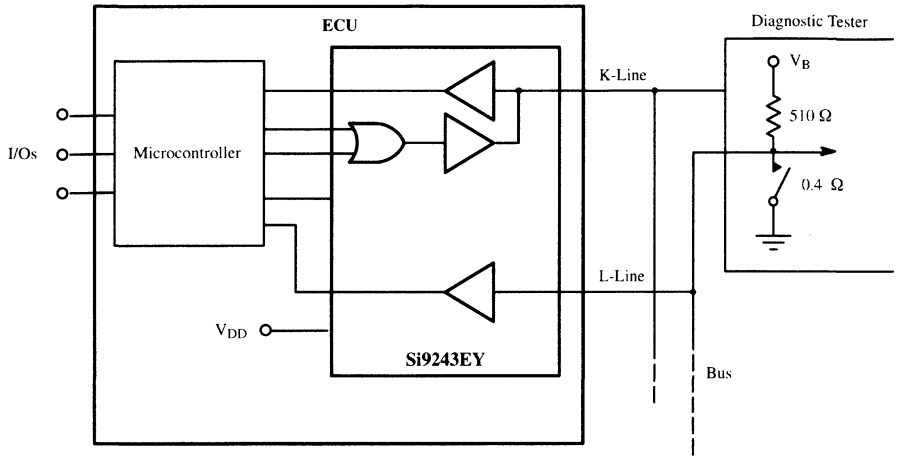
Parameter	Symbol	Test Conditions Unless Otherwise Specified V_{DD} = 4.5 to 5.5 V, V_B = 7.25 to 35 V		Temp[a]	Limits E Suffix: −40 to 125°C Min[b]	Typ[c]	Max[b]	Unit
Receiver								
L and K Input Low Voltage	V_{ILK}			Full		0.4 V_{BAT}	0.33 V_{BAT}	V
L and K Input High Voltage	V_{IHK}			Full	0.7 V_{BAT}	0.6 V_{BAT}		
L and K Input Hysteresis[d]	V_{HYS}			Full	0.1 V_{BAT}			
RXL and RXK Output Low Voltage	V_{OLR}	TX = 4 V	V_{ILK}, V_{ILL} = 0.33 V_{BAT} I_{OLR} = 1 mA	Full			0.4	
RXL and RXK High Voltage	V_{OHR}	TX = 4 V	V_{IHK}, V_{IHL} = 0.70 V_{BAT} I_{OHR} = −40 µA	Full	4			
L and K Input Currents	I_{IHK}	TX = 4 V	V_{IHK} = V_B	Full	1.5		20	µA
Supplies								
Bat Supply Current	I_{BAT}	TX = 1.5 V, K, L Open		Full		2.7	5.0	mA
Logic Supply Current	I_{DD}	TX = 1.5 V, K, L Open		Full		1	3.0	
Miscellaneous								
Baud Rate	BR	R_L = 510 Ω, C_L = 10 nF		Full	10.4			kBaud
TX Minimum Pulse Width[d, e]	t_{TX}			Full	1			µs

Notes
a. Room = 25°C, Cold and Hot = as determined by the operating temperature suffix.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. Guaranteed by design, not subject to production test.
e. Minimum pulse width to reset a fault condition.

Test Circuit



Application Circuit



ECU = Electronic Control Unit

Driver ICs for Automotive Diagnostic Communications Meet ISO 9141 Standards

by John Bendel

A series of compact, single-ended bus drivers for automotive diagnostic applications enables communication over the relatively long distances between testing equipment and automotive electronic control units, while protecting sensitive logic devices from the hazards of the automotive environment. The Si9241EY and Si9243EY are the first narrow-body, small outline products on the market to meet the ISO 9141 standard for this application.

ISO 9141 (General Description)

ISO 9141 is an international standard for communications between automobiles and diagnostic testers. It specifies a serial data communication bus between the vehicle's Electronic Control Units (ECUs) and the diagnostic test SAE OBDII Scan Tool (SAE J 1978). ISO 9141 has been adopted by the California Air Resources Board for all cars sold in California with feedback fuel control systems. Similar rules are being adopted in New York, New Jersey, Massachusetts, and Maryland, and are expected to affect the design of most cars sold in the United States.

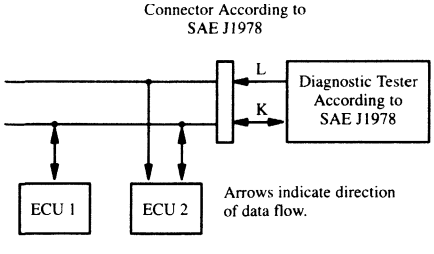


Figure 1. Possible System Configuration

Figure 1 is a system configuration for the ISO 9141 specification. The primary form of communication is with the single-ended K-Line. The K-Line passes data bidirectionally, as well as transferring all address information during initialization.

The optional L-Line is unidirectional and is only used to pass address information from the diagnostic tester to the ECUs during initialization. The L-Line is in a 1-state during all other events. The K-Line will mimic the L-Line's address initialization.

Siliconix ISO 9141 Drivers

Siliconix has produced two drivers to meet ISO 9141 configurations. Each driver is housed in a small-outline surface-mount package with on-board fault protection to protect the controller and tester from the automotive environment.

Both drivers have short circuit and over-temperature protection and open load detection. The devices protect against voltage transients (-3 V ^{3} [V_{BAT}, K and L] $\leq$ 45 V), which exceed ISO 9141 (–1 V to 40 V).

The Drivers

The Si9241EY (Figure 2) is designed for the user that needs only K-Line communication. The ECU controls the K output through Transmit Pin (Tx) and Chip Select Bar ($\overline{CS}$). The fault detection circuitry monitors Tx and K to determine open and shorted loads. If K is high when Tx is low, the K-Line is shorted. Conversely, if K is low when Tx is high, the K-Line is open. Over-temperature protection is always enabled, so a fault is determined whenever the junction temperature exceeds 150°C. All faults are latched until chip select bar is set high.

If chip select is not to be used, TX and $\overline{CS}$ Bar should be tied together, so all faults will reset when TX toggles high.

The Si9243EY (Figure 3) is designed for users that need both K and L Lines for communication. It is packaged in an SO-8 for space savings, but due to pin limitation, it does not have a chip select function. For the same reason, the Fault Detection signal is not bonded out. The fault detection and protection circuitry are active, and the device will shut down in the event of a fault.

Updates to this app note may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70573.

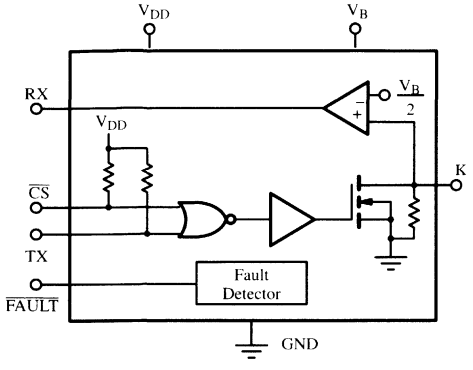


Figure 2. Si9241 K-Line Only Driver

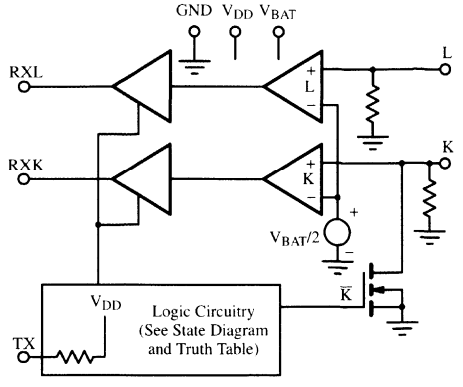


Figure 3. Si9243 K- and L-Line Driver

Since the fault detection signal is not brought out, it is up to the user to determine if a fault has occurred. One method is to monitor the RxK and TX lines and ensure they are in phase. An exclusive OR can also perform the fault function.

The fault condition is cleared when TX is set high.

System Anomalies

Two system anomalies in the automotive environment that the Si924x drivers may be subjected to are Reverse Battery and Ground Disconnect.

The Si924x drivers have an integrated diode in the V_{BAT} line to protect the device from reverse battery conditions. This diode will protect the IC to reverse batteries up to –18 V.

It is more difficult to protect the device against a ground disconnect. If the ground of an Si924x driver is disconnected and allowed to float, it is possible for the V_{DD} protection diode to forward conduct into the V_{BAT} line. A 100-Ω series resistor in the V_{DD} line will limit the current and prevent the device from failing as shown in Figure 4.

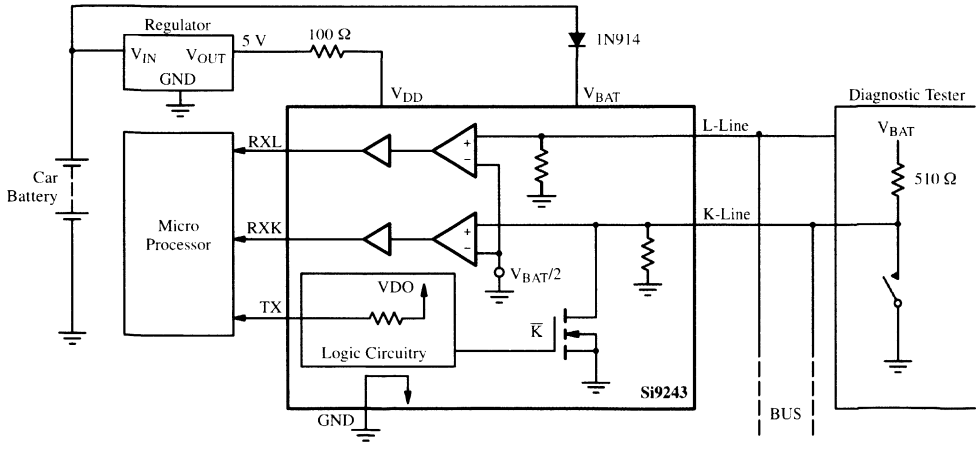


Figure 4. Si9243EY Applications Circuit

A second potential failure during ground disconnects is if the K-Line goes 8 V above the Bat line, while V_{DD} is still connected. Current will flow through the K-Line to V_{BAT} through a parasitic n-p-n. To remedy this situation, a diode must be placed in series with the V_{BAT} line (Figure 4). This condition will not occur if $\overline{CS}$ and TX are low.

Signal and Communication Specifications

ISO 9141 specifies different logic levels for the Receiver and Transmitter.

Receiver Logic Levels:

Logic "0" ≤ 0.3 * V_{BAT}
0.7 * V_{BAT} [3] Logic "1"

Transmitter Logic Levels:

Logic "0" ≤ 0.2 * V_{BAT} 0.8 *
V_{BAT} ≥ Logic "1"

The Siliconix drivers operate to the above specifications, but with a slightly tighter transmission requirement: Logic "1" minimum ≥ 0.91*V_{BAT}.

A logic bit transition must be less than 10% of the total bit time. The transition time is measured between the 80% and 20% battery points. Bit time is defined as the time between the 50% battery points of consecutive rising and falling levels.

Physical Layer

Figure 5 shows the physical layer capacitance of the ISO 9141 communication scheme.

C_{TE} = Tester and Cables

C_{OBW} = On-Board Wiring

C_{ECU} = Sum of all ECU Input Capacitance

where C_{ECU} + C_{OBW} is less or equal to 7.6 nF and C_{TE} is less or equal to 2 nF.

The capacitance of the K or L Lines with respect to GND can be no greater than 500 pF.

The resistance of the K and L Line is specified with respect to their State.

Logic "1"/Receiving	Logic "0"
K (ECU to GND)	≥ 50 kW ≤ 110 W
L (ECU to GND)	≥ 50 kW N/A

Any resistance placed between the K or L Line and V_b must have a value greater than 100 kΩ.

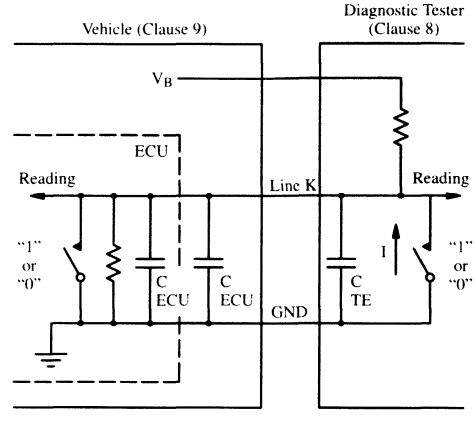


Figure 5. Communication Schematic

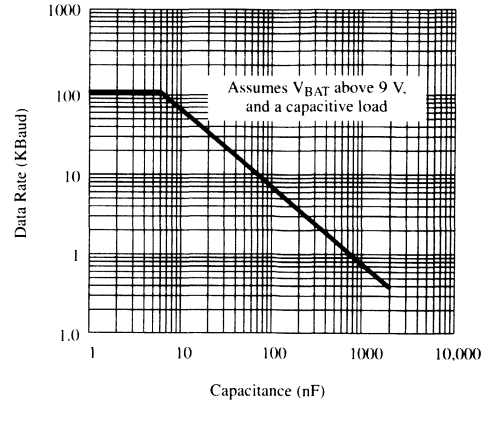


Figure 6. Maximum NRZ Data Rate with Capacitive Load Si924X with 510-Ω Load

Data Rate

The maximum data rate will vary depending on the number of ECUs and length of cabling. ISO 9141 specifies a maximum bus capacitance of 9.6 nF. Figure 6 shows the maximum data rate versus capacitance.

Data Format and Protocol

This application note will only give a general outline of the ISO 9141 communication scheme. The user is advised to read the actual ISO 9141 specification.

Initialization

Before initialization, the K-Line is a Logic 1 for the time period of the address to be transmitted. The diagnostic tester then sends an 8-bit address on the K and L lines (one start, 8-bit address, one stop) to the ECU.

Transmission

Before transmitting, the K-Line is a Logic 1 for the time period of the word to be transmitted. An alternate bit pattern is then sent to synchronize the receiver and set the baud rate. After the transmission of the synchronization pattern, two key words are sent to the tester to identify the form of the data and the hardware configuration.

When the last key word is sent by the ECU, the tester will echo back the logic inversion of the last word back to the ECU. When this is complete, the ECU will transmit the logic inversion of the initialization address.

Conclusion

Siliconix' ISO 9141 bus driver series is produced to save the automotive designer time and space while improving the overall reliability of the diagnostic system. Each driver exceeds the ISO 9141 transient and data requirements, as well saving significant space overall to a discrete solution. With these factors considered, it should reduce manufacturing, building and design costs, and produce a very economical solution to automotive bus interfacing.

Reference

ISO 9141 - CARB Road Vehicles – Diagnostic Systems. N425/rev. Jan. 91

Reliability Information

Introduction

Reliability at Siliconix is ensured with two primary programs: the Reliability Qualification Program and the Reliability Monitoring Program. Siliconix publishes this data by product family and it can be obtained by request through your local sales office.

Qualification Program

Qualification programs of accelerated stress testing are developed for the introduction of new devices (die qualifications), packages, major process changes, new materials or suppliers, new manufacturing equipment, and new manufacturing locations.

A qualification starts after a qualification test plan is developed. This plan specifies the following:

- Purpose and scope
- Device or geometry types and packages being qualified
- Process and assembly specs involved
- Test vehicles and location
- Tests and stresses
- Duration of each stress
- Sample sizes
- Acceptance criteria
- Number of lots required

Monitoring Program

The Reliability Monitoring Program, which includes accelerated life tests, is designed to continuously monitor product reliability. The program furnishes up-to-date failure-rate and failure-mechanism data which can be used to predict and improve long-term reliability performance. The Monitoring Program covers a wide range of technologies and product lines manufactured by Siliconix. In order to accomplish this, products are grouped by similar technologies. For example, components built in the same wafer fab, using the same manufacturing processes, having similar complexity, functionality, and package types are grouped into a technology family. One component or more representing each technology group is monitored according to a quarterly schedule.

The short-term and long-term monitor tests are outlined in Tables 1 and 2. Also, the Reliability Monitor Program is summarized in general outline form as a flow chart in Figure 1 and with operating life data in Table 3.

Accelerated Reliability

Accelerated tests were developed to shorten the time required for reliability testing. The life cycle of a component is accelerated by applying stress that is more severe than that encountered under normal operating conditions. This acceleration is produced by elevating temperatures, increasing humidity or pressure, alternating hot and cold temperature, switching power on and off, or some combination of these conditions. The test results are used to predict normal operating performance. In the sections below we present a brief description of each stress.

Summary of Tests

High-Temperature Operational Life (HTOL) Test

The HTOL accelerated test is performed under dynamic (clocked) biasing state at an elevated temperature between 125°C and 150°C. During the stress condition it is intended circuits throughout the part toggle at various clock frequencies with the highest fault coverage at critical nodes as possible. In some cases the outputs of the DUTs are passively loaded and monitored. Devices are normally tested at 168 hours (providing failure rates due to infant mortality), 500 hours and 1000 hours for use life failure rates. Failure rates are reported in FITs – Failure In Time.

High-Temperature Static Life (HTSL) Test

The HTSL accelerated test is performed with the DUT powered up at maximum V_{CC} operating voltage and at 150°C. The input pins are biased either at high or low state and the outputs are normally floating. The test is intended to detect the reliability hazards rising from junction engineering, defects or contamination. Devices are tested at 168 hours (infant mortality), 500 hours and 1000 hours, and the failure rates are reported in FITs –Failure In Time.

Temperature Cycling Test

Temperature cycling exploits the differences in thermal coefficients of expansion between silicon and the other materials used in die fabrication and packaging. Each cycle consists of 10-minute exposures (–65°C for Power ICs) and 150°C with a 1-minute transfer at room temperature between the temperature extremes. This test reveals potential weaknesses in die and package materials and construction and in the integration of the die and package.

Thermal Shock Test

The purpose of the thermal shock test is similar to that of temperature cycling. This stress is more extreme, however, due to the fact that the ambient medium is liquid and not air, and the transition time is much shorter than for temperature cycling.

Each cycle consists of a 5-minute exposure at –60°C or –65° and 150°C with a maximum 10-second transfer time between the temperature extremes.

Bias Humidity Test

The bias humidity test is used to test plastic packaged devices for the effects of moisture penetration while electrical potentials are applied. The components are placed in a biased condition and then are subjected for 1000 hours to a temperature of 85°C and a relative humidity 85%. This test confirms package integrity.

Pressure Pot Test

In the pressure pot test, water vapor is forced into non-hermetic packages via micro gaps in the package-lead seal. Water is then carried to the die surface via capillary action of the bond wires. Electrical leakage may result. External contamination of the package or lead finish may be transported to the die or may directly cause corrosion of the leads.

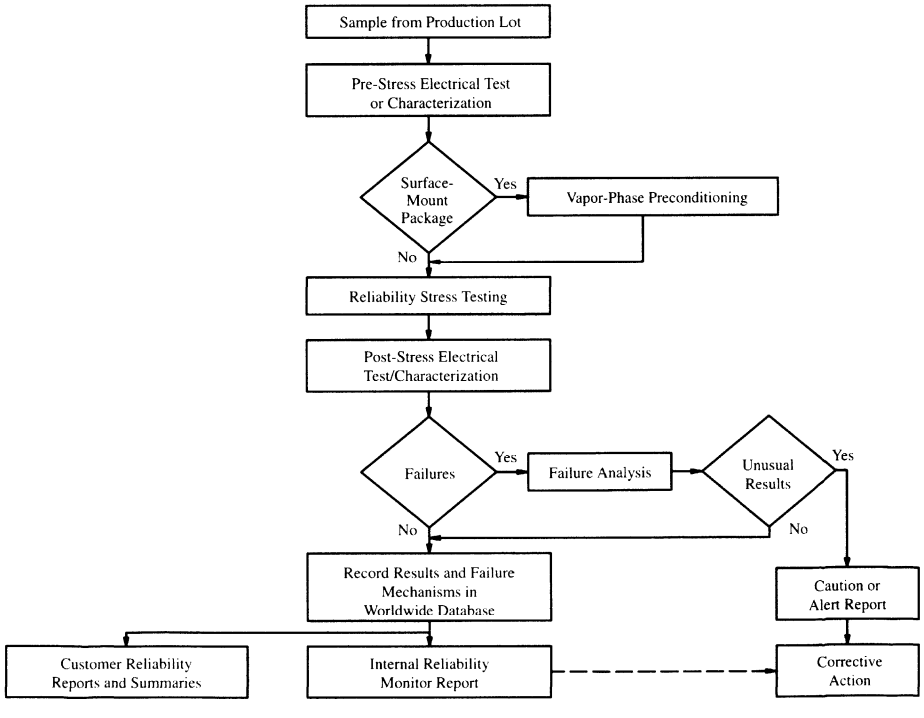


Figure 1. Reliability Monitor Flow (Short- and Long-Term Monitors)

Power IC's

Table 1. Short-Term Reliability Monitor for Power IC's

Test	Condition	Sample Size	Test Points
Static Operating Life	125°C or 150°C	50	168 hours
Dynamic Operating Life			
Pressure Pot	121°C, 15 PSIG		96 hours (Plastic)
Thermal Shock	Liquid to liquid. –60°C to 150°C		100 cycles
Solderability	MIL-STD-883D, M2003	15 leads	(245°C ±5°C)
Lead Integrity	MIL-STD-883D, M2004		
Lid Torque	MIL-STD-883D, M2024		(Hermetic)
Marking Permanency	MIL-STD-883D, M2015	16	
Salt Atmosphere	MIL-STD-883D, M1009	15	24 hours (Hermetic)

Table 2. Long-Term Reliability Monitor

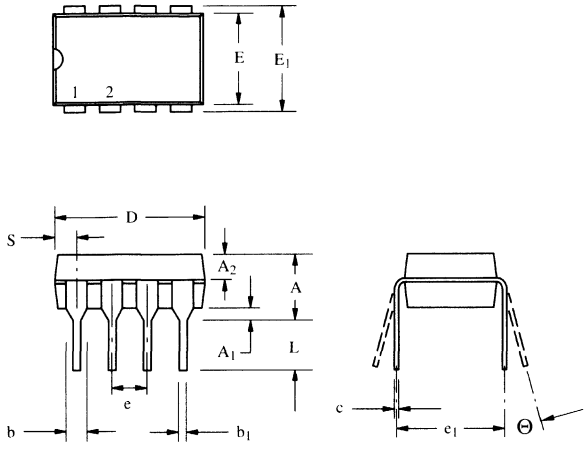
Test	Condition	Sample Size	Test Points
Static Operating Life	125°C or 150°C	50	0, 168, 1000 hours
Dynamic Operating Life			
Biased Humidity (Plastic)	85°C, 85% relative humidity		0, 500, 1000 hours
Temperature Cycling	Air-to-air –60°C to 150°C		0, 250, 1000 cycles

Table 3. Operating Life Data

High Temperature Operating Life Technology	Number of Units	Equivalent Device Hours at 55°C and 0.6 eV	FITs[a]	
			0.6 eV	1.0 eV
Power IC	2,097	4,618,752,555	7.2	0.35

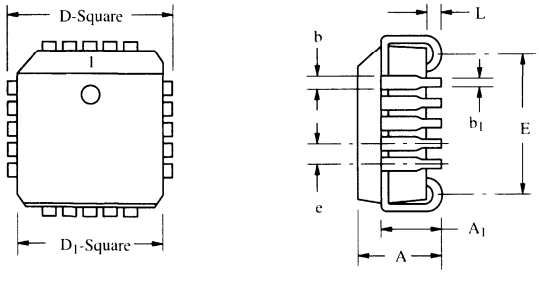
Note:
a. 1 failure per billion device hours

Plastic DIP: 8, 14, 16 and 20 Leads



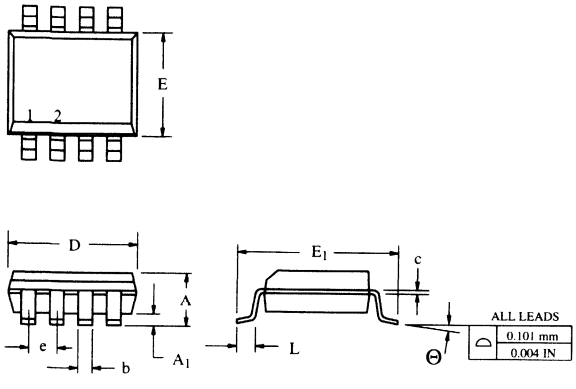
Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	3.81	5.08	0.150	0.200
A_1	0.38	1.27	0.015	0.050
A_2	1.27	2.03	0.050	0.080
b	0.89	1.65	0.035	0.065
b_1	0.38	0.51	0.015	0.020
c	0.20	0.30	0.008	0.012
D–8	9.65	11.68	0.380	0.460
D–14	17.27	19.30	0.680	0.760
D–16	18.93	21.33	0.745	0.840
D–20	24.89	26.92	0.980	1.060
E	5.59	7.11	0.220	0.280
E_1	7.62	8.26	0.300	0.325
e	2.29	2.79	0.090	0.110
e_1	7.37	7.87	0.290	0.310
L	2.79	3.81	0.110	0.150
S–8	1.02	2.03	0.040	0.080
S–14	1.02	2.03	0.040	0.080
S–16	0.38	1.52	0.015	0.060
S–20	1.02	2.03	0.040	0.080
Θ	0°	15°	0°	15°

PLCC: 20, 28, 44, 52, 68, and 84 Leads



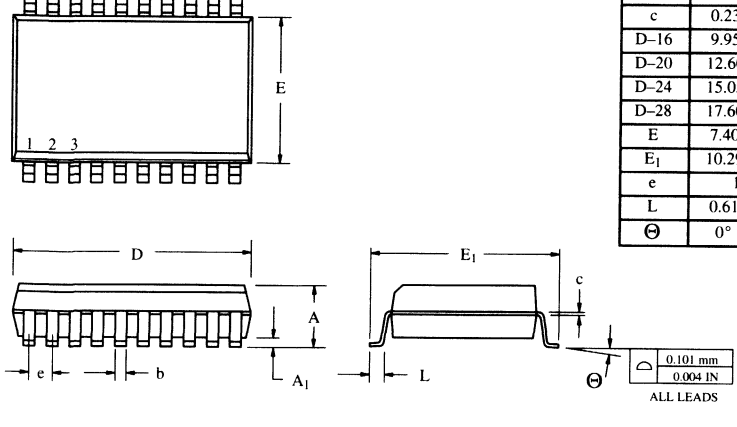
Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	4.20	4.57	0.165	0.180
A_1	2.29	3.04	0.090	0.120
b	0.66	0.81	0.026	0.032
b_1	0.33	0.55	0.013	0.021
D-20	9.78	10.03	0.385	0.395
D-44	17.40	17.65	0.685	0.695
D-28	12.32	12.57	0.485	0.495
D-52	19.94	20.19	0.785	0.795
D-68	25.02	25.27	0.985	0.995
D-84	30.10	30.35	1.185	1.195
D_1-20	8.89	9.04	0.350	0.356
D_1-28	11.43	11.58	0.450	0.456
D_1-44	16.51	16.66	0.650	0.656
D_1-52	19.05	19.25	0.750	0.758
D_1-68	24.13	24.33	0.950	0.958
D_1-84	29.21	29.41	1.150	1.158
E-20	9.78	10.03	0.385	0.395
E-28	9.91	10.92	0.390	0.430
E-44	17.40	17.65	0.685	0.695
E-52	19.94	20.19	0.785	0.795
E-68	25.02	25.27	0.985	0.995
E-84	30.10	30.35	1.185	1.195
e	1.27 BSC		0.050 BSC	
L	0.51	–	0.020	–

SOIC: 8, 14, and 16 Leads



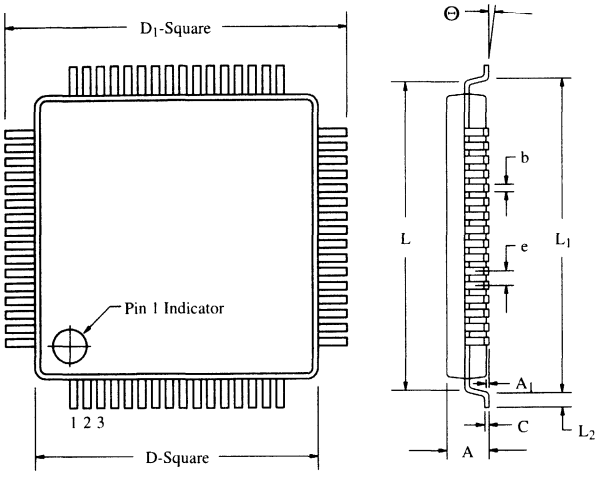
Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A_1	0.10	0.20	0.004	0.008
B	0.35	0.45	0.014	0.018
c	0.18	0.23	0.007	0.009
D-8	4.69	5.00	0.185	0.196
D-14	8.55	8.75	0.336	0.344
D-16	9.80	10.00	0.385	0.393
E	3.80	4.00	0.149	0.157
E_1	5.80	6.20	0.228	0.244
e	1.27 BSC		0.050 BSC	
L	0.50	0.93	0.020	0.037
Θ	0°	8°	0°	8°

SOIC, Wide-Body: 16, 20, 24, and 28 Leads



Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	2.35	2.64	0.093	0.104
A_1	0.10	0.30	0.004	0.012
b	0.35	0.45	0.014	0.018
c	0.23	0.28	0.009	0.011
D–16	9.95	10.75	0.392	0.423
D–20	12.60	12.98	0.496	0.511
D–24	15.05	15.85	0.593	0.624
D–28	17.60	18.40	0.693	0.724
E	7.40	7.59	0.291	0.299
E_1	10.29	10.59	0.405	0.417
e	127 BSC		0.050 BSC	
L	0.61	0.99	0.024	0.039
Θ	0°	8°	0°	8°

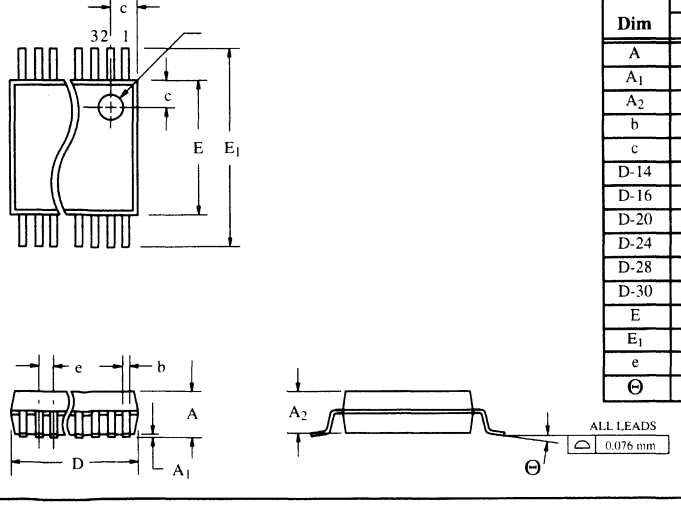
SQFP: 48 and 64 Leads



Dim	Millimeters		Inches*	
	Min	Max	Min	Max
A	1.35	1.60	0.053	0.063
A_1	0.04	0.16	0.002	0.006
b	0.14	0.26	0.006	0.010
C	0.117	0.177	0.005	0.007
D-48	6.90	7.10	0.272	0.280
D-64	9.90	10.10	0.390	0.398
D_1-48	8.70	9.30	0.343	0.366
D_1-64	11.7	12.3	0.461	0.484
e	0.40	0.60	0.016	0.024
L-48	–	7.80	–	0.307
L-64	–	10.80	–	0.425
L_1-48	7.80	8.20	0.307	0.323
L_1-64	10.80	11.20	0.425	0.441
L_2	0.30	0.70	0.012	0.028
Θ	0°	7°	0°	7°

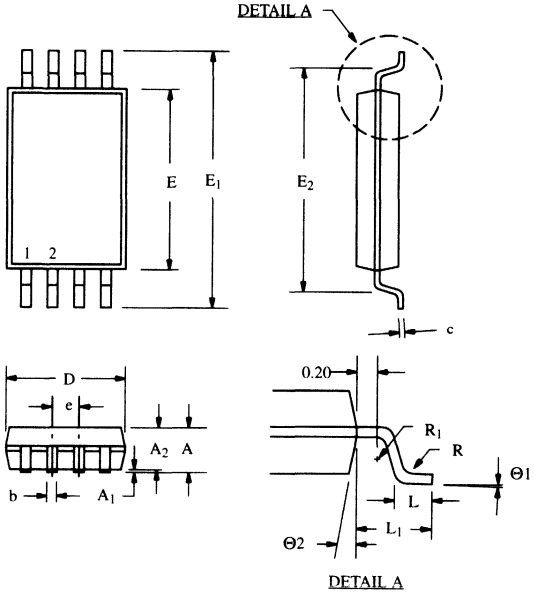
*For Reference Only

SSOP: 14, 16, 20, 24, 28, and 30 Leads



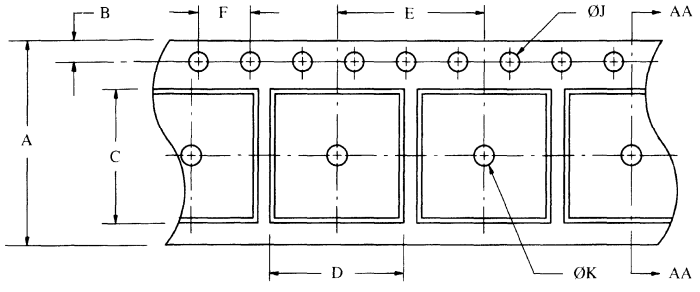
Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	1.73	1.99	0.068	0.078
A_1	0.05	0.21	0.002	0.008
A_2	1.68	1.78	0.066	0.070
b	0.25	0.38	0.010	0.015
c	1.14		0.045	
D-14	6.07	6.33	0.239	0.249
D-16	6.07	6.33	0.239	0.249
D-20	7.07	7.33	0.278	0.289
D-24	8.07	8.33	0.318	0.328
D-28	10.07	10.33	0.397	0.407
D-30	10.07	10.33	0.397	0.407
E	5.20	5.38	0.205	0.212
E_1	7.65	7.90	0.301	0.311
e	0.65 BSC		0.0256 BSC	
Θ	0°	8°	0°	8°

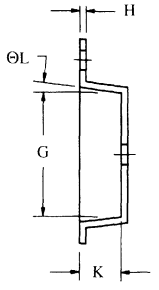
TSSOP: 8, 16, and 28 Leads



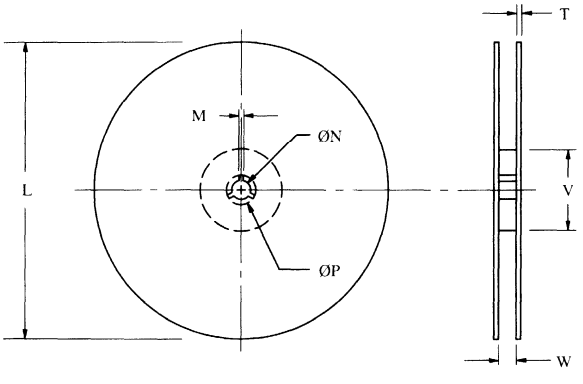
Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	1.05	1.20	0.041	0.047
A_1	0.05	0.15	0.002	0.006
A_2	–	1.05	–	0.041
b	0.25	0.30	0.010	0.012
c	0.127		0.005	
D-8	2.90	3.10	0.114	0.122
D-16	4.90	5.10	0.193	0.201
D-28	9.60	9.80	0.378	0.386
E	4.30	4.50	0.170	0.177
E_1	6.10	6.70	0.240	0.264
E_2	5.14	5.24	0.202	0.206
e	0.65 BSC		0.025 BSC	
L	0.50	0.70	0.020	0.028
L_1	1.0		0.039	
R	0.09	–	0.004	–
R_1	0.09	–	0.004	–
Θ1	0°	8°	0°	8°
Θ2	12°			

Tape and Reel Options





SECTION A-A



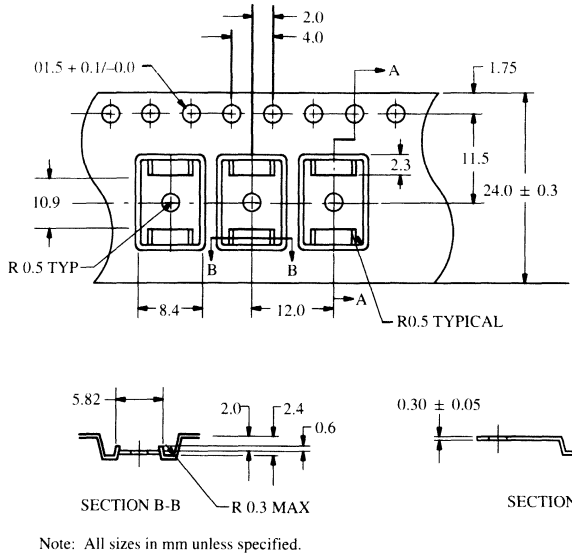
Quantity Per Reel	
SOIC Narrow	2500
SOIC Widebody	1500
SSOP	2000
TSSOP	3000

	SO-8				SO-14				SO-16			
	Millimeters		Inches		Millimeters		Inches		Millimeters		Inches	
Dim	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
A	11.9	12.1	0.469	0.476	15.9	16.1	0.626	0.634	15.9	16.1	0.626	0.634
B	1.65	1.85	0.065	0.073	1.65	1.85	0.065	0.073	1.65	1.85	0.065	0.073
C	5.10	5.30	0.201	0.209	9.05	9.25	0.356	0.364	10.35	10.55	0.407	0.415
D	6.30	6.50	0.248	0.256	6.55	6.75	0.258	0.266	6.55	6.75	0.258	0.266
E	7.90	8.60	0.311	0.339	7.90	8.10	0.311	0.319	7.90	8.10	0.311	0.319
F	3.90	4.10	0.154	0.161	3.90	4.10	0.154	0.161	3.90	4.10	0.154	0.161
G	5.10	5.30	0.200	0.209	9.05	9.25	0.356	0.364	10.35	10.55	0.407	0.415
H	0.25	0.35	0.010	0.014	0.25	0.35	0.010	0.014	0.25	0.35	0.010	0.014
ØJ	1.50	1.60	0.059	0.063	1.50	1.60	0.060	0.063	1.50	1.60	0.060	0.063
K	1.90	2.30	0.075	0.091	1.90	2.30	0.075	0.091	1.90	2.30	0.075	0.091
ØK	1.50	1.70	0.059	0.067	1.40	1.60	0.055	0.063	1.40	1.60	0.055	0.063
L	328	332	12.91	13.07	328	332	12.91	13.07	328	332	12.91	13.07
ΘL	–	3°	–	3°	–	3°	–	3°	–	3°	–	3°
M	1.50	2.50	0.059	0.098	1.50	2.50	0.059	0.098	1.50	2.50	0.059	0.098
ØN	12.8	13.2	0.504	0.520	12.8	13.2	0.054	0.520	12.8	13.2	0.054	0.520
ØP	21.5	22.5	0.847	0.886	21.5	22.5	0.847	0.886	21.5	22.5	0.847	0.886
T	1.00	2.00	0.039	0.078	1.00	2.00	0.039	0.078	1.00	2.00	0.039	0.078
V	53.0	54.0	2.087	2.126	53.0	54.0	2.087	2.126	53.0	54.0	2.087	2.126
W	12.4	14.4	0.488	2.667	16.4	18.4	0.646	0.724	16.4	18.4	0.646	0.724

Tape and Reel Options (Cont'd)

	SO-16 (Widebody)				SO-20 (Widebody)				SO-24 (Widebody)			
	Millimeters		Inches		Millimeters		Inches		Millimeters		Inches	
Dim	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
A	10.3	11.2	0.406	0.441	10.3	11.2	0.406	0.441	10.3	11.2	0.406	0.441
B	1.65	1.85	0.065	0.073	1.65	1.85	0.065	0.073	1.65	1.85	0.065	0.073
C	10.6	10.8	0.417	0.425	13.2	13.4	0.520	0.528	15.9	16.1	0.626	0.634
D	10.8	11.0	0.425	0.433	10.8	11.0	0.425	0.433	10.8	11.0	0.425	0.433
E	11.9	12.1	0.469	0.476	11.9	12.1	0.469	0.476	11.9	12.1	0.469	0.476
F	3.90	4.10	0.154	0.161	3.90	4.10	0.154	0.161	3.90	4.10	0.154	0.161
G	10.6	10.8	0.417	0.425	13.2	13.4	0.520	0.528	15.9	16.1	0.626	0.634
H	0.25	0.35	0.010	0.014	0.25	0.35	0.010	0.014	0.25	0.35	0.010	0.014
ØJ	1.50	1.60	0.059	0.063	1.50	1.60	0.059	0.063	1.50	1.60	0.059	0.063
K	2.8	3.2	0.110	0.126	2.8	3.2	0.110	0.126	2.8	3.2	0.110	0.126
ØK	1.50	1.70	0.059	0.067	1.50	1.70	0.059	0.067	1.50	1.70	0.059	0.067
L	328	332	12.91	13.07	328	332	12.91	13.07	328	332	12.91	13.07
ΘL	–	3°	–	3°	–	3°	–	3°	–	3°	–	3°
M	1.50	2.50	0.059	0.098	1.50	2.50	0.059	0.098	1.50	2.50	0.059	0.098
ØN	12.8	13.2	0.504	0.520	12.8	13.2	0.504	0.520	12.8	13.2	0.504	0.520
ØP	21.5	22.5	0.847	0.886	21.5	22.5	0.847	0.886	21.5	22.5	0.847	0.886
T	1.00	2.00	0.039	0.078	1.00	2.00	0.039	0.078	1.00	2.00	0.039	0.078
V	53.0	54.0	2.087	2.126	53.0	54.0	2.087	2.126	53.0	54.0	2.087	2.126
W	24.4	26.4	0.961	1.039	24.4	26.4	0.961	1.039	24.4	26.4	0.961	1.039

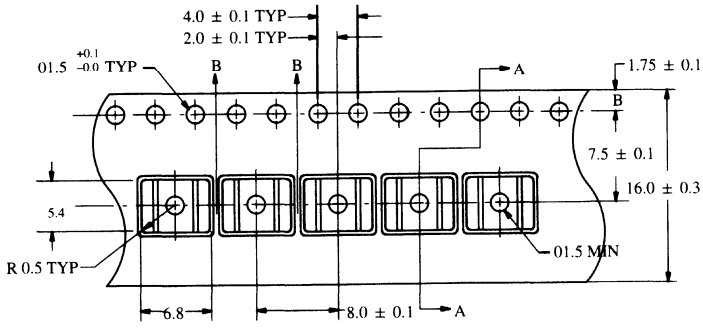
Tape and Reel Option for SSOP, 28-Pin

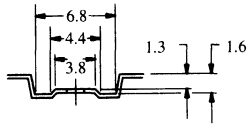


Note: All sizes in mm unless specified.

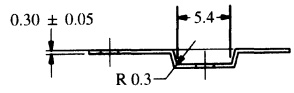
5
Appendix

Tape and Reel Option for TSSOP, 16-Pin





SECTION B-B



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Note: All sizes in mm unless specified.

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Rancho Cordova
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JAN Devices
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